# KSZ8091MLX

## 10BASE-T/100BASE-TX Physical Layer Transceiver

### Features

- Single-Chip 10BASE-T/100BASE-TX IEEE 802.3 Compliant Ethernet Transceiver
- MII Interface Support
- Back-to-Back Mode Support for a 100 Mbps Copper Repeater
- MDC/MDIO Management Interface for PHY Register Configuration
- Programmable Interrupt Output
- LED Outputs for Link, Activity, and Speed Status Indication
- On-Chip Termination Resistors for the Differential Pairs
- Baseline Wander Correction
- HP Auto MDI/MDI-X to Reliably Detect and Correct Straight-Through and Crossover Cable Connections with Disable and Enable Option
- Auto-Negotiation to Automatically Select the Highest Link-Up Speed (10/100 Mbps) and Duplex (Half/Full)
- Energy Efficient Ethernet (EEE) Support with Low-Power Idle (LPI) Mode and Clock Stoppage for 100BASE-TX and Transmit Amplitude Reduction with 10BASE-Te Option
- Wake-on-LAN (WOL) Support with Either Magic Packet, Link Status Change, or Robust Custom-Packet Detection
- LinkMD® TDR-Based Cable Diagnostics to Identify Faulty Copper Cabling
- HBM ESD Rating (6 kV)
- Parametric NAND Tree Support for Fault Detection Between Chip I/Os and the Board
- Loopback Modes for Diagnostics
- Power-Down and Power-Saving Modes
- Single 3.3V Power Supply with $V_{DD}$ I/O Options for 1.8V, 2.5V, or 3.3V
- Built-In 1.2V Regulator for Core
- Available in 48-Pin 7 mm x 7 mm LQFP Package

### Target Applications

- Game Consoles
- IP Phones
- IP Set-Top Boxes
- IP TVs
- LOM
- Printers

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## Table of Contents

# 1.0 INTRODUCTION

## 1.1 General Description

The KSZ8091MLX is a single-supply 10BASE-T/100BASE-TX Ethernet physical layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

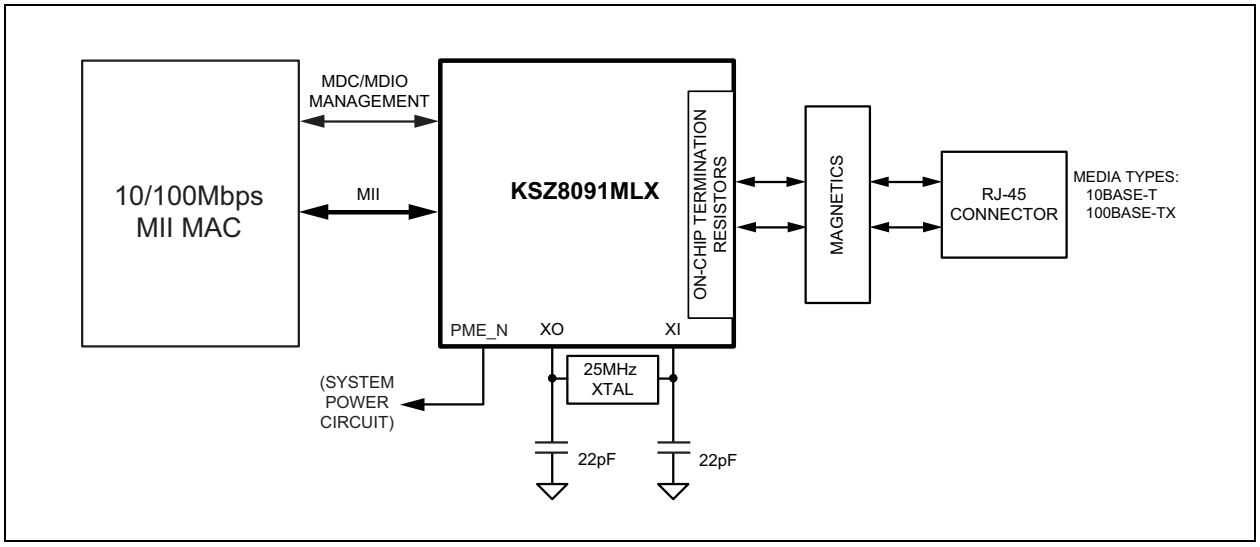
The KSZ8091MLX is a highly-integrated, compact solution. It reduces board cost and simplifies board layout by using on-chip termination resistors for the differential pairs, by integrating a low-noise regulator to supply the 1.2V core, and by offering a flexible 1.8/2.5/3.3V digital I/O interface.

The KSZ8091MLX offers the Media Independent Interface (MII) for direct connection with MII-compliant Ethernet MAC processors and switches.

Energy Efficient Ethernet (EEE) provides further power saving during idle traffic periods and Wake-on-LAN (WOL) provides a mechanism for the KSZ8091MLX to wake up a system that is in standby power mode.

The KSZ8091MLX is available in the 48-pin, lead-free LQFP package.

**FIGURE 1-1: SYSTEM BLOCK DIAGRAM**



## 2.0 PIN DESCRIPTION AND CONFIGURATION

**FIGURE 2-1: 48-PIN 7 MM X 7 MM LQFP ASSIGNMENT (TOP VIEW)**

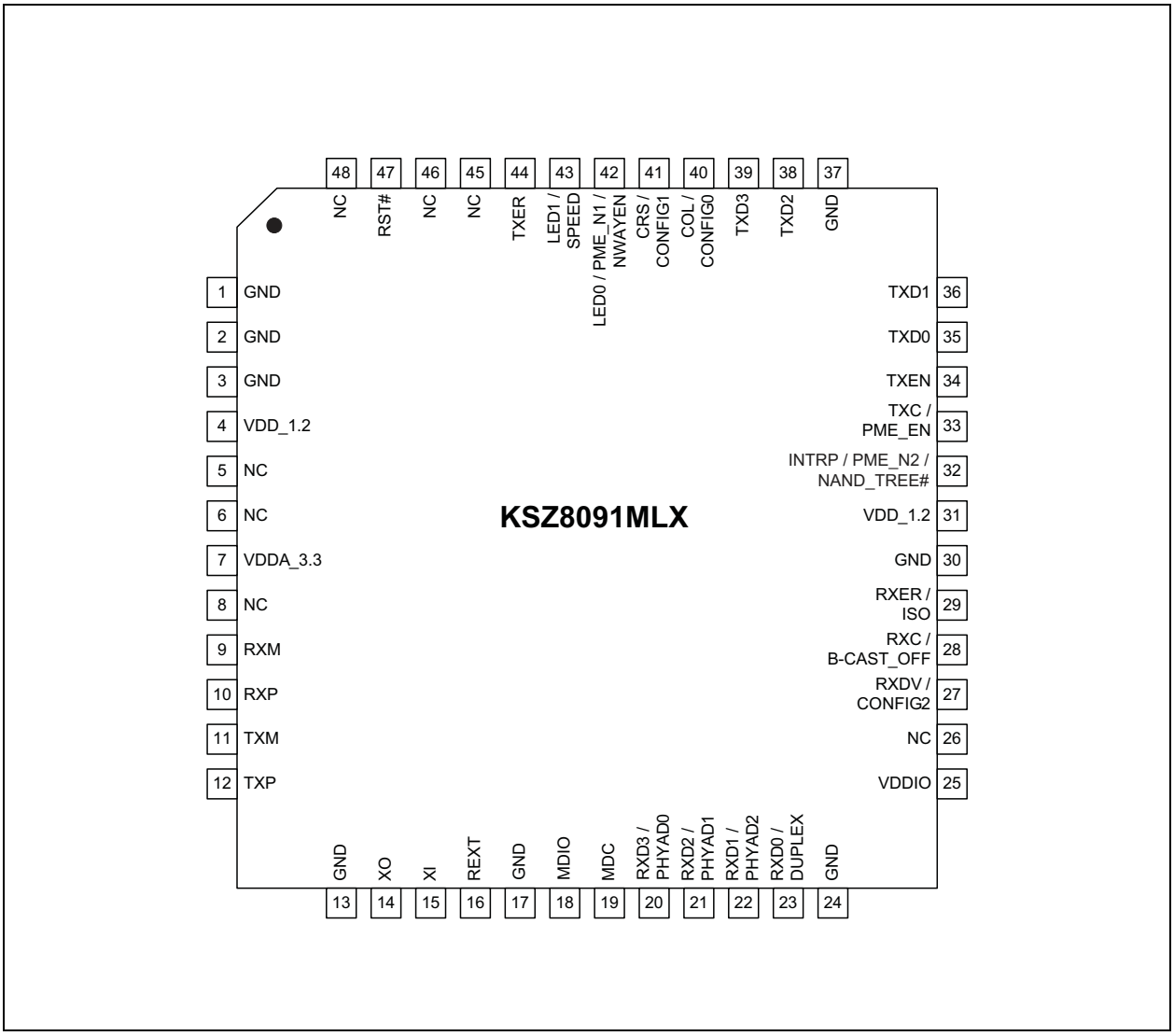


**TABLE 2-1: SIGNALS - KSZ8091MLX**

| Pin Number | Pin Name | Type Note 2-1 | Description |
|---|---|---|---|
| 1 | GND | GND | Ground. |
| 2 | GND | GND | Ground. |
| 3 | GND | GND | Ground. |
| 4 | VDD_1.2 | P | 1.2V core $V_{DD}$. (Power supplied by KSZ8091MLX.)<br>Decouple with 2.2 µF and 0.1 µF capacitors to ground, and join with Pin 31 by power trace or plane. |
| 5 | NC | — | No Connect. This pin is not bonded and can be left floating. |
| 6 | NC | — | No Connect. This pin is not bonded and can be left floating. |
| 7 | VDDA_3.3 | P | 3.3V analog $V_{DD}$. |
| 8 | NC | — | No Connect. This pin is not bonded and can be left floating. |
| 9 | RXM | I/O | Physical Receive or Transmit Signal (– differential). |
| 10 | RXP | I/O | Physical Receive or Transmit Signal (+ differential). |
| 11 | TXM | I/O | Physical Transmit or Receive Signal (– differential). |
| 12 | TXP | I/O | Physical Transmit or Receive Signal (+ differential). |
| 13 | GND | GND | Ground. |
| 14 | XO | O | Crystal Feedback for 25 MHz crystal. This pin is a no connect if an oscillator or external clock source is used. |
| 15 | XI | I | Crystal/Oscillator/External Clock Input (25 MHz ±50 ppm). |
| 16 | REXT | I | Set PHY Transmit Output Current. Connect a 6.49 kΩ resistor to ground on this pin. |
| 17 | GND | GND | Ground. |
| 18 | MDIO | Ipu/ Opu | Management Interface (MII) Data I/O. This pin has a weak pull-up, is open-drain, and requires an external 1.0 kΩ pull-up resistor. |
| 19 | MDC | Ipu | Management Interface (MII) Clock Input. This clock pin is synchronous to the MDIO data pin. |
| 20 | RXD3/ PHYAD0 | Ipu/O | MII mode: MII Receive Data Output[3] (Note 2-2).<br>Config mode: The pull-up/pull-down value is latched as PHYADDR[0] at the de-assertion of reset. See the Strap-In Options section for details. |
| 21 | RXD2/ PHYAD1 | Ipd/O | MII Mode: MII Receive Data Output[2] (Note 2-2).<br>Config. Mode: The pull-up/pull-down value is latched as PHYADDR[1] at the de-assertion of reset. See the Strap-In Options section for details. |
| 22 | RXD1/ PHYAD2 | Ipd/O | MII Mode: MII Receive Data Output[1] (Note 2-2).<br>Config. Mode: The pull-up/pull-down value is latched as PHYADDR[2] at the de-assertion of reset. See the Strap-In Options section for details. |
| 23 | RXD0/ DUPLEX | Ipu/O | MII mode: MII Receive Data Output[0] (Note 2-2).<br>Config. Mode: The pull-up/pull-down value is latched as DUPLEX at the de-assertion of reset. See the Strap-In Options section for details. |

**TABLE 2-1: SIGNALS - KSZ8091MLX (CONTINUED)**

| Pin Number | Pin Name | Type Note 2-1 | Description |
|---|---|---|---|
| 24 | GND | GND | Ground. |
| 25 | VDDIO | P | 3.3V, 2.5V, or 1.8V digital $V_{DD}$. |
| 26 | NC | — | No Connect. This pin is not bonded and can be left floating. |
| 27 | RXDV/ CONFIG2 | Ipd/O | MII Mode: MII Receive Data Valid Output<br>Config. Mode: The pull-up/pull-down value is latched as CONFIG2 at the de-assertion of reset. See the Strap-In Options section for details. |
| 28 | RXC/ B-CAST_OFF | Ipd/O | MII mode: MII Receive Clock Output<br>Config mode: The pull-up/pull-down value is latched as B-CAST_OFF at the de-assertion of reset. See the Strap-In Options section for details. |
| 29 | RXER/ ISO | Ipd/O | MII Mode: MII Receive Error Output<br>Config. Mode: The pull-up/pull-down value is latched as ISOLATE at the de-assertion of reset. See the Strap-In Options section for details. |
| 30 | GND | GND | Ground. |
| 31 | VDD_1.2 | P | 1.2V core $V_{DD}$ (power supplied by KSZ8091MLX). Decouple with 0.1 µF capacitor to ground, and join with Pin 4 by power trace or plane. |
| 32 | INTRP/ PME_N2/ NAND_Tree# | Ipu/ Opu | Interrupt Output: Programmable interrupt output, with Register 1Bh as the Interrupt Control/Status register, for programming the interrupt conditions and reading the interrupt status. Register 1Fh, Bit [9] sets the interrupt output to active low (default) or active high.<br>PME_N Output: Programmable PME_N output (pin option 2). When asserted low, this pin signals that a WOL event has occurred.<br>Config. Mode: The pull-up/pull-down value is latched as NAND Tree# at the de-assertion of reset. See the Strap-In Options section for details.<br>This pin has a weak pull-up and is an open-drain.<br>For Interrupt (when active low) and PME functions, this pin requires an external 1.0 kΩ pull-up resistor to VDDIO (digital $V_{DD}$). |
| 33 | TXC/ PME_EN | Opd | MII Mode: MII Transmit Clock Output.<br>Config. Mode: The pull-up/pull-down value is latched as PME_EN at the de-assertion of reset. See the Strap-In Options section for details. |
| 34 | TXEN | I | MII Mode: MII Transmit Enable input |
| 35 | TXD0 | I | MII Mode: MII Transmit Data Input[0] (Note 2-3) |
| 36 | TXD1 | I | MII Mode: MII Transmit Data Input[1] (Note 2-3) |
| 37 | GND | GND | Ground. |
| 38 | TXD2 | I | MII Mode: MII Transmit Data Input[2] (Note 2-3) |
| 39 | TXD3 | I | MII Mode: MII Transmit Data Input[3] (Note 2-3) |
| 40 | COL/ CONFIG0 | Ipd/O | MII Mode: MII Collision Detect output<br>Config. Mode: The pull-up/pull-down value is latched as CONFIG0 at the de-assertion of reset. See the Strap-In Options section for details. |
| 41 | CRS/ CONFIG1 | Ipd/O | MII Mode: MII Carrier Sense output<br>Config. Mode: The pull-up/pull-down value is latched as CONFIG1 at the de-assertion of reset. See the Strap-In Options section for details. |

**TABLE 2-1: SIGNALS - KSZ8091MLX (CONTINUED)**

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-1</th><th colspan="3">Description</th></tr>
<tr><td rowspan="11">42</td><td rowspan="11">LED0/<br>PME_N1/<br>NWAYEN</td><td rowspan="11">Ipu/O</td><td colspan="3">LED Output: Programmable LED0 Output.<br>PME_N Output: Programmable PME_N Output (pin option 1)<br>In this mode, this pin has a weak pull-up, is an open-drain, and requires an external 1.0 kΩ pull-up resistor to VDDIO (digital $V_{DD}$).<br>Config. Mode: Latched as auto-negotiation enable (Register 0h, Bit [12]) at the de-assertion of reset. See the Strap-In Options section for details.<br>The LED0 pin is programmable using Register 1Fh, Bits [5:4], and is defined as follows.</td></tr>
<tr><td colspan="3">LED Mode = [00]</td></tr>
<tr><td>Link/Activity</td><td>Pin State</td><td>LED Definition</td></tr>
<tr><td>No Link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
<tr><td colspan="3">LED Mode = [01]</td></tr>
<tr><td>Link</td><td>Pin State</td><td>LED Definition</td></tr>
<tr><td>No Link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
<tr><td colspan="3">LED Mode = [10], [11]: Reserved</td></tr>
<tr><td rowspan="11">43</td><td rowspan="11">LED1/<br>SPEED</td><td rowspan="11">Ipu/O</td><td colspan="3">LED Output: Programmable LED1 output<br>Config. Mode: Latched as Speed (Register 0h, Bit [13]) at the de-assertion of reset.<br>See the Strap-In Options section for details.<br>The LED1 pin is programmable using Register 1Fh, Bits [5:4], and is defined as follows.</td></tr>
<tr><td colspan="3">LED Mode = [00]</td></tr>
<tr><td>Speed</td><td>Pin State</td><td>LED Definition</td></tr>
<tr><td>10BASE-T</td><td>High</td><td>OFF</td></tr>
<tr><td>100BASE-TX</td><td>Low</td><td>ON</td></tr>
<tr><td colspan="3">LED Mode = [01]</td></tr>
<tr><td>Activity</td><td>Pin State</td><td>LED Definition</td></tr>
<tr><td>No Activity</td><td>High</td><td>OFF</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
<tr><td colspan="3">LED Mode = [10], [11]: Reserved</td></tr>
</table>

**TABLE 2-1: SIGNALS - KSZ8091MLX (CONTINUED)**

| Pin Number | Pin Name | Type Note 2-1 | Description |
|---|---|---|---|
| 44 | TXER | Ipd | MII Mode: MII Transmit Error Input.<br>For EEE mode, this pin is driven by the EEE-MAC to put the KSZ8091MLX transmit into the LPI state.<br>For non-EEE mode, this pin is not defined for error transmission from MAC to KSZ8091MLX and can be left as a no connect.<br>For NAND_Tree mode, this pin should be pulled up by a pull-up resistor. |
| 45 | NC | — | No Connect. This pin is not bonded and can be left floating. |
| 46 | NC | — | No Connect. This pin is not bonded and can be left floating. |
| 47 | RST# | Ipu | Chip Reset (active-low). |
| 48 | NC | — | No Connect. This pin is not bonded and can be left floating. |

**Note 2-1** P = power supply
GND = ground
I = input
O = output
I/O = bi-directional
Ipu = Input with internal pull-up (see Electrical Characteristics for value).
Ipd = Input with internal pull-down (see Electrical Characteristics for value).
Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
Ipu/Opu = Input with internal pull-up (see Electrical Characteristics for value) and output with internal pull-up (see Electrical Characteristics for value).

**Note 2-2** MII RX Mode: The RXD[3:0] bits are synchronous with RXC. When RXDV is asserted, RXD[3:0] presents valid data to the MAC.

**Note 2-3** MII TX Mode: The TXD[3:0] bits are synchronous with TXC. When TXEN is asserted, TXD[3:0] presents valid data from the MAC.

## 2.1 Strap-In Options

The strap-in pins are latched at the de-assertion of reset. In some systems, the MAC MII receive input pins may drive high/low during power-up or reset, and consequently cause the PHY strap-in pins on the MII signals to be latched to unintended high/low states. In this case, external pull-ups (4.7 kΩ) or pull-downs (1.0 kΩ) should be added on these PHY strap-in pins to ensure that the intended values are strapped-in correctly.

**TABLE 2-2: STRAP-IN OPTIONS - KSZ8091MLX**

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type<br>Note 2-4</th><th colspan="2">Description</th></tr>
<tr><td>22</td><td>PHYAD2</td><td>Ipd/O</td><td colspan="2" rowspan="3">PHYAD[2:0] is latched at de-assertion of reset and is configurable to any value from 0 to 7 with PHY Address 1 as the default value.<br>PHY Address 0 is assigned by default as the broadcast PHY address, but it can be assigned as a unique PHY address after pulling the B-CAST_OFF strapping pin high or writing a ‘1’ to Register 16h, bit [9].<br>PHY Address bits [4:3] are set to 00 by default.</td></tr>
<tr><td>21</td><td>PHYAD1</td><td>Ipd/O</td></tr>
<tr><td>20</td><td>PHYAD0</td><td>Ipu/O</td></tr>
<tr><td>27</td><td>CONFIG2</td><td rowspan="4">Ipd/O</td><td colspan="2">The CONFIG[2:0] strap-in pins are latched at the de-assertion of reset.</td></tr>
<tr><td rowspan="2">41</td><td rowspan="2">CONFIG1</td><td>CONFIG[2:0]</td><td>Mode</td></tr>
<tr><td>000</td><td>MII (default)</td></tr>
<tr><td rowspan="2">40</td><td rowspan="2">CONFIG0</td><td>110</td><td>MII back-to-back</td></tr>
<tr><td>001 – 101, 111</td><td>Reserved, not used</td></tr>
<tr><td>33</td><td>PME_EN</td><td>Ipd/O</td><td colspan="2">PME output for Wake-on-LAN<br>Pull-up = Enable<br>Pull-down (default) = Disable<br>At the de-assertion of reset, this pin value is latched into Register 16h, bit [15].</td></tr>
<tr><td>29</td><td>ISO</td><td>Ipd/O</td><td colspan="2">Isolate mode<br>Pull-up = Enable<br>Pull-down (default) = Disable<br>At the de-assertion of reset, this pin value is latched into Register 0h, bit [10].</td></tr>
<tr><td>43</td><td>SPEED</td><td>Ipu/O</td><td colspan="2">Speed Mode:<br>Pull-up (default) = 100 Mbps<br>Pull-down = 10 Mbps<br>At the de-assertion of reset, this pin value is latched into Register 0h, Bit [13] as the speed select, and also is latched into Register 4h (Auto-Negotiation advertisement) as the speed capability support.</td></tr>
<tr><td>23</td><td>DUPLEX</td><td>Ipu/O</td><td colspan="2">Duplex Mode:<br>Pull-up (default) = Half-duplex<br>Pull-down = Full-duplex<br>At the de-assertion of reset, this pin value is latched into Register 0h, Bit [8].</td></tr>
<tr><td>42</td><td>NWAYEN</td><td>Ipu/O</td><td colspan="2">Nway Auto-Negotiation Enable:<br>Pull-up (default) = Enable auto-negotiation<br>Pull-down = Disable auto-negotiation<br>At the de-assertion of reset, this pin value is latched into Register 0h, Bit [12].</td></tr>
<tr><td>28</td><td>B-CAST_OFF</td><td>Ipd/O</td><td colspan="2">Broadcast Off – for PHY Address 0:<br>Pull-up = PHY Address 0 is set as an unique PHY address<br>Pull-down (default) = PHY Address 0 is set as a broadcast PHY address<br>At the de-assertion of reset, this pin value is latched by the chip.</td></tr>
</table>

**TABLE 2-2: STRAP-IN OPTIONS - KSZ8091MLX (CONTINUED)**

| Pin Number | Pin Name | Type Note 2-4 | Description |
|---|---|---|---|
| 32 | NAND_Tree# | Ipu/Opu | NAND Tree Mode:<br>Pull-up (default) = Disable<br>Pull-down = Enable<br>At the de-assertion of reset, this pin value is latched by the chip. |

**Note 2-4** Ipu/O = Input with internal pull-up during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down during power-up/reset; output pin otherwise.
Ipu/Opu = Input with internal pull-up and output with internal pull-up.

## 3.0 FUNCTIONAL DESCRIPTION

The KSZ8091MLX is an integrated single 3.3V supply Fast Ethernet transceiver. It is fully compliant with the IEEE 802.3 Specification, and reduces board cost and simplifies board layout by using on-chip termination resistors for the two differential pairs and by integrating the regulator to supply the 1.2V core.

On the copper media side, the KSZ8091MLX supports 10BASE-T and 100BASE-TX for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable, and HP Auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables.

On the MAC processor side, the KSZ8091MLX offers the Media Independent Interface (MII) for direct connection with MII compliant Ethernet MAC processors and switches, respectively.

The MII management bus option gives the MAC processor complete access to the KSZ8091MLX control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status change.

### 3.1 10BASE-T/100BASE-TX Transceiver

#### 3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B encoding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding and followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 6.49 kΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

#### 3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC-restoration and data-conversion block. The DC-restoration circuit compensates for the effect of baseline wander and improves the dynamic range. The differential data-conversion circuit converts MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock-recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal to NRZ format. This signal is sent through the de-scrambler, then the 4B/5B decoder. Finally, the NRZ serial data is converted to MII format and provided as the input data to the MAC.

#### 3.1.3 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The scrambler spreads the power spectrum of the transmitted signal to reduce electromagnetic interference (EMI) and baseline wander. The de-scrambler recovers the scrambled signal.

#### 3.1.4 10BASE-T TRANSMIT

The 10BASE-T drivers are incorporated with the 100BASE-TX drivers to allow for transmission using the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output 10BASE-T signals with typical amplitude of 2.5V peak for standard 10BASE-T mode and 1.75V peak for energy-efficient 10BASE-Te mode. The 10BASE-T/10BASE-Te signals have harmonic contents that are at least 27 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

### 3.1.5 10BASE-T RECEIVE

On the receive side, input buffer and level detecting squelch circuits are used. A differential input receiver circuit and a phase-locked loop (PLL) performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV, or with short pulse widths, to prevent noise at the RXP and RXM inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8091MLX decodes a data frame. The receive clock is kept active during idle periods between data receptions.

### 3.1.6 SQE AND JABBER FUNCTION (10BASE-T ONLY)

In 10BASE-T operation, a short pulse is put out on the COL pin after each frame is transmitted. This SQE test is needed to test the 10BASE-T transmit/receive path. If transmit enable (TXEN) is high for more than 20 ms (jabbering), the 10BASE-T transmitter is disabled and COL is asserted high. If TXEN is then driven low for more than 250 ms, the 10BASE-T transmitter is re-enabled and COL is de-asserted (returns to low).

### 3.1.7 PLL CLOCK SYNTHESIZER

The KSZ8091MLX generates all internal clocks and all external clocks for system timing from an external 25 MHz crystal, oscillator, or reference clock.

### 3.1.8 AUTO-NEGOTIATION

The KSZ8091MLX conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest priority.

- Priority 1: 100BASE-TX, full-duplex
- Priority 2: 100BASE-TX, half-duplex
- Priority 3: 10BASE-T, full-duplex
- Priority 4: 10BASE-T, half-duplex

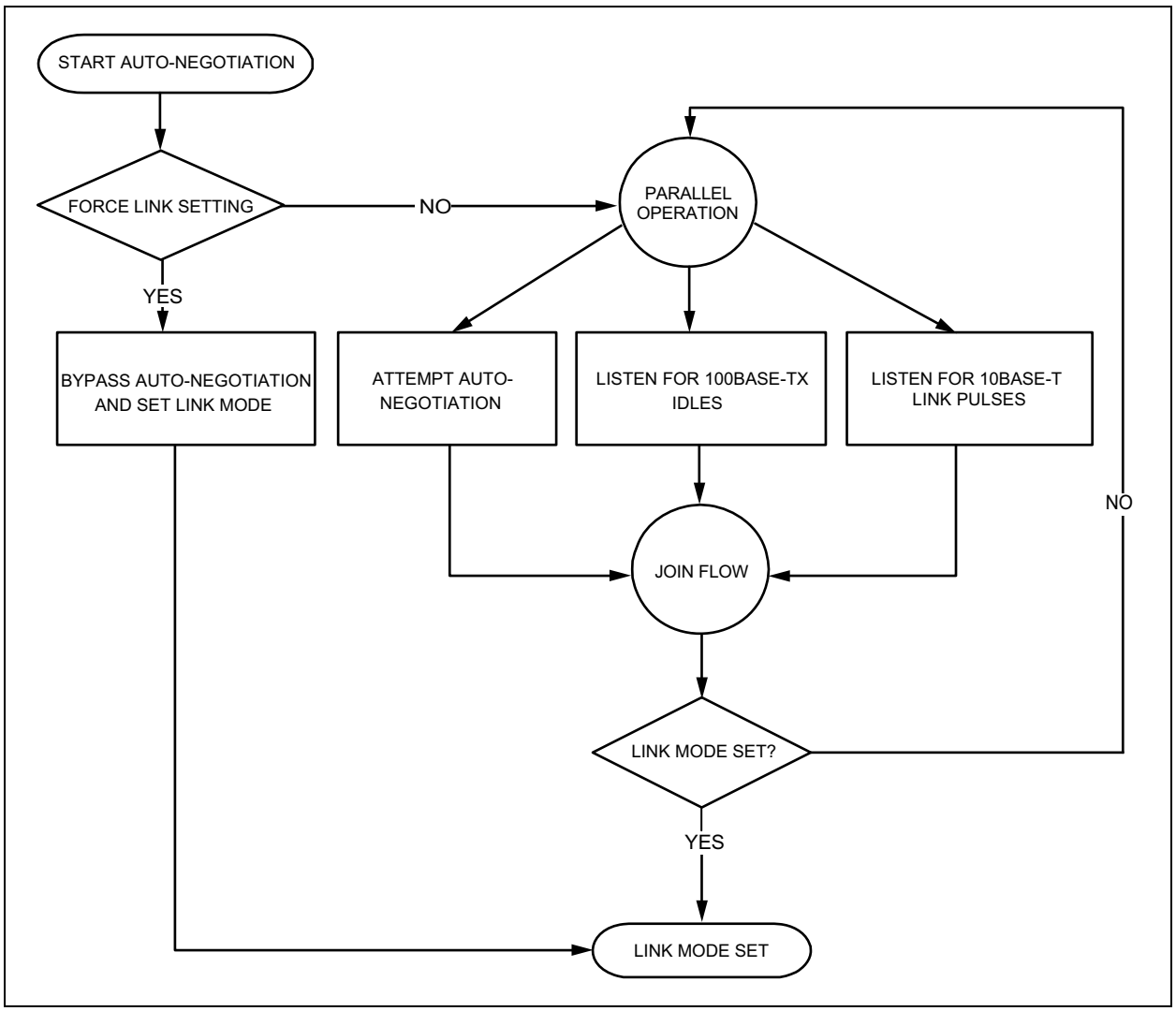
If auto-negotiation is not supported or the KSZ8091MLX link partner is forced to bypass auto-negotiation, then the KSZ8091MLX sets its operating mode by observing the signal at its receiver. This is known as parallel detection, which allows the KSZ8091MLX to establish a link by listening for a fixed signal protocol in the absence of the auto-negotiation advertisement protocol.

Auto-negotiation is enabled by either hardware pin strapping (NWAYEN, Pin 42) or software (Register 0h, Bit [12]).

By default, auto-negotiation is enabled after power-up or hardware reset. After that, auto-negotiation can be enabled or disabled by Register 0h, Bit [12]. If auto-negotiation is disabled, the speed is set by Register 0h, Bit [13], and the duplex is set by Register 0h, Bit [8].

The auto-negotiation link-up process is shown in Figure 3-1.

**FIGURE 3-1: AUTO-NEGOTIATION FLOW CHART**




## 3.2 MII Data Interface

The Media Independent Interface (MII) is compliant with the IEEE 802.3 Specification. It provides a common interface between MII PHYs and MACs, and has the following key characteristics:

- Pin count is 16 pins (7 pins for data transmission, 7 pins for data reception, and 2 pins for carrier and collision indication).
- 10 Mbps and 100 Mbps data rates are supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 4 bits wide, a nibble.

By default, the KSZ8091MLX is configured to MII mode after it is powered up or hardware reset with the following:

- A 25 MHz crystal connected to XI, XO (pins 15, 14), or an external 25 MHz clock source (oscillator) connected to XI.
- The CONFIG[2:0] strap-in pins (pins 27, 41, 40) set to 000 (default setting).

### 3.2.1 MII SIGNAL DEFINITION

Table 3-1 describes the MII signals. Refer to Clause 22 of the IEEE 802.3 Specification for detailed information.

**TABLE 3-1: MII SIGNAL DEFINITION**

| MII Signal Name | Direction with Respect to PHY, KSZ8091MLX Signal | Direction with Respect to MAC | Description |
|---|---|---|---|
| TXC | Output | Input | Transmit Clock<br>(2.5 MHz for 10 Mbps; 25 MHz for 100 Mbps) |
| TXEN | Input | Output | Transmit Enable |
| TXD[3:0] | Input | Output | Transmit Data[3:0] |
| TXER | Input | Output or not implemented | Transmit Error<br>(KSZ8091MLX implements only the EEE function for this pin. See Transmit Error (TXER) for details.) |
| RXC | Output | Input | Receive Clock<br>(2.5 MHz for 10 Mbps; 25 MHz for 100 Mbps) |
| RXDV | Output | Input | Receive Data Valid |
| RXD[3:0] | Output | Input | Receive Data[3:0] |
| RXER | Output | Input or not required | Receive Error |
| CRS | Output | Input | Carrier Sense |
| COL | Output | Input | Collision Detection |

#### 3.2.1.1 Transmit Clock (TXC)

TXC is sourced by the PHY. It is a continuous clock that provides the timing reference for TXEN, TXD[3:0], and TXER.

TXC is 2.5 MHz for 10 Mbps operation and 25 MHz for 100 Mbps operation.

#### 3.2.1.2 Transmit Enable (TXEN)

TXEN indicates that the MAC is presenting nibbles on TXD[3:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented on the MII. It is negated before the first TXC following the final nibble of a frame.

TXEN transitions synchronously with respect to TXC.

#### 3.2.1.3 Transmit Data[3:0] (TXD[3:0])

When TXEN is asserted, TXD[3:0] are the data nibbles presented by the MAC and accepted by the PHY for transmission.

When TXEN is de-asserted, the MAC drives TXD[3:0] to either 0000 for the idle state (non-EEE mode) or 0001 for the LPI state (EEE mode).

TXD[3:0] transitions synchronously with respect to TXC.

#### 3.2.1.4 Transmit Error (TXER)

TXER is implemented only for the EEE function.

For EEE mode, this pin is driven by the EEE-MAC to put the KSZ8091MLX transmit into the LPI state.

For non-EEE mode, this pin is not defined for error transmission from MAC to KSZ8091MLX and can be left as a no connect.

TXER transitions synchronously with respect to TXC.

#### 3.2.1.5 Receive Clock (RXC)

RXC provides the timing reference for RXDV, RXD[3:0], and RXER.

In 10 Mbps mode, RXC is recovered from the line while the carrier is active. When the line is idle or the link is down, RXC is derived from the PHY's reference clock.

In 100 Mbps mode, RXC is continuously recovered from the line. If the link is down, RXC is derived from the PHY's reference clock.

RXC is 2.5 MHz for 10 Mbps operation and 25 MHz for 100 Mbps operation.

#### 3.2.1.6 Receive Data Valid (RXDV)

RXDV is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on RXD[3:0].

In 10 Mbps mode, RXDV is asserted with the first nibble of the start-of-frame delimiter (SFD), 5D, and remains asserted until the end of the frame.

In 100 Mbps mode, RXDV is asserted from the first nibble of the preamble to the last nibble of the frame.

RXDV transitions synchronously with respect to RXC.

#### 3.2.1.7 Receive Data[3:0] (RXD[3:0])

For each clock period in which RXDV is asserted, RXD[3:0] transfers a nibble of recovered data from the PHY.

When RXDV is de-asserted, the PHY drives RXD[3:0] to either 0000 for the idle state (non-EEE mode) or 0001 for the LPI state (EEE mode).

RXD[3:0] transitions synchronously with respect to RXC.

#### 3.2.1.8 Receive Error (RXER)

When RXDV is asserted, RXER is asserted for one or more RXC periods to indicate that a symbol error (for example, a coding error that a PHY can detect that may otherwise be undetectable by the MAC sub-layer) is detected somewhere in the frame that is being transferred from the PHY to the MAC.

In EEE mode only, when RXDV is de-asserted, RXER is driven by the PHY to inform the MAC that the KSZ8091MLX receive is in the LPI state.

RXER transitions synchronously with respect to RXC.

#### 3.2.1.9 Carrier Sense (CRS)

CRS is asserted and de-asserted as follows:

- In 10 Mbps mode, CRS assertion is based on the reception of valid preambles. CRS de-assertion is based on the reception of an end-of-frame (EOF) marker.
- In 100 Mbps mode, CRS is asserted when a start-of-stream delimiter or /J/K symbol pair is detected. CRS is de-asserted when an end-of-stream delimiter or /T/R symbol pair is detected. Additionally, the PMA layer de-asserts CRS if IDLE symbols are received without /T/R.

#### 3.2.1.10 Collision Detection (COL)

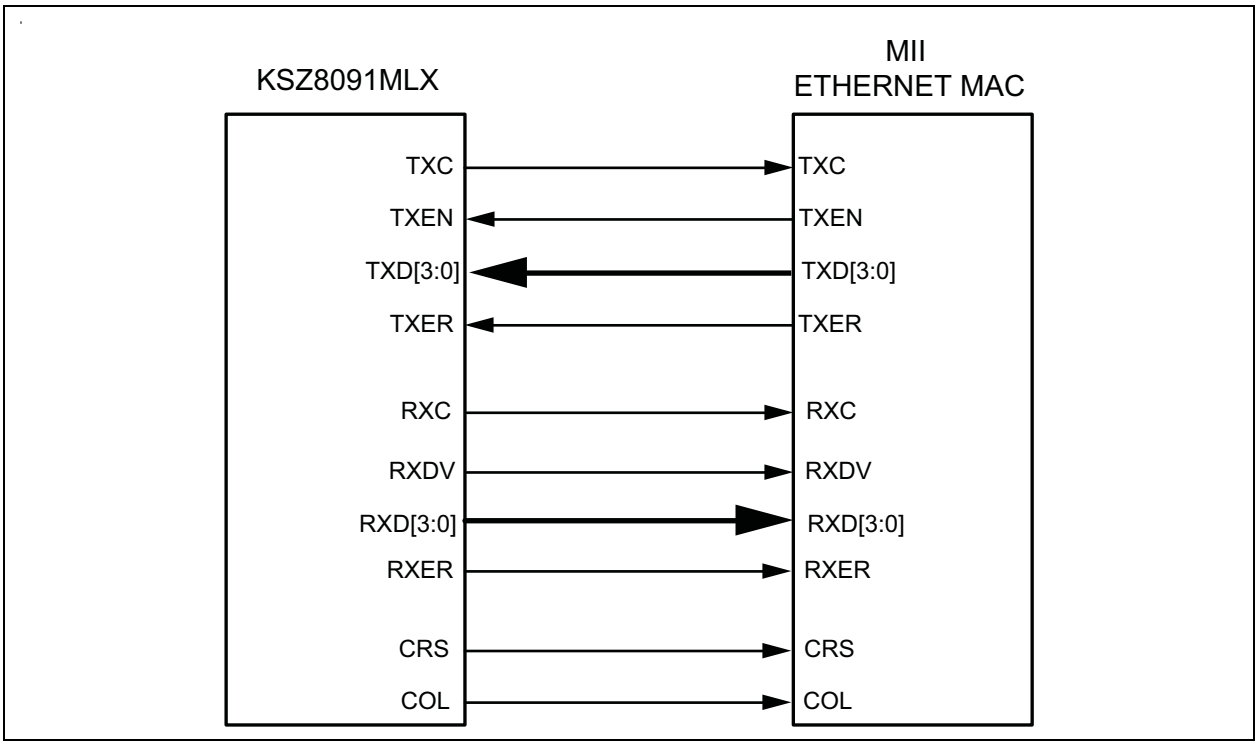
COL is asserted in half-duplex mode whenever the transmitter and receiver are simultaneously active on the line. This informs the MAC that a collision has occurred during its transmission to the PHY.

COL transitions asynchronously with respect to TXC and RXC.

### 3.2.2 MII SIGNAL DIAGRAM

The KSZ8091MLX MII pin connections to the MAC are shown in Figure 3-2.

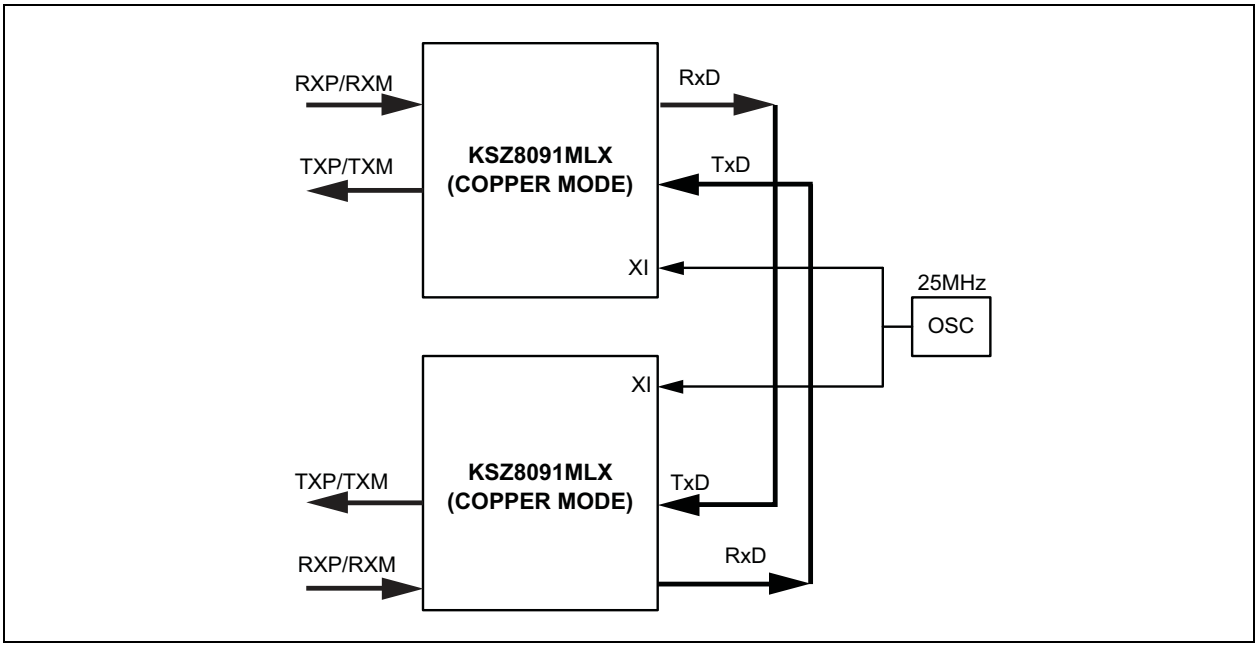
**FIGURE 3-2: KSZ8091MLX MII INTERFACE**



## 3.3 Back-to-Back Mode – 100 Mbps Copper Repeater

Two KSZ8091MLX devices can be connected back-to-back to form a 100BASE-TX copper repeater.

**FIGURE 3-3: KSZ8091MLX TO KSZ8091MLX BACK-TO-BACK COPPER REPEATER**




### 3.3.1 MII BACK-TO-BACK MODE

In MII back-to-back mode, a KSZ8091MLX interfaces with another KSZ8091MLX to provide a complete 100 Mbps copper repeater solution.

The KSZ8091MLX devices are configured to MII back-to-back mode after power-up or reset with the following:

- Strap-in pin CONFIG[2:0] (pins 27, 41, 40) set to 110.
- A common 25 MHz reference clock connected to XI (Pin 15) of both KSZ8091MLX devices.
- MII signals connected as shown in Table 3-2.

**TABLE 3-2: MII SIGNAL CONNECTION FOR MII BACK-TO-BACK MODE (100BASE-TX COPPER REPEATER)**

| KSZ8091MLX (100BASE-TX Copper) [Device 1] | | | KSZ8091MLX (100BASE-TX Copper) [Device 2] | | |
|---|---|---|---|---|---|
| **Pin Name** | **Pin Number** | **Pin Type** | **Pin Name** | **Pin Number** | **Pin Type** |
| RXDV | 27 | Output | TXEN | 34 | Input |
| RXD3 | 20 | Output | TXD3 | 39 | Input |
| RXD2 | 21 | Output | TXD2 | 38 | Input |
| RXD1 | 22 | Output | TXD1 | 36 | Input |
| RXD0 | 23 | Output | TXD0 | 35 | Input |
| TXEN | 34 | Input | RXDV | 27 | Output |
| TXD3 | 39 | Input | RXD3 | 20 | Output |
| TXD2 | 38 | Input | RXD2 | 21 | Output |
| TXD1 | 36 | Input | RXD1 | 22 | Output |
| TXD0 | 35 | Input | RXD0 | 23 | Output |

## 3.4 MII Management (MIIM) Interface

The KSZ8091MLX supports the IEEE 802.3 MII management interface, also known as the Management Data Input/Output (MDIO) interface. This interface allows an upper-layer device, such as a MAC processor, to monitor and control the state of the KSZ8091MLX. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. More details about the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the physical connection mentioned earlier, which allows the external controller to communicate with one or more PHY devices.
- A 32-register address space for direct access to IEEE-defined registers and vendor-specific registers, and for indirect access to MMD addresses and registers. See the Register Descriptions section.

As the default, the KSZ8091MLX supports unique PHY Addresses 1 to 7, and broadcast PHY Address 0. The latter is defined in the IEEE 802.3 Specification, and can be used to read/write to a single KSZ8091MLX device, or write to multiple KSZ8091MLX devices simultaneously.

PHY Address 0 can optionally be disabled as the broadcast address by either hardware pin strapping (B-CAST_OFF, Pin 28) or software (Register 16h, Bit [9]), and assigned as a unique PHY address.

The PHYAD[2:0] strapping pins are used to assign a unique PHY address between 0 and 7 to each KSZ8091MLX device.

The MIIM interface can operates up to a maximum clock speed of 10 MHz MAC clock.

Table 3-3 shows the MII management frame format for the KSZ8091MLX.

**TABLE 3-3: MII MANAGEMENT FRAME FORMAT FOR THE KSZ8091MLX**

| | Preamble | Start of Frame | Read/ Write OP Code | PHY Address Bits[4:0] | REG Address Bits[4:0] | TA | Data Bits[15:0] | Idle |
|---|---|---|---|---|---|---|---|---|
| **Read** | 32 1's | 01 | 10 | 00AAA | RRRRR | Z0 | DDDDDDDD_DDDDDDDD | Z |
| **Write** | 32 1's | 01 | 01 | 00AAA | RRRRR | 10 | DDDDDDDD_DDDDDDDD | Z |

## 3.5 Interrupt (INTRP)

INTRP (Pin 32) is an optional interrupt signal that is used to inform the external controller that there has been a status update to the KSZ8091MLX PHY Register. Bits [15:8] of Register 1Bh are the interrupt control bits to enable and disable the conditions for asserting the INTRP signal. Bits [7:0] of Register 1Bh are the interrupt status bits to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading Register 1Bh.

Bit [9] of Register 1Fh sets the interrupt level to active high or active low. The default is active low.

The MII management bus option gives the MAC processor complete access to the KSZ8091MLX control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll the PHY for status change.

## 3.6 HP Auto MDI/MDI-X

HP Auto MDI/MDI-X configuration eliminates the need to decide whether to use a straight cable or a crossover cable between the KSZ8091MLX and its link partner. This feature allows the KSZ8091MLX to use either type of cable to connect with a link partner that is in either MDI or MDI-X mode. The auto-sense function detects transmit and receive pairs from the link partner and assigns transmit and receive pairs to the KSZ8091MLX accordingly.

HP Auto MDI/MDI-X is enabled by default. It is disabled by writing a '1' to Register 1Fh, Bit [13]. MDI and MDI-X mode is selected by Register 1Fh, Bit [14] if HP Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

Table 3-4 shows how the IEEE 802.3 Standard defines MDI and MDI-X.

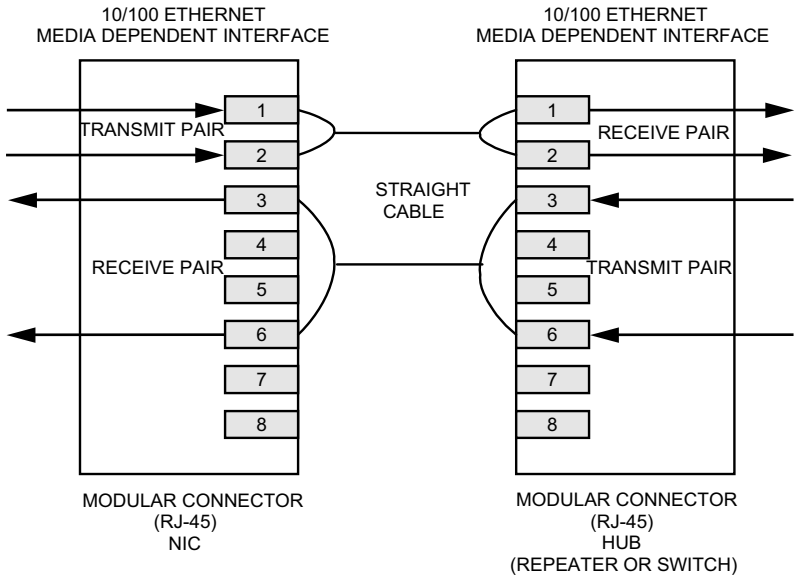
**TABLE 3-4: MDI/MDI-X PIN DESCRIPTION**

| MDI | | MDI-X | |
|---|---|---|---|
| **RJ-45 Pin** | **Signal** | **RJ-45 Pin** | **Signal** |
| 1 | TX+ | 1 | RX+ |
| 2 | TX– | 2 | RX– |
| 3 | RX+ | 3 | TX+ |
| 6 | RX– | 6 | TX– |

### 3.6.1 STRAIGHT CABLE

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 3-4 shows a typical straight cable connection between a NIC card (MDI device) and a switch or hub (MDI-X device).

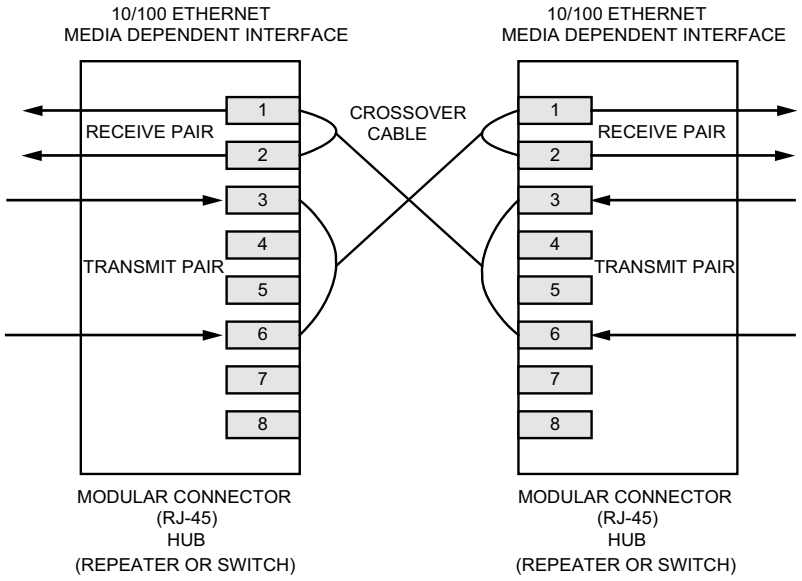
**FIGURE 3-4: TYPICAL STRAIGHT CABLE CONNECTION**




### 3.6.2 CROSSOVER CABLE

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 3-5 shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

**FIGURE 3-5: TYPICAL CROSSOVER CABLE CONNECTION**




## 3.7 Loopback Mode

The KSZ8091MLX supports the following loopback operations to verify analog and/or digital data paths.

- Local (digital) loopback
- Remote (analog) loopback

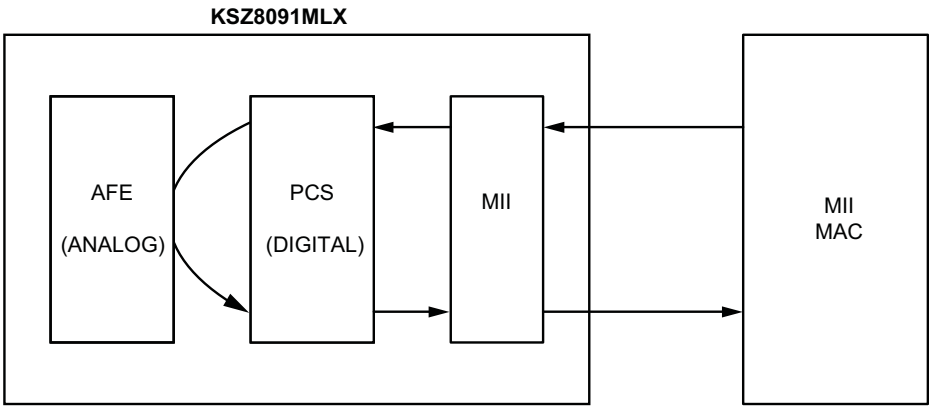
### 3.7.1 LOCAL (DIGITAL) LOOPBACK

This loopback mode checks the MII/RMII transmit and receive data paths between the KSZ8091MLX and the external MAC, and is supported for both speeds (10/100 Mbps) at full-duplex.

The loopback data path is shown in Figure 3-6.

1. The MII MAC transmits frames to the KSZ8091MLX.
2. Frames are wrapped around inside the KSZ8091MLX.
3. The KSZ8091MLX transmits frames back to the MII MAC.

**FIGURE 3-6: LOCAL (DIGITAL) LOOPBACK**



The following programming action and register settings are used for local loopback mode:

For 10/100 Mbps loopback:

Set Register 0h,

Bit [14] = 1 // Enable local loopback mode

Bit [13] = 0/1 // Select 10 Mbps/100 Mbps speed

Bit [12] = 0 // Disable auto-negotiation

Bit [8] = 1 // Select full-duplex mode

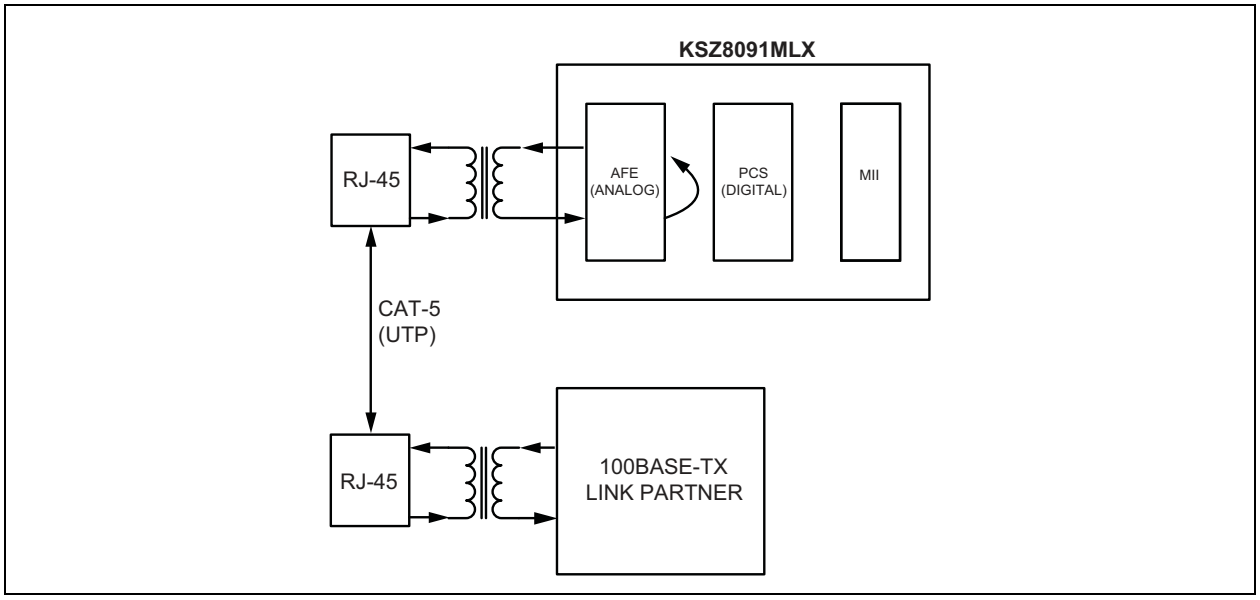
### 3.7.2 REMOTE (ANALOG) LOOPBACK

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between the KSZ8091MLX and its link partner, and is supported for 100BASE-TX full-duplex mode only.

The loopback data path is shown in Figure 3-7.

1. The Fast Ethernet (100BASE-TX) PHY link partner transmits frames to the KSZ8091MLX.
2. Frames are wrapped around inside the KSZ8091MLX.
3. The KSZ8091MLX transmits frames back to the Fast Ethernet (100BASE-TX) PHY link partner.

**FIGURE 3-7: REMOTE (ANALOG) LOOPBACK**




The following programming steps and register settings are used for remote loopback mode:

1. Set Register 0h,

Bits [13] = 1 // Select 100 Mbps speed

Bit [12] = 0 // Disable auto-negotiation

Bit [8] = 1 // Select full-duplex mode

Or just auto-negotiate and link up at 100BASE-TX full-duplex mode with the link partner.

2. Set Register 1Fh,

Bit [2] = 1 // Enable remote loopback mode

## 3.8 LinkMD® Cable Diagnostic

The LinkMD function uses time-domain reflectometry (TDR) to analyze the cabling plant for common cabling problems. These include open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI or MDI-X pair, then analyzing the shape of the reflected signal to determine the type of fault. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

LinkMD is initiated by accessing register 1Dh, the LinkMD Cable Diagnostic register, in conjunction with Register 1Fh, the PHY Control 2 Register. The latter register is used to disable Auto MDI/MDI-X and to select either MDI or MDI-X as the cable differential pair for testing.

### 3.8.1 USAGE

The following is a sample procedure for using LinkMD with Registers 1Dh and 1Fh:

1. Disable auto MDI/MDI-X by writing a ‘1’ to Register 1Fh, bit [13].
2. Start cable diagnostic test by writing a ‘1’ to Register 1Dh, bit [15]. This enable bit is self-clearing.
3. Wait (poll) for Register 1Dh, bit [15] to return a ‘0’, and indicating cable diagnostic test is completed.
4. Read cable diagnostic test results in Register 1Dh, bits [14:13]. The results are as follows:

   00 = normal condition (valid test)

   01 = open condition detected in cable (valid test)

   10 = short condition detected in cable (valid test)

   11 = cable diagnostic test failed (invalid test)

The ‘11’ case, invalid test, occurs when the device is unable to shut down the link partner. In this instance, the test is not run because it would be impossible for the device to determine if the detected signal is a reflection of the signal generated or a signal from another source.

5. Get distance to fault by concatenating Register 1Dh, bits [8:0] and multiplying the result by a constant of 0.38. The distance to the cable fault can be determined by the following formula:

**EQUATION 3-1:**

$$D(Distance \text{ to cable fault in meters}) = 0.38 \times (Register \text{ 1Dh, bits[8:0]})$$

Concatenated value of Registers 1Dh bits [8:0] should be converted to decimal before multiplying by 0.38.

The constant (0.38) may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

## 3.9 NAND Tree Support

The KSZ8091MLX provides parametric NAND tree support for fault detection between chip I/Os and board. The NAND tree is a chain of nested NAND gates in which each KSZ8091MLX digital I/O (NAND tree input) pin is an input to one NAND gate along the chain. At the end of the chain, the CRS pin provides the output for the nested NAND gates.

The NAND tree test process includes:

- Enabling NAND tree mode
- Pulling all NAND tree input pins high
- Driving each NAND tree input pin low, sequentially, according to the NAND tree pin order
- Checking the NAND tree output to make sure there is a toggle high-to-low or low-to-high for each NAND tree input driven low

Table 3-5 lists the NAND tree pin order.

**TABLE 3-5: NAND TREE TEST PIN ORDER FOR KSZ8091MLX**

| Pin Number | Pin Name | NAND Tree Description |
|---|---|---|
| 18 | MDIO | Input |
| 19 | MDC | Input |
| 20 | RXD3 | Input |
| 21 | RXD2 | Input |
| 22 | RXD1 | Input |
| 23 | RXD0 | Input |
| 27 | RXDV | Input |
| 28 | RXC | Input |
| 29 | RXER | Input |
| 32 | INTRP | Input |
| 33 | TXC | Input |
| 34 | TXEN | Input |
| 35 | TXD0 | Input |
| 36 | TXD1 | Input |
| 38 | TXD2 | Input |
| 39 | TXD3 | Input |
| 42 | LED0 | Input |
| 43 | LED1 | Input |
| 40 | COL | Input |
| 41 | CRS | Output |

### 3.9.1 NAND TREE I/O TESTING

Use the following procedure to check for faults on the KSZ8091MLX digital I/O pin connections to the board:

1. Enable NAND tree mode using either a hardware strap-in pin (NAND_Tree#, Pin 32) or software (Register 16h, Bit [5]). TXER, pin 44, also needs to be pulled up by a pull-up resistor.
2. Use board logic to drive all KSZ8091MLX NAND tree input pins high.
3. Use board logic to drive each NAND tree input pin, in KSZ8091MLX NAND tree pin order, as follows:
   a) Toggle the first pin (MDIO) from high to low, and verify that the CRS pin switches from high to low to indicate that the first pin is connected properly.
   b) Leave the first pin (MDIO) low.
   c) Toggle the second pin (MDC) from high to low, and verify that the CRS pin switches from low to high to indicate that the second pin is connected properly.
   d) Leave the first pin (MDIO) and the second pin (MDC) low.
   e) Toggle the third pin (RXD3) from high to low, and verify that the CRS pin switches from high to low to indicate that the third pin is connected properly.
   f) Continue with this sequence until all KSZ8091MLX NAND tree input pins have been toggled.

Each KSZ8091MLX NAND tree input pin must cause the CRS output pin to toggle high-to-low or low-to-high to indicate a good connection. If the CRS pin fails to toggle when the KSZ8091MLX input pin toggles from high to low, the input pin has a fault.

## 3.10 Power Management

The KSZ8091MLX incorporates a number of power-management modes and features that provide methods to consume less energy. These are discussed in the following sections.

### 3.10.1 POWER-SAVING MODE

Power-saving mode is used to reduce the transceiver power consumption when the cable is unplugged. It is enabled by writing a ‘1’ to Register 1Fh, bit [10], and is in effect when auto-negotiation mode is enabled and the cable is disconnected (no link).

In this mode, the KSZ8091MLX shuts down all transceiver blocks, except for the transmitter, energy detect, and PLL circuits.

By default, power-saving mode is disabled after power-up.

### 3.10.2 ENERGY-DETECT POWER-DOWN MODE

Energy-detect power-down (EDPD) mode is used to further reduce transceiver power consumption when the cable is unplugged. It is enabled by writing a ‘0’ to Register 18h, bit [11], and is in effect when auto-negotiation mode is enabled and the cable is disconnected (no link).

EDPD mode works with the PLL off (set by writing a ‘1’ to Register 10h, bit [4] to automatically turn the PLL off in EDPD mode) to turn off all KSZ8091MLX transceiver blocks except the transmitter and energy-detect circuits.

Power can be reduced further by extending the time interval between transmissions of link pulses to check for the presence of a link partner. The periodic transmission of link pulses is needed to ensure the KSZ8091MLX and its link partner, when operating in the same low-power state and with Auto MDI/MDI-X disabled, can wake up when the cable is connected between them.

By default, energy-detect power-down mode is disabled after power-up.

### 3.10.3 POWER-DOWN MODE

Power-down mode is used to power down the KSZ8091MLX device when it is not in use after power-up. It is enabled by writing a ‘1’ to Register 0h, bit [11].

In this mode, the KSZ8091MLX disables all internal functions except the MII management interface. The KSZ8091MLX exits (disables) power-down mode after Register 0h, bit [11] is set back to ‘0’.

### 3.10.4 SLOW-OSCILLATOR MODE

Slow-oscillator mode is used to disconnect the input reference crystal/clock on XI (pin 15) and select the on-chip slow oscillator when the KSZ8091MLX device is not in use after power-up. It is enabled by writing a ‘1’ to Register 11h, bit [5].

Slow-oscillator mode works in conjunction with power-down mode to put the KSZ8091MLX device in the lowest power state, with all internal functions disabled except the MII management interface. To properly exit this mode and return to normal PHY operation, use the following programming sequence:

1. Disable slow-oscillator mode by writing a ‘0’ to Register 11h, Bit [5].
2. Disable power-down mode by writing a ‘0’ to Register 0h, Bit [11].
3. Initiate software reset by writing a ‘1’ to Register 0h, Bit [15].

## 3.11 Energy Efficient Ethernet (EEE)

The KSZ8091MLX implements Energy Efficient Ethernet (EEE) for the Media Independent Interface (MII) as described in IEEE Standard 802.3az. The Standard is defined around an EEE-compliant MAC on the host side and an EEE-compliant link partner on the line side that support special signaling associated with EEE. EEE saves power by keeping the AC signal on the copper Ethernet cable at approximately 0V peak-to-peak as often as possible during periods of no traffic activity, while maintaining the link-up status. This is referred to as low-power idle (LPI) mode or state.

During LPI mode, the copper link responds automatically when it receives traffic and resumes normal PHY operation immediately, without blockage of traffic or loss of packet. This involves exiting LPI mode and returning to normal 100 Mbps operating mode. Wake-up time is <30 µs for 100BASE-TX.

The LPI state is controlled independently for transmit and receive paths, allowing the LPI state to be active (enabled) for:

- Transmit cable path only
- Receive cable path only
- Both transmit and receive cable paths

The KSZ8091MLX has the EEE function disabled as the power-up default setting. To enable the EEE function for 100 Mbps mode, use the following programming sequence:

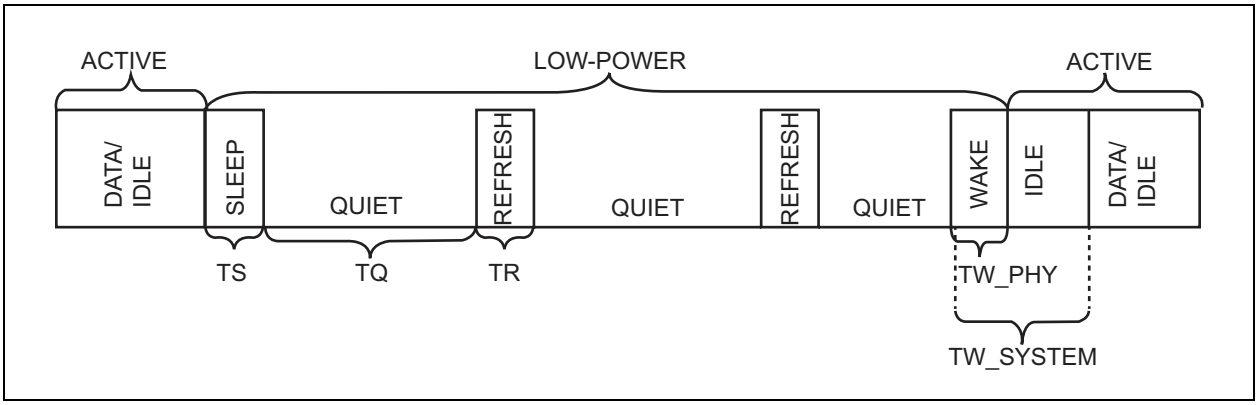
1. Enable 100 Mbps EEE mode advertisement by writing a ‘1’ to MMD address 7h, Register 3Ch, bit [1].

2. Restart auto-negotiation by writing a ‘1’ to standard Register 0h, bit [9].

For standard (non-EEE) 10BASE-T mode, normal link pulses (NLPs) with long periods of no AC signal transmission are used to maintain the link during the idle period when there is no traffic activity. To save more power, the KSZ8091MLX provides the option to enable 10BASE-Te mode, which saves additional power by reducing the transmitted signal amplitude from 2.5V to 1.75V. To enable 10BASE-Te mode, write a ‘1’ to standard Register 13h, Bit [4] and write a ‘0’ to MMD Address 1Ch, Register 4h, Bit [13].

During LPI mode, refresh transmissions are used to maintain the link; power savings occur in quiet periods. Approximately every 20 to 22 milliseconds, a refresh transmission of 200 to 220 microseconds is sent to the link partner. The refresh transmissions and quiet periods are shown in Figure 3-8.

**FIGURE 3-8: LPI MODE (REFRESH TRANSMISSIONS AND QUIET PERIODS)**



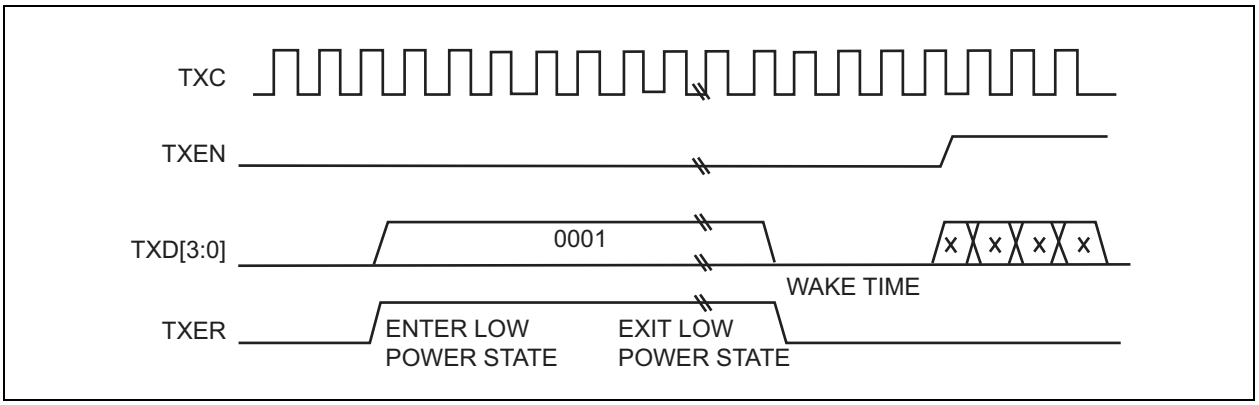

### 3.11.1 TRANSMIT DIRECTION CONTROL (MAC-TO-PHY)

The KSZ8091MLX enters LPI mode for the transmit direction when its attached EEE-compliant MII MAC de-asserts TXEN, asserts TXER, and sets TXD[3:0] to 0001. The KSZ8091MLX remains in the LPI transmit state while the MAC maintains the states of these signals. When the MAC changes any of the TXEN, TXER, or TX data signals from their LPI state values, the KSZ8091MLX exits the LPI transmit state.

The TXC clock is not stopped, because it is sourced from the PHY and is used by the MAC for MII transmit.

Figure 3-9 shows the LPI transition for MII (100 Mbps) transmit.

**FIGURE 3-9: LPI TRANSITION - MII (100 MBPS) TRANSMIT**




### 3.11.2 RECEIVE DIRECTION CONTROL (PHY-TO-MAC)

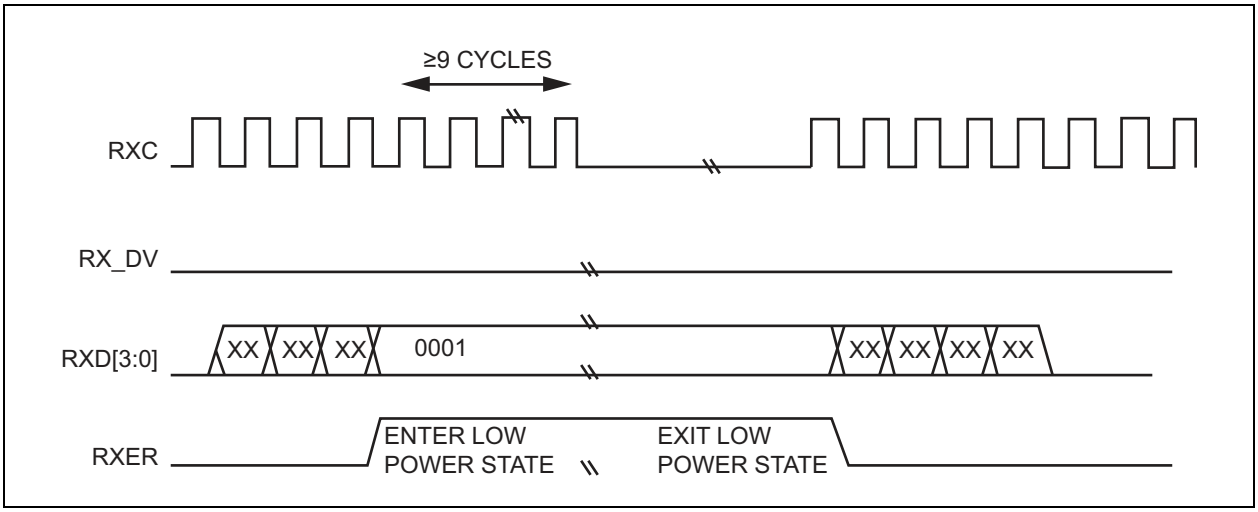
The KSZ8091MLX enters LPI mode for the receive direction when it receives the /P/ code bit pattern (Sleep/Refresh) from its EEE-compliant link partner. It then de-asserts RXDV, asserts RXER, and drives RXD[3:0] to 0001. The KSZ8091MLX remains in the LPI receive state while it continues to receive the refresh from its link partner, so it will

continue to maintain and drive the LPI output states for the MII receive signals to inform the attached EEE-compliant MII MAC that it is in the LPI receive state. When the KSZ8091MLX receives a non /P/ code bit pattern (non-refresh), it exits the LPI receive state and sets the RXDV, RXER, and RX data signals to set a normal frame or normal idle.

The KSZ8091MLX stops the RXC clock output to the MAC after nine or more RXC clock cycles have occurred in the LPI receive state, to save more power. By default, RXC clock stoppage is enabled. It is disabled by writing a '0' to MMD Address 3h, Register 0h, Bit [10].

Figure 3-10 shows the LPI transition for MII (100 Mbps) receive.

**FIGURE 3-10: LPI TRANSITION - MII (100 MBPS) RECEIVE**




### 3.11.3 REGISTERS ASSOCIATED WITH EEE

The following registers are provided for EEE configuration and management:

- Standard Register 13h - AFE Control 4 (to enable 10BASE-Te mode)
- MMD address 1h, Register 0h - PMA/PMD Control 1 (to enable LPI)
- MMD address 1h, Register 1h - PMA/PMD Status 1 (for LPI status)
- MMD address 3h, Register 0h - EEE PCS Control 1 (to stop RXC clock)
- MMD address 7h, Register 3Ch - EEE Advertisement
- MMD address 7h, Register 3Dh - EEE Link Partner Advertisement

## 3.12 Wake-On-LAN

Wake-On-LAN (WOL) is normally a MAC-based function to wake up a host system (for example, an Ethernet end device, such as a PC) that is in standby power mode. Wake-up is triggered by receiving and detecting a special packet (commonly referred to as the "magic packet") that is sent by the remote link partner. The KSZ8091MLX can perform the same WOL function if the MAC address of its associated MAC device is entered into the KSZ8091MLX PHY Registers for magic-packet detection. When the KSZ8091MLX detects the magic packet, it wakes up the host by driving its power management event (PME) output pin low.

By default, the WOL function is disabled. It is enabled by setting the enabling bit and configuring the associated registers for the selected PME wake-up detection method.

The KSZ8091MLX provides three methods to trigger a PME wake-up:

- Magic-packet detection
- Customized-packet detection
- Link status change detection

### 3.12.1 MAGIC-PACKET DETECTION

The magic packet's frame format starts with 6 bytes of 0xFFh and is followed by 16 repetitions of the MAC address of its associated MAC device (local MAC device).

When the magic packet is detected from its link partner, the KSZ8091MLX asserts its PME output pin low.

The following MMD address 1Fh registers are provided for magic-packet detection:

- Magic-packet detection is enabled by writing a '1' to MMD address 1Fh, Register 0h, bit [6]
- The MAC address (for the local MAC device) is written to and stored in MMD address 1Fh, Registers 19h – 1Bh

The KSZ8091MLX does not generate the magic packet. The magic packet must be provided by the external system.

### 3.12.2 CUSTOMIZED-PACKET DETECTION

The customized packet has associated register/bit masks to select which byte, or bytes, of the first 64 bytes of the packet to use in the CRC calculation. After the KSZ8091MLX receives the packet from its link partner, the selected bytes for the received packet are used to calculate the CRC. The calculated CRC is compared to the expected CRC value that was previously written to and stored in the KSZ8091MLX PHY Registers. If there is a match, the KSZ8091MLX asserts its PME output pin low.

Four customized packets are provided to support four types of wake-up scenarios. A dedicated set of registers is used to configure and enable each customized packet.

The following MMD Registers are provided for customized-packet detection:

- Each of the four customized packets is enabled via MMD address 1Fh, Register 0h,
  - Bit [2] // For customized packets, type 0
  - Bit [3] // For customized packets, type 1
  - Bit [4] // For customized packets, type 2
  - Bit [5] // For customized packets, type 3
- Masks to indicate which of the first 64-bytes to use in the CRC calculation are set in:
  - MMD address 1Fh, Registers 1h – 4h // For customized packets, type 0
  - MMD address 1Fh, Registers 7h – Ah // For customized packets, type 1
  - MMD address 1Fh, Registers Dh – 10h // For customized packets, type 2
  - MMD address 1Fh, Registers 13h – 16h // For customized packets, type 3
- 32-bit expected CRCs are written to and stored in:
  - MMD address 1Fh, Registers 5h – 6h // For customized packets, type 0
  - MMD address 1Fh, Registers Bh – Ch // For customized packets, type 1
  - MMD address 1Fh, Registers 11h – 12h // For customized packets, type 2
  - MMD address 1Fh, Registers 17h – 18h // For customized packets, type 3

### 3.12.3 LINK STATUS CHANGE DETECTION

If link status change detection is enabled, the KSZ8091MLX asserts its PME output pin low whenever there is a link status change, using the following MMD address 1Fh register bits and their enabled (1) or disabled (0) settings:

- MMD address 1Fh, Register 0h, bit [0] // For link-up detection
- MMD address 1Fh, Register 0h, bit [1] // For link-down detection

The PME output signal is available on either INTRP/PME_N2 (pin 32) or LED0/PME_N1 (pin 42), and is enabled using standard Register 16h, bit [15]. MMD address 1Fh, Register 0h, bits [15:14] defines and selects the output functions for pins 32 and 42.

The PME output is active low and requires a 1 kΩ pull-up to the VDDIO supply. When asserted, the PME output is cleared by disabling the register bit that enabled the PME trigger source (magic packet, customized packet, link status change).

## 3.13 Reference Circuit for Power and Ground Connections

The KSZ8091MLX is a single 3.3V supply device with a built-in regulator to supply the 1.2V core. The power and ground connections are shown in Figure 3-11 and Table 3-6 for 3.3V VDDIO.

**FIGURE 3-11: KSZ8091MLX POWER AND GROUND CONNECTIONS**

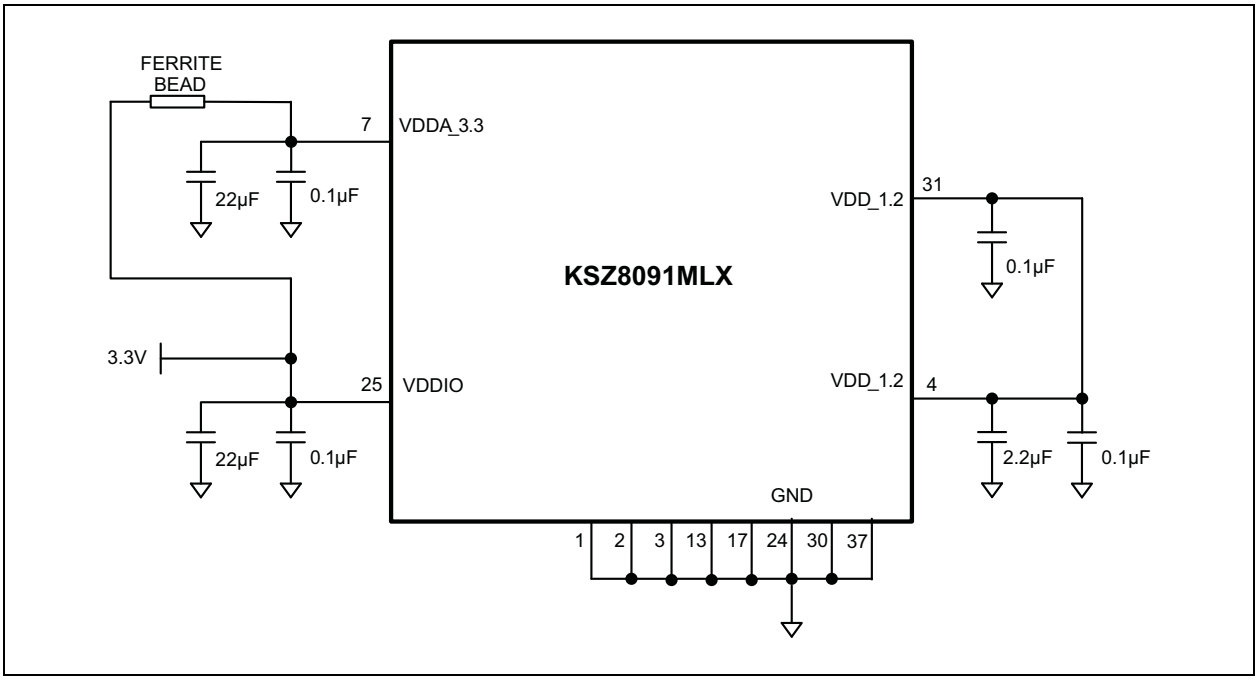



**TABLE 3-6: KSZ8091MLX POWER PIN DESCRIPTION**

| Power Pin | Pin Number | Description |
|---|---|---|
| VDD_1.2 | 4 | Connect with Pin 31 by power trace or plane. Decouple with 2.2 µF and 0.1 µF capacitors to ground. |
| VDDA_3.3 | 7 | Connect to board's 3.3V supply through a ferrite bead. Decouple with 22 µF and 0.1 µF capacitors to ground. |
| VDDIO | 25 | Connect to board's 3.3V supply for 3.3V VDDIO. Decouple with 22 µF and 0.1 µF capacitors to ground. |
| VDD_1.2 | 31 | Connect with Pin 4 by power trace or plane. Decouple with 0.1 µF capacitor to ground. |

## 3.14 Typical Current/Power Consumption

Table 3-7, Table 3-8, and Table 3-9 show typical values for current consumption by the transceiver (VDDA_3.3) and digital I/O (VDDIO) power pins, and typical values for power consumption by the KSZ8091MLX device for the indicated nominal operating voltages. These current and power consumption values include the transmit driver current and on-chip regulator current for the 1.2V core.

**TABLE 3-7: TYPICAL CURRENT/POWER CONSUMPTION (VDDA_3.3 = 3.3V, VDDIO = 3.3V)**

| Condition | 3.3V Transceiver (VDDA_3.3) | 3.3V Digital I/Os (VDDIO) | Total Chip Power |
|---|---|---|---|
| 100BASE-TX Link-up (no traffic) | 34 mA | 12 mA | 152 mW |
| 100BASE-TX Full-duplex @ 100% utilization | 34 mA | 13 mA | 155 mW |
| 10BASE-T Link-up (no traffic) | 14 mA | 11 mA | 82.5 mW |
| 10BASE-T Full-duplex @ 100% utilization | 30 mA | 11 mA | 135 mW |
| EEE 100 Mbps Link-up mode (transmit and receive in LPI state with no traffic) | 13 mA | 10 mA | 75.9 mW |
| Power-saving mode (Reg. 1Fh, Bit [10] = 1) | 13 mA | 10 mA | 75.9 mW |
| EDPD mode (Reg. 18h, Bit [11] = 0) | 10 mA | 10 mA | 66 mW |
| EDPD mode (Reg. 18h, Bit [11] = 0) and PLL off (Reg. 10h, Bit [4] = 1) | 3.77 mA | 1.54 mA | 17.5 mW |
| Software power-down mode (Reg. 0h, Bit [11] =1) | 2.59 mA | 1.51 mA | 13.5 mW |
| Software power-down mode (Reg. 0h, Bit [11] =1) and slow-oscillator mode (Reg. 11h, Bit [5] =1) | 1.36 mA | 0.45 mA | 5.97 mW |

**TABLE 3-8: TYPICAL CURRENT/POWER CONSUMPTION (VDDA_3.3 = 3.3V, VDDIO = 2.5V)**

| Condition | 3.3V Transceiver (VDDA_3.3) | 2.5V Digital I/Os (VDDIO) | Total Chip Power |
|---|---|---|---|
| 100BASE-TX Link-up (no traffic) | 34 mA | 11 mA | 140 mW |
| 100BASE-TX Full-duplex @ 100% utilization | 34 mA | 12 mA | 142 mW |
| 10BASE-T Link-up (no traffic) | 15 mA | 10 mA | 74.5 mW |
| 10BASE-T Full-duplex @ 100% utilization | 27 mA | 10 mA | 114 mW |
| EEE 100 Mbps Link-up mode (transmit and receive in LPI state with no traffic) | 13 mA | 10 mA | 67.9 mW |
| Power-saving mode (Reg. 1Fh, Bit [10] = 1) | 13 mA | 10 mA | 67.9 mW |
| EDPD mode (Reg. 18h, Bit [11] = 0) | 11 mA | 10 mA | 61.3 mW |
| EDPD mode (Reg. 18h, Bit [11] = 0) and PLL off (Reg. 10h, Bit [4] = 1) | 3.55 mA | 1.35 mA | 15.1 mW |
| Software power-down mode (Reg. 0h, Bit [11] =1) | 2.29 mA | 1.34 mA | 10.9 mW |
| Software power-down mode (Reg. 0h, Bit [11] =1) and slow-oscillator mode (Reg. 11h, Bit [5] =1) | 1.15 mA | 0.29 mA | 4.52 mW |

**TABLE 3-9: TYPICAL CURRENT/POWER CONSUMPTION (VDDA_3.3 = 3.3V, VDDIO = 1.8V)**

| Condition | 3.3V Transceiver (VDDA_3.3) | 1.8V Digital I/Os (VDDIO) | Total Chip Power |
|---|---|---|---|
| 100BASE-TX Link-up (no traffic) | 34 mA | 11 mA | 132 mW |
| 100BASE-TX Full-duplex @ 100% utilization | 34 mA | 12 mA | 134 mW |
| 10BASE-T Link-up (no traffic) | 15 mA | 9 mA | 65.7 mW |
| 10BASE-T Full-duplex @ 100% utilization | 27 mA | 9 mA | 105 mW |

**TABLE 3-9: TYPICAL CURRENT/POWER CONSUMPTION (VDDA_3.3 = 3.3V, VDDIO = 1.8V) (CONTINUED)**

| Condition | 3.3V Transceiver (VDDA_3.3) | 1.8V Digital I/Os (VDDIO) | Total Chip Power |
|---|---|---|---|
| EEE 100 Mbps Link-up mode (transmit and receive in LPI state with no traffic) | 13 mA | 9 mA | 59.1 mW |
| Power-saving mode (Reg. 1Fh, Bit [10] = 1) | 13 mA | 9 mA | 59.1 mW |
| EDPD mode (Reg. 18h, Bit [11] = 0) | 11 mA | 9 mA | 52.5 mW |
| EDPD mode (Reg. 18h, Bit [11] = 0) and PLL off (Reg. 10h, Bit [4] = 1) | 4.05 mA | 1.21 mA | 15.5 mW |
| Software power-down mode (Reg. 0h, Bit [11] =1) | 2.79 mA | 1.21 mA | 11.4 mW |
| Software power-down mode (Reg. 0h, Bit [11] =1) and slow-oscillator mode (Reg. 11h, Bit [5] =1) | 1.65 mA | 0.19 mA | 5.79 mW |

## 4.0 REGISTER DESCRIPTIONS

The register space within the KSZ8091MLX consists of two distinct areas.

- Standard registers // Direct register access
- MDIO manageable device (MMD) registers // Indirect register access

The KSZ8091MLX supports the following standard registers.

### 4.1 Register Map

**TABLE 4-1: STANDARD REGISTERS SUPPORTED BY KSZ8091MLX**

| Register Number (hex) | Description |
|---|---|
| **IEEE Defined Registers** | |
| 0h | Basic Control |
| 1h | Basic Status |
| 2h | PHY Identifier 1 |
| 3h | PHY Identifier 2 |
| 4h | Auto-Negotiation Advertisement |
| 5h | Auto-Negotiation Link Partner Ability |
| 6h | Auto-Negotiation Expansion |
| 7h | Auto-Negotiation Next Page |
| 8h | Auto-Negotiation Link Partner Next Page Ability |
| 9h - Ch | Reserved |
| Dh | MMD Access - Control |
| Eh | MMD Access - Register/Data |
| Fh | Reserved |
| **Vendor Specific Registers** | |
| 10h | Digital Reserved Control |
| 11h | AFE Control 1 |
| 12h | Reserved |
| 13h | AFE Control 4 |
| 14h | Reserved |
| 15h | RXER Counter |
| 16h | Operation Mode Strap Override |
| 17h | Operation Mode Strap Status |
| 18h | Expanded Control |
| 19h - 1Ah | Reserved |
| 1Bh | Interrupt Control/Status |
| 1Ch | Reserved |
| 1Dh | LinkMD Cable Diagnostic |
| 1Eh | PHY Control 1 |
| 1Fh | PHY Control 2 |

The KSZ8091MLX supports the following MMD device addresses and their associated register addresses, which make up the indirect MMD registers.

**TABLE 4-2: MMD REGISTERS SUPPORTED BY KSZ8091MLX**

| Device Address (Hex) | Register Address (Hex) | Description |
|---|---|---|
| 1h | 0h | PMA/PMD Control 1 |
| | 1h | PMA/PMD Status 1 |
| 3h | 0h | EEE PCS Control 1 |
| 7h | 3Ch | EEE Advertisement |
| | 3Dh | EEE Link Partner Advertisement |
| 1Fh | 0h | Wake-On-LAN – Control |
| | 1h | Wake-On-LAN – Customized Packet, Type 0, Mask 0 |
| | 2h | Wake-On-LAN – Customized Packet, Type 0, Mask 1 |
| | 3h | Wake-On-LAN – Customized Packet, Type 0, Mask 2 |
| | 4h | Wake-On-LAN – Customized Packet, Type 0, Mask 3 |
| | 5h | Wake-On-LAN – Customized Packet, Type 0, Expected CRC 0 |
| | 6h | Wake-On-LAN – Customized Packet, Type 0, Expected CRC 1 |
| | 7h | Wake-On-LAN – Customized Packet, Type 1, Mask 0 |
| | 8h | Wake-On-LAN – Customized Packet, Type 1, Mask 1 |
| | 9h | Wake-On-LAN – Customized Packet, Type 1, Mask 2 |
| | Ah | Wake-On-LAN – Customized Packet, Type 1, Mask 3 |
| | Bh | Wake-On-LAN – Customized Packet, Type 1, Expected CRC 0 |
| | Ch | Wake-On-LAN – Customized Packet, Type 1, Expected CRC 1 |
| | Dh | Wake-On-LAN – Customized Packet, Type 2, Mask 0 |
| | Eh | Wake-On-LAN – Customized Packet, Type 2, Mask 1 |
| | Fh | Wake-On-LAN – Customized Packet, Type 2, Mask 2 |
| | 10h | Wake-On-LAN – Customized Packet, Type 2, Mask 3 |
| | 11h | Wake-On-LAN – Customized Packet, Type 2, Expected CRC 0 |
| | 12h | Wake-On-LAN – Customized Packet, Type 2, Expected CRC 1 |
| | 13h | Wake-On-LAN – Customized Packet, Type 3, Mask 0 |
| | 14h | Wake-On-LAN – Customized Packet, Type 3, Mask 1 |
| | 15h | Wake-On-LAN – Customized Packet, Type 3, Mask 2 |
| | 16h | Wake-On-LAN – Customized Packet, Type 3, Mask 3 |
| | 17h | Wake-On-LAN – Customized Packet, Type 3, Expected CRC 0 |
| | 18h | Wake-On-LAN – Customized Packet, Type 3, Expected CRC 1 |
| | 19h | Wake-On-LAN – Magic Packet, MAC-DA-0 |
| | 1Ah | Wake-On-LAN – Magic Packet, MAC-DA-1 |
| | 1Bh | Wake-On-LAN – Magic Packet, MAC-DA-2 |

## 4.2 Standard Registers

Standard registers provide direct read/write access to a 32-register address space, as defined in Clause 22 of the IEEE 802.3 Specification. Within this address space, the first 16 registers (Registers 0h to Fh) are defined according to the IEEE specification, while the remaining 16 registers (Registers 10h to 1Fh) are defined specific to the PHY vendor.

**TABLE 4-3: IEEE DEFINED REGISTER DESCRIPTIONS**

| Address | Name | Description | Mode Note 4-1 | Default |
|---|---|---|---|---|
| **Register 0h – Basic Control** | | | | |
| 0.15 | Reset | 1 = Software reset<br>0 = Normal operation<br>This bit is self-cleared after a '1' is written to it. | RW/SC | 0 |
| 0.14 | Loopback | 1 = Loopback mode<br>0 = Normal operation | RW | 0 |
| 0.13 | Speed Select | 1 = 100 Mbps<br>0 = 10 Mbps<br>This bit is ignored if auto-negotiation is enabled (Register 0.12 = 1). | RW | Set by the SPEED strap-in pin.<br>See the Strap-In Options section for details. |
| 0.12 | Auto-Negotiation Enable | 1 = Enable auto-negotiation process<br>0 = Disable auto-negotiation process<br>If enabled, the auto-negotiation result overrides the settings in Registers 0.13 and 0.8. | RW | Set by the NWAYEN strap-in pin.<br>See the Strap-In Options section for details. |
| 0.11 | Power-Down | 1 = Power-down mode<br>0 = Normal operation<br>If software reset (Register 0.15) is used to exit power-down mode (Register 0.11 = 1), two software reset writes (Register 0.15 = 1) are required. The first write clears power-down mode; the second write resets the chip and re-latches the pin strap-in pin values. | RW | 0 |
| 0.10 | Isolate | 1 = Electrical isolation of PHY from MII<br>0 = Normal operation | RW | Set by the ISO strap-in pin.<br>See the Strap-In Options section for details. |
| 0.9 | Restart Auto-Negotiation | 1 = Restart auto-negotiation process<br>0 = Normal operation.<br>This bit is self-cleared after a '1' is written to it. | RW/SC | 0 |
| 0.8 | Duplex Mode | 1 = Full-duplex<br>0 = Half-duplex | RW | The inverse of the DUPLEX strap-in pin value.<br>See the Strap-In Options section for details. |
| 0.7 | Collision Test | 1 = Enable COL test<br>0 = Disable COL test | RW | 0 |
| 0.6:0 | Reserved | Reserved | RO | 000_0000 |
| **Register 1h - Basic Status** | | | | |
| 1.15 | 100BASE-T4 | 1 = T4 capable<br>0 = Not T4 capable | RO | 0 |
| 1.14 | 100BASE-TX Full-Duplex | 1 = Capable of 100 Mbps full-duplex<br>0 = Not capable of 100 Mbps full-duplex | RO | 1 |

**TABLE 4-3: IEEE DEFINED REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode Note 4-1 | Default |
|---|---|---|---|---|
| 1.13 | 100BASE-TX Half-Duplex | 1 = Capable of 100 Mbps half-duplex<br>0 = Not capable of 100 Mbps half-duplex | RO | 1 |
| 1.12 | 10BASE-T Full-Duplex | 1 = Capable of 10 Mbps full-duplex<br>0 = Not capable of 10 Mbps full-duplex | RO | 1 |
| 1.11 | 10BASE-T Half-Duplex | 1 = Capable of 10 Mbps half-duplex<br>0 = Not capable of 10 Mbps half-duplex | RO | 1 |
| 1.10:7 | Reserved | Reserved | RO | 000_0 |
| 1.6 | No Preamble | 1 = Preamble suppression<br>0 = Normal preamble | RO | 1 |
| 1.5 | Auto-Negotiation Complete | 1 = Auto-negotiation process completed<br>0 = Auto-negotiation process not completed | RO | 0 |
| 1.4 | Remote Fault | 1 = Remote fault<br>0 = No remote fault | RO/LH | 0 |
| 1.3 | Auto-Negotiation Ability | 1 = Can perform auto-negotiation<br>0 = Cannot perform auto-negotiation | RO | 1 |
| 1.2 | Link Status | 1 = Link is up<br>0 = Link is down | RO/LL | 0 |
| 1.1 | Jabber Detect | 1 = Jabber detected<br>0 = Jabber not detected (default is low) | RO/LH | 0 |
| 1.0 | Extended Capability | 1 = Supports extended capability registers | RO | 1 |
| **Register 2h - PHY Identifier 1** | | | | |
| 2.15:0 | PHY ID Number | Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI). KENDIN Communication's OUI is 0010A1 (hex). | RO | 0022h |
| **Register 3h - PHY Identifier 2** | | | | |
| 3.15:10 | PHY ID Number | Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI). KENDIN Communication's OUI is 0010A1 (hex). | RO | 0001_01 |
| 3.9:4 | Model Number | Six-bit manufacturer's model number | RO | 01_0110 |
| 3.3:0 | Revision Number | Four-bit manufacturer's revision number | RO | Indicates silicon revision. |
| **Register 4h - Auto-Negotiation Advertisement** | | | | |
| 4.15 | Next Page | 1 = Next page capable<br>0 = No next page capability | RW | 1 |
| 4.14 | Reserved | Reserved | RO | 0 |
| 4.13 | Remote Fault | 1 = Remote fault supported<br>0 = No remote fault | RW | 0 |
| 4.12 | Reserved | Reserved | RO | 0 |
| 4.11:10 | Pause | [00] = No pause<br>[10] = Asymmetric pause<br>[01] = Symmetric pause<br>[11] = Asymmetric and symmetric pause | RW | 00 |
| 4.9 | 100BASE-T4 | 1 = T4 capable<br>0 = No T4 capability | RO | 0 |

**TABLE 4-3: IEEE DEFINED REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode Note 4-1 | Default |
|---|---|---|---|---|
| 4.8 | 100BASE-TX Full-Duplex | 1 = 100 Mbps full-duplex capable<br>0 = No 100 Mbps full-duplex capability | RW | Set by the SPEED strap-in pin. See the Strap-In Options section for details. |
| 4.7 | 100BASE-TX Half-Duplex | 1 = 100 Mbps half-duplex capable<br>0 = No 100 Mbps half-duplex capability | RW | Set by the SPEED strap-in pin.<br>See the Strap-In Options section for details. |
| 4.6 | 10BASE-T Full-Duplex | 1 = 10 Mbps full-duplex capable<br>0 = No 10 Mbps full-duplex capability | RW | 1 |
| 4.5 | 10BASE-T Half-Duplex | 1 = 10 Mbps half-duplex capable<br>0 = No 10 Mbps half-duplex capability | RW | 1 |
| 4.4:0 | Selector Field | [00001] = IEEE 802.3 | RW | 0_0001 |
| **Register 5h - Auto-Negotiation Link Partner Ability** | | | | |
| 5.15 | Next Page | 1 = Next page capable<br>0 = No next page capability | RO | 0 |
| 5.14 | Acknowledge | 1 = Link code word received from partner<br>0 = Link code word not yet received | RO | 0 |
| 5.13 | Remote Fault | 1 = Remote fault detected<br>0 = No remote fault | RO | 0 |
| 5.12 | Reserved | Reserved | RO | 0 |
| 5.11:10 | Pause | [00] = No pause<br>[10] = Asymmetric pause<br>[01] = Symmetric pause<br>[11] = Asymmetric and symmetric pause | RO | 00 |
| 5.9 | 100BASE-T4 | 1 = T4 capable<br>0 = No T4 capability | RO | 0 |
| 5.8 | 100BASE-TX Full-Duplex | 1 = 100 Mbps full-duplex capable<br>0 = No 100 Mbps full-duplex capability | RO | 0 |
| 5.7 | 100BASE-TX Half-Duplex | 1 = 100 Mbps half-duplex capable<br>0 = No 100 Mbps half-duplex capability | RO | 0 |
| 5.6 | 10BASE-T Full-Duplex | 1 = 10 Mbps full-duplex capable<br>0 = No 10 Mbps full-duplex capability | RO | 0 |
| 5.5 | 10BASE-T Half-Duplex | 1 = 10 Mbps half-duplex capable<br>0 = No 10 Mbps half-duplex capability | RO | 0 |
| 5.4:0 | Selector Field | [00001] = IEEE 802.3 | RO | 0_0001 |
| **Register 6h - Auto-Negotiation Expansion** | | | | |
| 6.15:5 | Reserved | Reserved | RO | 0000_0000_000 |
| 6.4 | Parallel Detection Fault | 1 = Fault detected by parallel detection<br>0 = No fault detected by parallel detection | RO/LH | 0 |
| 6.3 | Link Partner Next Page Able | 1 = Link partner has next page capability<br>0 = Link partner does not have next page capability | RO | 0 |
| 6.2 | Next Page Able | 1 = Local device has next page capability<br>0 = Local device does not have next page capability | RO | 1 |

**TABLE 4-3: IEEE DEFINED REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode Note 4-1 | Default |
|---|---|---|---|---|
| 6.1 | Page Received | 1 = New page received<br>0 = New page not received yet | RO/LH | 0 |
| 6.0 | Link Partner Auto-Negotiation Able | 1 = Link partner has auto-negotiation capability<br>0 = Link partner does not have auto-negotiation capability | RO | 0 |
| **Register 7h - Auto-Negotiation Next Page** | | | | |
| 7.15 | Next Page | 1 = Additional next pages will follow<br>0 = Last page | RW | 0 |
| 7.14 | Reserved | Reserved | RO | 0 |
| 7.13 | Message Page | 1 = Message page<br>0 = Unformatted page | RW | 1 |
| 7.12 | Acknowledge2 | 1 = Will comply with message<br>0 = Cannot comply with message | RW | 0 |
| 7.11 | Toggle | 1 = Previous value of the transmitted link code word equaled logic 1<br>0 = Logic 0 | RO | 0 |
| 7.10:0 | Message Field | 11-bit wide field to encode 2048 messages | RW | 000_0000_0001 |
| **Register 8h - Auto-Negotiation Link Partner Next Page Ability** | | | | |
| 8.15 | Next Page | 1 = Additional next pages will follow<br>0 = Last page | RO | 0 |
| 8.14 | Acknowledge | 1 = Successful receipt of link word<br>0 = No successful receipt of link word | RO | 0 |
| 8.13 | Message Page | 1 = Message page<br>0 = Unformatted page | RO | 0 |
| 8.12 | Acknowledge2 | 1 = Can act on the information<br>0 = Cannot act on the information | RO | 0 |
| 8.11 | Toggle | 1 = Previous value of transmitted link code word equal to logic 0<br>0 = Previous value of transmitted link code word equal to logic 1 | RO | 0 |
| 8.10:0 | Message Field | 11-bit wide field to encode 2048 messages | RO | 000_0000_0000 |
| **Register Dh - MMD Access - Control** | | | | |
| D.15:14 | MMD – Operation Mode | For the selected MMD device address (bits [4:0] of this register), these two bits select one of the following register or data operations and the usage for MMD Access – Register/Data (Reg. Eh).<br>00 = Register<br>01 = Data, no post increment<br>10 = Data, post increment on reads and writes<br>11 = Data, post increment on writes only | RW | 00 |
| D.13:5 | Reserved | Reserved | RW | 00_0000_000 |
| D.4:0 | MMD – Device Address | These five bits set the MMD device address. | RW | 0_0000 |

**TABLE 4-3: IEEE DEFINED REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode Note 4-1 | Default |
|---|---|---|---|---|
| **Register Eh - MMD Access - Register/Data** | | | | |
| E.15:0 | MMD – Register/ Data | For the selected MMD device address (Reg. Dh, bits [4:0]),<br>When Reg. Dh, bits [15:14] = 00, this register contains the read/write register address for the MMD device address.<br>Otherwise, this register contains the read/write data value for the MMD device address and its selected register address.<br>See also Reg. Dh, bits [15:14], for descriptions of post increment reads and writes of this register for data operation. | RW | 0000_0000_0000_ 0000 |

**Note 4-1** RW = Read/Write; RO = Read Only; SC = Self-Cleared; LH = Latch High; LL = Latch Low.

**TABLE 4-4: VENDOR SPECIFIC REGISTER DESCRIPTIONS**

| Address | Name | Description | Mode Note 4-1 | Default |
|---|---|---|---|---|
| **Register 10h – Digital Reserved Control** | | | | |
| 10.15:5 | Reserved | Reserved | RW | 0000_0000_000 |
| 10.4 | PLL Off | 1 = Turn PLL off automatically in EDPD mode<br>0 = Keep PLL on in EDPD mode.<br>See also Register 18h, Bit [11] for EDPD mode | RW | 0 |
| 10.3:0 | Reserved | Reserved | RW | 0000 |
| **Register 11h – AFE Control 1** | | | | |
| 11.15:6 | Reserved | Reserved | RW | 0000_0000_00 |
| 11.5 | Slow-Oscillator Mode Enable | Slow-oscillator mode is used to disconnect the input reference crystal/clock on the XI pin and select the on-chip slow oscillator when the KSZ8091MLX device is not in use after power-up.<br>1 = Enable<br>0 = Disable<br>This bit automatically sets software power-down to the analog side when enabled. | RW | 0 |
| 11.4:0 | Reserved | Reserved | RW | 0_0000 |
| **Register 13h - AFE Control 4** | | | | |
| 13.15:5 | Reserved | Reserved | RW | 0000_0000_000 |
| 13.4 | 10BASE-Te Mode | 1 = EEE 10BASE-Te (1.75V TX amplitude) and also set MMD Address 1Ch, Register 4h, Bit [13] to ‘0’.<br>0 = Standard 10BASE-T (2.5V TX amplitude) and also set MMD Address 1Ch, Register 4h, Bit [13] to ‘1’. | RW | 0 |
| 13.3:0 | Reserved | Reserved | RW | 0000 |
| **Register 15h – RXER Counter** | | | | |
| 15.15:0 | RXER Counter | Receive error counter for symbol error frames | RO/SC | 0000h |

**TABLE 4-4: VENDOR SPECIFIC REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode Note 4-1 | Default |
|---|---|---|---|---|
| **Register 16h – Operation Mode Strap Override** | | | | |
| 16.15 | PME Enable | PME for Wake-on-LAN<br>1 = Enable<br>0 = Disable<br>This bit works in conjunction with MMD Address 1Fh, Reg. 0h, Bits [15:14] to define the output for pins 32 and 42. | RW | Set by the PME_EN strap-in pin.<br>See the Strap-In Options section for details. |
| 16.14:11 | Reserved | Reserved | RW | 000_0 |
| 16.10 | Reserved | Reserved | RO | 0 |
| 16.9 | B-CAST_OFF Override | 1 = Override strap-in for B-CAST_OFF<br>If bit is '1', PHY Address 0 is non-broadcast. | RW | 0 |
| 16.8 | Reserved | Reserved | RW | 0 |
| 16.7 | MII B-to-B Override | 1 = Override strap-in for MII back-to-back mode (also set bit 0 of this register to '1') | RW | 0 |
| 16.6 | Reserved | Reserved | RW | 0 |
| 16.5 | NAND Tree Override | 1 = Override strap-in for NAND tree mode | RW | 0 |
| 16.4:1 | Reserved | Reserved | RW | 0_000 |
| 16.0 | MII Override | 1 = Override strap-in for MII mode | RW | 1 |
| **Register 17h - Operation Mode Strap Status** | | | | |
| 17.15:13 | PHYAD[2:0] Strap-In Status | [000] = Strap to PHY Address 0<br>[001] = Strap to PHY Address 1<br>[010] = Strap to PHY Address 2<br>[011] = Strap to PHY Address 3<br>[100] = Strap to PHY Address 4<br>[101] = Strap to PHY Address 5<br>[110] = Strap to PHY Address 6<br>[111] = Strap to PHY Address 7 | RO | — |
| 17.12:10 | Reserved | Reserved | RO | — |
| 17.9 | B-CAST_OFF Strap-In Status | 1 = Strap to B-CAST_OFF<br>If bit is '1', PHY Address 0 is non-broadcast. | RO | — |
| 17.8 | Reserved | Reserved | RO | — |
| 17.7 | MII B-to-B Strap-In Status | 1 = Strap to MII back-to-back mode | RO | — |
| 17.6 | Reserved | Reserved | RO | — |
| 17.5 | NAND Tree Strap-In Status | 1 = Strap to NAND tree mode | RO | — |
| 17.4:1 | Reserved | Reserved | RO | — |
| 17.0 | MII Strap-In Status | 1 = Strap to MII mode | RO | — |
| **Register 18h - Expanded Control** | | | | |
| 18.15:12 | Reserved | Reserved | RW | 0000 |

**TABLE 4-4: VENDOR SPECIFIC REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode Note 4-1 | Default |
|---|---|---|---|---|
| 18.11 | EDPD Disabled | Energy-detect power-down mode<br>1 = Disable<br>0 = Enable<br>See also Register 10h, Bit [4] for PLL off. | RW | 1 |
| 18.10 | 100BASE-TX Latency | 1 = MII output is random latency<br>0 = MII output is fixed latency<br>For both settings, all bytes of received preamble are passed to the MII output. | RW | 0 |
| 18.9:7 | Reserved | Reserved | RW | 00_0 |
| 18.6 | 10BASE-T Preamble Restore | 1 = Restore received preamble to MII output<br>0 = Remove all seven bytes of preamble before sending frame (starting with SFD) to MII output | RW | 0 |
| 18.5:0 | Reserved | Reserved | RW | 00_0001 |
| **Register 1Bh – Interrupt Control/Status** | | | | |
| 1B.15 | Jabber Interrupt Enable | 1 = Enable jabber interrupt<br>0 = Disable jabber interrupt | RW | 0 |
| 1B.14 | Receive Error Interrupt Enable | 1 = Enable receive error interrupt<br>0 = Disable receive error interrupt | RW | 0 |
| 1B.13 | Page Received Interrupt Enable | 1 = Enable page received interrupt<br>0 = Disable page received interrupt | RW | 0 |
| 1B.12 | Parallel Detect Fault Interrupt Enable | 1 = Enable parallel detect fault interrupt<br>0 = Disable parallel detect fault interrupt | RW | 0 |
| 1B.11 | Link Partner Acknowledge Interrupt Enable | 1 = Enable link partner acknowledge interrupt<br>0 = Disable link partner acknowledge interrupt | RW | 0 |
| 1B.10 | Link-Down Interrupt Enable | 1= Enable link-down interrupt<br>0 = Disable link-down interrupt | RW | 0 |
| 1B.9 | Remote Fault Interrupt Enable | 1 = Enable remote fault interrupt<br>0 = Disable remote fault interrupt | RW | 0 |
| 1B.8 | Link-Up Interrupt Enable | 1 = Enable link-up interrupt<br>0 = Disable link-up interrupt | RW | 0 |
| 1B.7 | Jabber Interrupt | 1 = Jabber occurred<br>0 = Jabber did not occur | RO/SC | 0 |
| 1B.6 | Receive Error Interrupt | 1 = Receive error occurred<br>0 = Receive error did not occur | RO/SC | 0 |
| 1B.5 | Page Receive Interrupt | 1 = Page receive occurred<br>0 = Page receive did not occur | RO/SC | 0 |
| 1B.4 | Parallel Detect Fault Interrupt | 1 = Parallel detect fault occurred<br>0 = Parallel detect fault did not occur | RO/SC | 0 |

**TABLE 4-4: VENDOR SPECIFIC REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode Note 4-1 | Default |
|---|---|---|---|---|
| 1B.3 | Link Partner Acknowl-edge Inter-rupt | 1 = Link partner acknowledge occurred<br>0 = Link partner acknowledge did not occur | RO/SC | 0 |
| 1B.2 | Link-Down Interrupt | 1 = Link-down occurred<br>0 = Link-down did not occur | RO/SC | 0 |
| 1B.1 | Remote Fault Interrupt | 1 = Remote fault occurred<br>0 = Remote fault did not occur | RO/SC | 0 |
| 1B.0 | Link-Up Interrupt | 1 = Link-up occurred<br>0 = Link-up did not occur | RO/SC | 0 |
| **Register 1Dh – LinkMD Control/Status** | | | | |
| 1D.15 | Cable Diag-nostic Test Enable | 1 = Enable cable diagnostic test. After test has completed, this bit is self-cleared.<br>0 = Indicates cable diagnostic test (if enabled) has completed and the status information is valid for read. | RW/SC | 0 |
| 1D.14:13 | Cable Diag-nostic Test Result | [00] = Normal condition<br>[01] = Open condition has been detected in cable<br>[10] = Short condition has been detected in cable<br>[11] = Cable diagnostic test has failed | RO | 00 |
| 1D.12 | Short Cable Indicator | 1 = Short cable (<10 meter) has been detected by LinkMD | RO | 0 |
| 1D.11:9 | Reserved | Reserved | RW | 000 |
| 1D.8:0 | Cable Fault Counter | Distance to fault | RO | 0_0000_0000 |
| **Register 1Eh – PHY Control 1** | | | | |
| 1E.15:10 | Reserved | Reserved | RO | 0000_00 |
| 1E.9 | Enable Pause (Flow Control) | 1 = Flow control capable<br>0 = No flow control capability | RO | 0 |
| 1E.8 | Link Status | 1 = Link is up<br>0 = Link is down | RO | 0 |
| 1E.7 | Polarity Status | 1 = Polarity is reversed<br>0 = Polarity is not reversed | RO | — |
| 1E.6 | Reserved | Reserved | RO | 0 |
| 1E.5 | MDI/MDI-X State | 1 = MDI-X<br>0 = MDI | RO | — |
| 1E.4 | Energy Detect | 1 = Signal present on receive differential pair<br>0 = No signal detected on receive differential pair | RO | 0 |
| 1E.3 | PHY Isolate | 1 = PHY in isolate mode<br>0 = PHY in normal operation | RW | 0 |
| 1E.2:0 | Operation Mode Indication | [000] = Still in auto-negotiation<br>[001] = 10BASE-T half-duplex<br>[010] = 100BASE-TX half-duplex<br>[011] = Reserved<br>[100] = Reserved<br>[101] = 10BASE-T full-duplex<br>[110] = 100BASE-TX full-duplex<br>[111] = Reserved | RO | 000 |

**TABLE 4-4: VENDOR SPECIFIC REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode Note 4-1 | Default |
|---|---|---|---|---|
| **Register 1Fh – PHY Control 2** | | | | |
| 1F.15 | HP_MDIX | 1 = HP Auto MDI/MDI-X mode<br>0 = Microchip Auto MDI/MDI-X mode | RW | 1 |
| 1F.14 | MDI/MDI-X Select | When Auto MDI/MDI-X is disabled,<br>1 = MDI-X mode<br>Transmit on RXP, RXM (Pins 10, 9) and Receive on TXP, TXM (Pins 12, 11)<br>0 = MDI mode<br>Transmit on TXP, TXM (Pins 12, 11) and Receive on RXP, RXM (Pins 10, 9) | RW | 0 |
| 1F.13 | Pair Swap Disable | 1 = Disable Auto MDI/MDI-X<br>0 = Enable Auto MDI/MDI-X | RW | 0 |
| 1F.12 | Reserved | Reserved | RW | 0 |
| 1F.11 | Force Link | 1 = Force link pass<br>0 = Normal link operation<br>This bit bypasses the control logic and allows the transmitter to send a pattern even if there is no link. | RW | 0 |
| 1F.10 | Power Saving | 1 = Enable power saving<br>0 = Disable power saving | RW | 0 |
| 1F.9 | Interrupt Level | 1 = Interrupt pin active high<br>0 = Interrupt pin active low | RW | 0 |
| 1F.8 | Enable Jabber | 1 = Enable jabber counter<br>0 = Disable jabber counter | RW | 1 |
| 1F.7:6 | Reserved | Reserved | RW | 0 |
| 1F.5:4 | LED Mode | [00] = LED1: Speed<br>LED0: Link/Activity<br>[01] = LED1: Activity<br>LED0: Link<br>[10], [11] = Reserved | RW | 00 |
| 1F.3 | Disable Transmitter | 1 = Disable transmitter<br>0 = Enable transmitter | RW | 0 |
| 1F.2 | Remote Loopback | 1 = Remote (analog) loopback is enabled<br>0 = Normal mode | RW | 0 |
| 1F.1 | Enable SQE Test | 1 = Enable SQE test<br>0 = Disable SQE test | RW | 0 |
| 1F.0 | Disable Data Scrambling | 1 = Disable scrambler<br>0 = Enable scrambler | RW | 0 |

**Note 4-1** RW = Read/Write; RO = Read Only; SC = Self-Cleared.

## 4.3 MMD Registers

MMD registers provide indirect read/write access to up to 32 MMD Device Addresses with each device supporting up to 65,536 16-bit registers, as defined in Clause 22 of the IEEE 802.3 Specification. The KSZ8091MLX, however, uses only a small fraction of the available registers. See the Register Descriptions section for a list of supported MMD device addresses and their associated register addresses.

The following two standard registers serve as the portal registers to access the indirect MMD registers.

- Standard register Dh – MMD Access – Control
- Standard register Eh – MMD Access – Register/Data

**TABLE 4-5: PORTAL REGISTERS (ACCESS TO INDIRECT MMD REGISTERS)**

| Address | Name | Description | Mode | Default |
|---|---|---|---|---|
| **Register Dh - MMD Access - Control** | | | | |
| D.15:14 | MMD – Operation Mode | For the selected MMD device address (bits [4:0] of this register), these two bits select one of the following register or data operations and the usage for MMD Access – Register/Data (Reg. Eh).<br>00 = Register<br>01 = Data, no post increment<br>10 = Data, post increment on reads and writes<br>11 = Data, post increment on writes only | RW | 00 |
| D.13:5 | Reserved | Reserved | RW | 00_0000_000 |
| D.4:0 | MMD – Device Address | These five bits set the MMD device address. | RW | 0_0000 |
| **Register Eh - MMD Access - Register/Data** | | | | |
| E.15:0 | MMD – Register/ Data | For the selected MMD device address (Reg. Dh, bits [4:0]),<br>When Reg. Dh, bits [15:14] = 00, this register contains the read/write register address for the MMD device address.<br>Otherwise, this register contains the read/write data value for the MMD device address and its selected register address.<br>See also Reg. Dh, bits [15:14], for descriptions of post increment reads and writes of this register for data operation. | RW | 0000_0000_0000_ 0000 |

Examples:

**MMD Register Write**

Write MMD – Device Address 1Fh, Register 0h = 0001h to enable link-up detection to trigger PME for WOL.

1. Write Register Dh with 001Fh // Set up register address for MMD – Device Address 1Fh.
2. Write Register Eh with 0000h // Select register 0h of MMD – Device Address 1Fh.
3. Write Register Dh with 401Fh // Select register data for MMD – Device Address 1Fh, Register 0h.
4. Write Register Eh with 0001h // Write value 0001h to MMD – Device Address 1Fh, Register 0h.

**MMD Register Read**

Read MMD – Device Address 1Fh, Register 19h – 1Bh for the magic packet's MAC address

1. Write Register Dh with 001Fh // Set up register address for MMD – Device Address 1Fh.
2. Write Register Eh with 0019h // Select Register 19h of MMD – Device Address 1Fh.
3. Write Register Dh with 801Fh // Select register data for MMD – Device Address 1Fh, Register 19h // with post increments
4. Read Register Eh // Read data in MMD – Device Address 1Fh, Register 19h.
5. Read Register Eh // Read data in MMD – Device Address 1Fh, Register 1Ah.
6. Read Register Eh // Read data in MMD – Device Address 1Fh, Register 1Bh.

**TABLE 4-6: MMD REGISTER DESCRIPTIONS**

| Address | Name | Description | Mode | Default |
|---|---|---|---|---|
| **MMD Address 1h, Register 0h – PMA/PMD Control 1** | | | | |
| 1.0.15:13 | Reserved | Reserved | RW | 000 |
| 1.0.12 | LPI enable | Lower Power Idle enable | RW | 0 |
| 1.0.11:0 | Reserved | Reserved | RW | 0000_0000_0000 |

**TABLE 4-6: MMD REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode | Default |
|---|---|---|---|---|
| **MMD Address 1h, Register 1h – PMA/PMD Status 1** | | | | |
| 1.1.15:9 | Reserved | Reserved | RO | 0000_000 |
| 1.1.8 | LPI State Entered | 1 = PMA/PMD has entered LPI state<br>0 = PMA/PMD has not entered LPI state | RO/LH | 0 |
| 1.1.7:4 | Reserved | Reserved | RO | 0000 |
| 1.1.3 | LPI State Indication | 1 = PMA/PMD is currently in LPI state<br>0 = PMA/PMD is currently not in LPI state | RO | 0 |
| 1.1.2:0 | Reserved | Reserved | RO | 000 |
| **MMD Address 3h, Register 0h – EEE PCS Control 1** | | | | |
| 3.0.15:12 | Reserved | Reserved | RO | 0000 |
| 3.0.11 | Reserved | Reserved | RW | 1 |
| 3.0.10 | 100BASE-TX RXC Clock Stoppable | During receive lower-power idle mode,<br>1 = RXC clock is stoppable for 100BASE-TX<br>0 = RXC clock is not stoppable for 100BASE-TX | RW | 1 |
| 3.0.9:4 | Reserved | Reserved | RW | 00_0001 |
| 3.0.3:2 | Reserved | Reserved | RO | 00 |
| 3.0.1:0 | Reserved | Reserved | RW | 00 |
| **MMD Address 7h, Register 3Ch – EEE Advertisement** | | | | |
| 7.3C.15:3 | Reserved | Reserved | RO | 0000_0000_0000_0 |
| 7.3C.2 | 1000BASE-T EEE Capable | 0 = 1000 Mbps EEE is not supported | RO | 0 |
| 7.3C.1 | 100BASE-TX EEE Capable | 1 = 100 Mbps EEE capable<br>0 = No 100 Mbps EEE capability<br>This bit is set to ‘0’ as the default after power-up or reset. Set this bit to ‘1’ to enable 100 Mbps EEE mode. | RW | 0 |
| 7.3C.0 | Reserved | Reserved | RO | 0 |
| **MMD Address 7h, Register 3Dh – EEE Link Partner Advertisement** | | | | |
| 7.3D.15:3 | Reserved | Reserved | RO | 0000_0000_0000_0 |
| 7.3D.2 | 1000BASE-T EEE Capable | 1 = 1000 Mbps EEE capable<br>0 = No 1000 Mbps EEE capability | RO | 0 |
| 7.3D.1 | 100BASE-TX EEE Capable | 1 = 100 Mbps EEE capable<br>0 = No 100 Mbps EEE capability | RO | 0 |
| 7.3D.0 | Reserved | Reserved | RO | 0 |
| **MMD Address 1Ch, Register 4h – DSP 10BASE-T/10BASE-Te Control** | | | | |
| 1C.4.15 | Reserved | Reserved | RW | 0 |
| 1C.4.14 | Reserved | Reserved | RO | 0 |
| 1C.4.13 | DSP 10BASE-T/ 10BASE-Te Mode Select | 1 = Standard 10BASE-T (2.5V TX amplitude) and also set Standard Register 13h, Bit [4] to ‘0’.<br>0 = EEE 10BASE-Te (1.75 TX amplitude) and also set Standard Register 13h, Bit [4] to ‘1’. | RW | 1 |
| 1C.4.12 | Reserved | Reserved | RW | 0 |
| 1C.4.11:0 | Reserved | Reserved | RO | 0000_0000_0000 |

**TABLE 4-6: MMD REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode | Default |
|---|---|---|---|---|
| **MMD Address 1Fh, Register 0h – Wake-On-LAN – Control** | | | | |
| 1F.0.15:14 | PME Output Select | These two bits work in conjunction with Reg. 16h, Bit [15] for PME enable to define the output for pins 32 and 42.<br>INTRP/PME_N2 (pin 32)<br>00 = INTRP output<br>01 = PME_N2 output<br>10 = INTRP and PME_N2 output<br>11 = Reserved<br>LED0/PME_N1 (pin 42)<br>00 = PME_N1 output<br>01 = LED0 output<br>10 = LED0 output<br>11 = PME_N1 output | RW | 00 |
| 1F.0.13:7 | Reserved | Reserved | RO | 00_0000_0 |
| 1F.0.6 | Magic Packet Detect Enable | 1 = Enable magic-packet detection<br>0 = Disable magic-packet detection | RW | 0 |
| 1F.0.5 | Custom-Packet Type 3 Detect Enable | 1 = Enable custom-packet, Type 3 detection<br>0 = Disable custom-packet, Type 3 detection | RW | 0 |
| 1F.0.4 | Custom-Packet Type 2 Detect Enable | 1 = Enable custom-packet, Type 2 detection<br>0 = Disable custom-packet, Type 2 detection | RW | 0 |
| 1F.0.3 | Custom-Packet Type 1 Detect Enable | 1 = Enable custom-packet, Type 1 detection<br>0 = Disable custom-packet, Type 1 detection | RW | 0 |
| 1F.0.2 | Custom-Packet Type 0 Detect Enable | 1 = Enable custom-packet, Type 0 detection<br>0 = Disable custom-packet, Type 0 detection | RW | 0 |
| 1F.0.1 | Link-Down Detect Enable | 1 = Enable link-down detection<br>0 = Disable link-down detection | RW | 0 |
| 1F.0.0 | Link-Up Detect Enable | 1 = Enable link-up detection<br>0 = Disable link-up detection | RW | 0 |

**TABLE 4-6: MMD REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode | Default |
|---|---|---|---|---|
| **MMD Address 1Fh, Register 1h – Wake-On-LAN – Customized Packet, Type 0, Mask 0<br>MMD Address 1Fh, Register 7h – Wake-On-LAN – Customized Packet, Type 1, Mask 0<br>MMD Address 1Fh, Register Dh – Wake-On-LAN – Customized Packet, Type 2, Mask 0<br>MMD Address 1Fh, Register 13h – Wake-On-LAN – Customized Packet, Type 3, Mask 0** | | | | |
| 1F.1.15:0<br>1F.7.15:0<br>1F.D.15:0<br>1F.13.15:0 | Custom Packet Type X Mask 0 | This register selects the bytes in the first 16 bytes of the packet (bytes 1 through 16) that will be used for CRC calculation.<br>For each bit in this register,<br>1 = Byte is selected for CRC calculation<br>0 = Byte is not selected for CRC calculation<br>The register-bit to packet-byte mapping is as follows:<br>Bit [15]: byte-16<br>... : ...<br>Bit [1]: byte-2<br>Bit [0]: byte-1 | RW | 0000_0000_0000_0000 |
| **MMD Address 1Fh, Register 2h – Wake-On-LAN – Customized Packet, Type 0, Mask 1<br>MMD Address 1Fh, Register 8h – Wake-On-LAN – Customized Packet, Type 1, Mask 1<br>MMD Address 1Fh, Register Eh – Wake-On-LAN – Customized Packet, Type 2, Mask 1<br>MMD Address 1Fh, Register 14h – Wake-On-LAN – Customized Packet, Type 3, Mask 1** | | | | |
| 1F.2.15:0<br>1F.8.15:0<br>1F.E.15:0<br>1F.14.15:0 | Custom Packet Type X Mask 1 | This register selects the bytes in the second 16 bytes of the packet (bytes 17 through 32) that will be used for CRC calculation.<br>For each bit in this register,<br>1 = Byte is selected for CRC calculation<br>0 = Byte is not selected for CRC calculation<br>The register-bit to packet-byte mapping is as follows:<br>Bit [15]: byte-32<br>... : ...<br>Bit [1]: byte-18<br>Bit [0]: byte-17 | RW | 0000_0000_0000_0000 |
| **MMD Address 1Fh, Register 3h – Wake-On-LAN – Customized Packet, Type 0, Mask 2<br>MMD Address 1Fh, Register 9h – Wake-On-LAN – Customized Packet, Type 1, Mask 2<br>MMD Address 1Fh, Register Fh – Wake-On-LAN – Customized Packet, Type 2, Mask 2<br>MMD Address 1Fh, Register 15h – Wake-On-LAN – Customized Packet, Type 3, Mask 2** | | | | |
| 1F.3.15:0<br>1F.9.15:0<br>1F.F.15:0<br>1F.15.15:0 | Custom Packet Type X Mask 2 | This register selects the bytes in the third 16 bytes of the packet (bytes 33 through 48) that will be used for CRC calculation.<br>For each bit in this register,<br>1 = Byte is selected for CRC calculation<br>0 = Byte is not selected for CRC calculation<br>The register-bit to packet-byte mapping is as follows:<br>Bit [15]: byte-48<br>... : ...<br>Bit [1]: byte-34<br>Bit [0]: byte-33 | RW | 0000_0000_0000_0000 |

**TABLE 4-6: MMD REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode | Default |
|---|---|---|---|---|
| **MMD Address 1Fh, Register 4h – Wake-On-LAN – Customized Packet, Type 0, Mask 3<br>MMD Address 1Fh, Register Ah – Wake-On-LAN – Customized Packet, Type 1, Mask 3<br>MMD Address 1Fh, Register 10h – Wake-On-LAN – Customized Packet, Type 2, Mask 3<br>MMD Address 1Fh, Register 16h – Wake-On-LAN – Customized Packet, Type 3, Mask 3** | | | | |
| 1F.4.15:0<br>1F.A.15:0<br>1F.10.15:0<br>1F.16.15:0 | Custom Packet Type X Mask 3 | This register selects the bytes in the fourth 16 bytes of the packet (bytes 49 through 64) that will be used for CRC calculation.<br>For each bit in this register,<br>1 = Byte is selected for CRC calculation<br>0 = Byte is not selected for CRC calculation<br>The register-bit to packet-byte mapping is as follows:<br>Bit [15]: byte-64<br>... : ...<br>Bit [1]: byte-50<br>Bit [0]: byte-49 | RW | 0000_0000_0000_0000 |
| **MMD Address 1Fh, Register 5h – Wake-On-LAN – Customized Packet, Type 0, Expected CRC 0<br>MMD Address 1Fh, Register Bh – Wake-On-LAN – Customized Packet, Type 1, Expected CRC 0<br>MMD Address 1Fh, Register 11h – Wake-On-LAN – Customized Packet, Type 2, Expected CRC 0<br>MMD Address 1Fh, Register 17h – Wake-On-LAN – Customized Packet, Type 3, Expected CRC 0** | | | | |
| 1F.5.15:0<br>1F.B.15:0<br>1F.11.15:0<br>1F.17.15:0 | Custom Packet Type X CRC 0 | This register stores the lower two bytes for the expected CRC.<br>Bit [15:8] = Byte 2 (CRC [15:8])<br>Bit [7:0] = Byte 1 (CRC [7:0])<br>The upper two bytes for the expected CRC are stored in the following register. | RW | 0000_0000_0000_0000 |
| **MMD Address 1Fh, Register 6h – Wake-On-LAN – Customized Packet, Type 0, Expected CRC 1<br>MMD Address 1Fh, Register Ch – Wake-On-LAN – Customized Packet, Type 1, Expected CRC 1<br>MMD Address 1Fh, Register 12h – Wake-On-LAN – Customized Packet, Type 2, Expected CRC 1<br>MMD Address 1Fh, Register 18h – Wake-On-LAN – Customized Packet, Type 3, Expected CRC 1** | | | | |
| 1F.6.15:0<br>1F.C.15:0<br>1F.12.15:0<br>1F.18.15:0 | Custom Packet Type X CRC 1 | This register stores the upper two bytes for the expected CRC.<br>Bit [15:8] = Byte 4 (CRC [31:24])<br>Bit [7:0] = Byte 3 (CRC [23:16])<br>The lower two bytes for the expected CRC are stored in the previous register. | RW | 0000_0000_0000_0000 |
| **MMD Address 1Fh, Register 19h – Wake-On-LAN – Magic Packet, MAC-DA-0** | | | | |
| 1F.19.15:0 | Magic Packet MAC-DA-0 | This register stores the lower two bytes of the destination MAC address for the magic packet.<br>Bit [15:8] = Byte 2 (MAC Address [15:8])<br>Bit [7:0] = Byte 1 (MAC Address [7:0])<br>The upper four bytes of the destination MAC address are stored in the following two registers. | RW | 0000_0000_0000_0000 |
| **MMD Address 1Fh, Register 1Ah – Wake-On-LAN – Magic Packet, MAC-DA-1** | | | | |
| 1F.1A.15:0 | Magic Packet MAC-DA-1 | This register stores the middle two bytes of the destination MAC address for the magic packet.<br>Bit [15:8] = Byte 4 (MAC Address [31:24])<br>Bit [7:0] = Byte 3 (MAC Address [23:16])<br>The lower two bytes and upper two bytes of the destination MAC address are stored in the previous and following registers, respectively. | RW | 0000_0000_0000_0000 |

**TABLE 4-6: MMD REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode | Default |
|---|---|---|---|---|
| **MMD Address 1Fh, Register 1Bh – Wake-On-LAN – Magic Packet, MAC-DA-2** | | | | |
| 1F.1B.15:0 | Magic Packet MAC-DA-2 | This register stores the upper two bytes of the destination MAC address for the magic packet.<br>Bit [15:8] = Byte 6 (MAC Address [47:40])<br>Bit [7:0] = Byte 5 (MAC Address [39:32])<br>The lower four bytes of the destination MAC address are stored in the previous two registers. | RW | 0000_0000_0000_0000 |

**Note 4-1** RW = Read/Write; RO = Read Only; LH = Latch High.

# 5.0 OPERATIONAL CHARACTERISTICS

## 5.1 Absolute Maximum Ratings*

Supply Voltage ($V_{IN}$)

($V_{DD\_1.2}$) ..... –0.5V to +1.8V

($V_{DDIO}$, $V_{DDA\_3.3}$) ..... –0.5V to +5.0V

Input Voltage (all inputs) ..... –0.5V to +5.0V

Output Voltage (all outputs) ..... –0.5V to +5.0V

Lead Temperature (soldering, 10s) ..... +260°C

Storage Temperature ($T_S$) ..... –55°C to +150°C

*Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

## 5.2 Operating Ratings**

Supply Voltage

($V_{DDIO\_3.3}$, $V_{DDA\_3.3}$) ..... +3.135V to +3.465V

($V_{DDIO\_2.5}$) ..... +2.375V to +2.625V

($V_{DDIO\_1.8}$) ..... +1.710V to +1.890V

Ambient Temperature

($T_A$ Commercial) ..... 0°C to +70°C

($T_A$ Industrial) ..... –40°C to +85°C

Maximum Junction Temperature ($T_J$ max.) ..... +125°C

Thermal Resistance ($\Theta_{JA}$) ..... +76C/W

Thermal Resistance ($\Theta_{JC}$) ..... +15°C/W

**The device is not guaranteed to function outside its operating ratings.

| **Note:** | Do not drive input signals without power supplied to the device. |
|---|---|

## 6.0 ELECTRICAL CHARACTERISTICS

$T_A$ = 25°C. Specification is for packaged product only.

**TABLE 6-1: ELECTRICAL CHARACTERISTICS**

| Parameters | Symbol | Min. | Typ. | Max. | Units | Note |
|---|---|---|---|---|---|---|
| **Supply Current ($V_{DDIO}$, $V_{DDA\_3.3}$ = 3.3V), Note 6-1** | | | | | | |
| 10BASE-T | $I_{DD1\_3.3V}$ | — | 41 | — | mA | Full-duplex traffic @ 100% utilization |
| 100BASE-TX | $I_{DD2\_3.3V}$ | — | 47 | — | mA | Full-duplex traffic @ 100% utilization |
| EEE (100 Mbps) Mode | $I_{DD3\_3.3V}$ | — | 23 | — | mA | TX and RX paths in LPI state with no traffic |
| EDPD Mode | $I_{DD4\_3.3V}$ | — | 20 | — | mA | Ethernet cable disconnected (Reg. 18h.11 = 0) |
| Power-Down Mode | $I_{DD5\_3.3V}$ | — | 4 | — | mA | Software power-down (Reg. 0h.11 = 1) |
| **CMOS Level Inputs** | | | | | | |
| Input High Voltage | $V_{IH}$ | 2.0 | — | — | V | $V_{DDIO}$ = 3.3V |
| | | 1.8 | — | — | V | $V_{DDIO}$ = 2.5V |
| | | 1.3 | — | — | V | $V_{DDIO}$ = 1.8V |
| Input Low Voltage | $V_{IL}$ | — | — | 0.8 | V | $V_{DDIO}$ = 3.3V |
| | | — | — | 0.7 | V | $V_{DDIO}$ = 2.5V |
| | | — | — | 0.5 | V | $V_{DDIO}$ = 1.8V |
| Input Current | $\|I_{IN}\|$ | — | — | 10 | µA | $V_{IN}$ = GND ~ $V_{DDIO}$ |
| **CMOS Level Outputs** | | | | | | |
| Output High Voltage | $V_{OH}$ | 2.4 | — | — | V | $V_{DDIO}$ = 3.3V |
| | | 2.0 | — | — | V | $V_{DDIO}$ = 2.5V |
| | | 1.5 | — | — | V | $V_{DDIO}$ = 1.8V |
| Output Low Voltage | $V_{OL}$ | — | — | 0.4 | V | $V_{DDIO}$ = 3.3V |
| | | — | — | 0.4 | V | $V_{DDIO}$ = 2.5V |
| | | — | — | 0.3 | V | $V_{DDIO}$ = 1.8V |
| Output Tri-State Leakage | $\|I_{OZ}\|$ | — | — | 10 | µA | — |
| **LED Output** | | | | | | |
| Output Drive Current | $I_{LED}$ | — | 8 | — | mA | Each LED pin (LED0, LED1) |
| **All Pull-Up/Pull-Down Pins (including Strap-In Pins)** | | | | | | |
| Internal Pull-Up Resistance | pu | 30 | 45 | 73 | kΩ | $V_{DDIO}$ = 3.3V |
| | | 39 | 61 | 102 | kΩ | $V_{DDIO}$ = 2.5V |
| | | 48 | 99 | 178 | kΩ | $V_{DDIO}$ = 1.8V |
| Internal Pull-Down Resistance | pd | 26 | 43 | 79 | kΩ | $V_{DDIO}$ = 3.3V |
| | | 34 | 59 | 113 | kΩ | $V_{DDIO}$ = 2.5V |
| | | 53 | 99 | 200 | kΩ | $V_{DDIO}$ = 1.8V |
| **100BASE-TX Transmit (measured differentially after 1:1 transformer)** | | | | | | |
| Peak Differential Output Voltage | $V_O$ | 0.95 | — | 1.05 | V | 100Ω termination across differential output |
| Output Voltage Imbalance | $V_{IMB}$ | — | — | 2 | % | 100Ω termination across differential output |
| Rise/Fall Time | $t_r/t_f$ | 3 | — | 5 | ns | — |
| Rise/Fall Time Imbalance | — | 0 | — | 0.5 | ns | — |
| Duty Cycle Distortion | — | — | — | ±0.25 | ns | — |
| Overshoot | — | — | — | 5 | % | — |

**TABLE 6-1: ELECTRICAL CHARACTERISTICS (CONTINUED)**

| Parameters | Symbol | Min. | Typ. | Max. | Units | Note |
|---|---|---|---|---|---|---|
| Output Jitter | — | — | 0.7 | — | ns | Peak-to-peak |
| **10BASE-T Transmit (measured differentially after 1:1 transformer)** | | | | | | |
| Peak Differential Output Voltage | $V_P$ | 2.2 | — | 2.8 | V | 100Ω termination across differential output |
| Jitter Added | — | — | — | 3.5 | ns | Peak-to-peak |
| Rise/Fall Time | $t_r/t_f$ | — | 25 | — | ns | — |
| **10BASE-T Receive** | | | | | | |
| Squelch Threshold | $V_{SQ}$ | — | 400 | — | mV | 5 MHz square wave |
| **Transmitter - Drive Setting** | | | | | | |
| Reference Voltage of $I_{SET}$ | $V_{SET}$ | — | 0.65 | — | V | $R(I_{SET})$ = 6.49 kΩ |
| **100 Mbps Mode - Industrial Applications Parameters** | | | | | | |
| Clock Phase Delay – XI Input to MII TXC Output | — | 15 | 20 | 25 | ns | XI (25 MHz clock input) to MII TXC (25 MHz clock output) delay, referenced to rising edges of both clocks. |
| Link Loss Reaction (Indication) Time | $t_{llr}$ | — | 4.4 | — | µs | Link loss detected at receive differential inputs to PHY signal indication time for each of the following:<br>1. For LED mode 00, Speed LED output changes from low (100 Mbps) to high (10 Mbps, default state for link-down).<br>2. For LED mode 01, Link LED output changes from low (link-up) to high (link-down).<br>3. INTRP pin asserts for link-down status change. |

**Note 6-1** Current consumption is for the single 3.3V supply KSZ8091MLX device only, and includes the transmit driver current and the 1.2V supply voltage ($V_{DD\_1.2}$) that are supplied by the KSZ8091MLX.

## 7.0 TIMING DIAGRAMS

### 7.1 MII SQE Timing (10BASE-T)

**FIGURE 7-1: MII SQE TIMING (10BASE-T)**

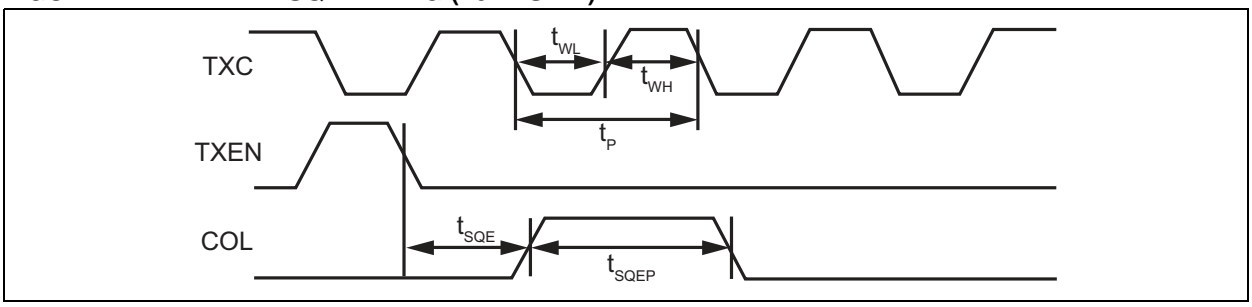



**TABLE 7-1: MII SQE TIMING (10BASE-T) PARAMETERS**

| Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_P$ | TXC period | — | 400 | — | ns |
| $t_{WL}$ | TXC pulse width low | — | 200 | — | ns |
| $t_{WH}$ | TXC pulse width high | — | 200 | — | ns |
| $t_{SQE}$ | COL (SQE) delay after TXEN de-asserted | — | 2.2 | — | µs |
| $t_{SQEP}$ | COL (SQE) pulse duration | — | 1.0 | — | µs |

## 7.2 MII Transmit Timing (10BASE-T)

**FIGURE 7-2: MII TRANSMIT TIMING (10BASE-T)**

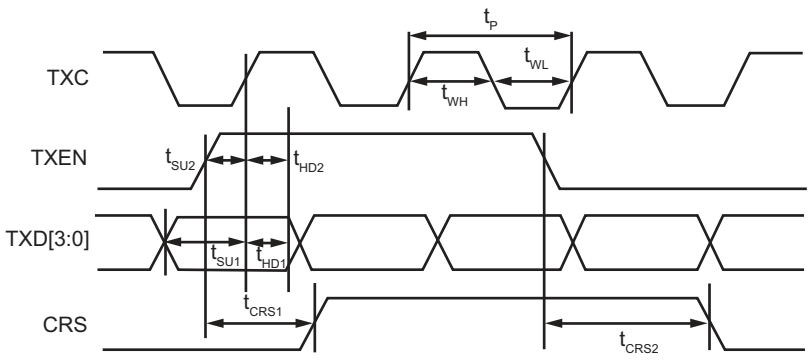



**TABLE 7-2: MII TRANSMIT TIMING (10BASE-T) PARAMETERS**

| Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_P$ | TXC period | — | 400 | — | ns |
| $t_{WL}$ | TXC pulse width low | — | 200 | — | ns |
| $t_{WH}$ | TXC pulse width high | — | 200 | — | ns |
| $t_{SU1}$ | TXD[3:0] setup to rising edge of TXC | 120 | — | — | ns |
| $t_{SU2}$ | TXEN setup to rising edge of TXC | 120 | — | — | ns |
| $t_{HD1}$ | TXD[3:0] hold from rising edge of TXC | 0 | — | — | ns |
| $t_{HD2}$ | TXEN hold from rising edge of TXC | 0 | — | — | ns |
| $t_{CRS1}$ | TXEN high to CRS asserted latency | — | 600 | — | ns |
| $t_{CRS2}$ | TXEN low to CRS de-asserted latency | — | 1.0 | — | µs |

## 7.3 MII Receive Timing (10BASE-T)

**FIGURE 7-3: MII RECEIVE TIMING (10BASE-T)**

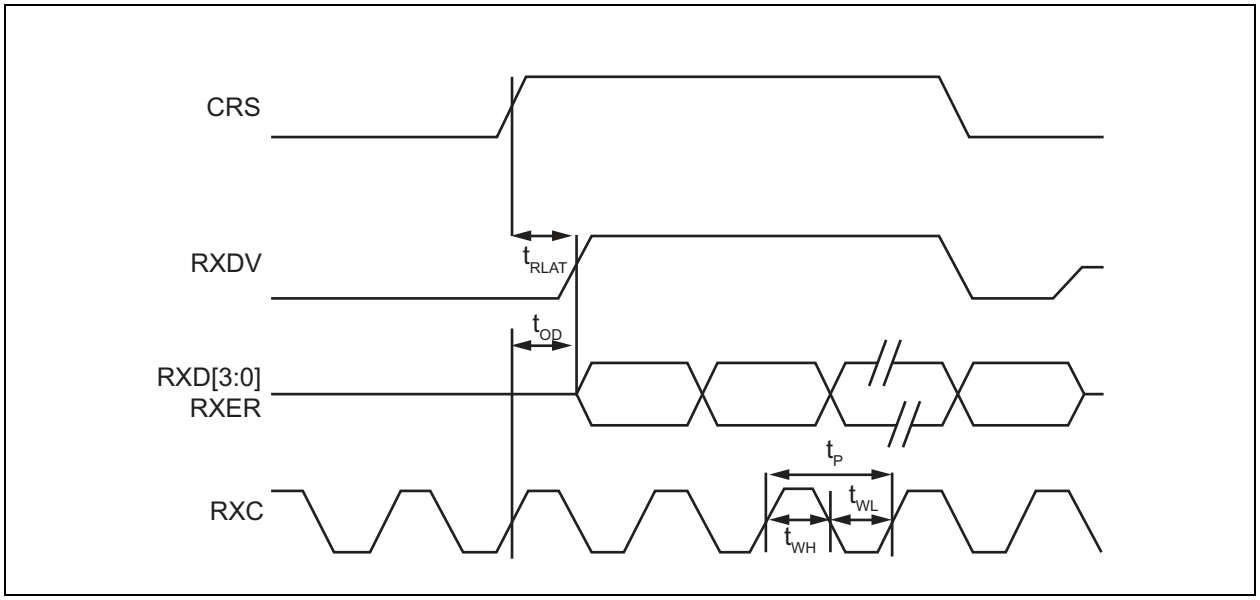



**TABLE 7-3: MII RECEIVE TIMING (10BASE-T) PARAMETERS**

| Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_P$ | RXC period | — | 400 | — | ns |
| $t_{WL}$ | RXC pulse width low | — | 200 | — | ns |
| $t_{WH}$ | RXC pulse width high | — | 200 | — | ns |
| $t_{OD}$ | (RXDV, RXD[3:0], RXER) output delay from rising edge of RXC | — | 205 | — | ns |
| $t_{RLAT}$ | CRS to (RXDV, RXD[3:0]) latency | — | 7.2 | — | µs |

## 7.4 MII Transmit Timing (100BASE-TX)

**FIGURE 7-4: MII TRANSMIT TIMING (100BASE-TX)**

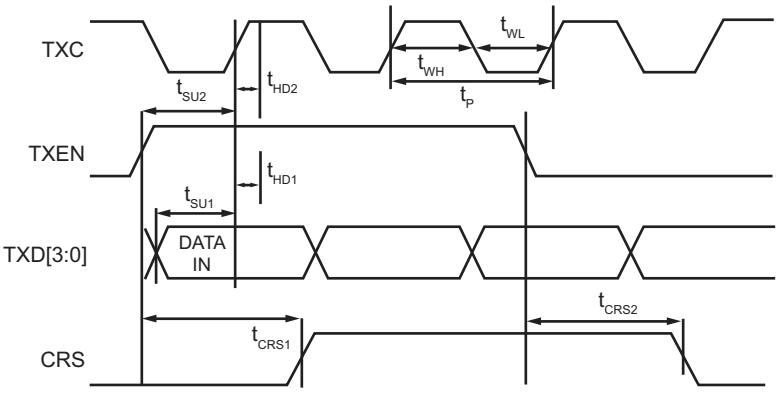



**TABLE 7-4: MII TRANSMIT TIMING (100BASE-TX) PARAMETERS**

| Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_P$ | TXC period | — | 40 | — | ns |
| $t_{WL}$ | TXC pulse width low | — | 20 | — | ns |
| $t_{WH}$ | TXC pulse width high | — | 20 | — | ns |
| $t_{SU1}$ | TXD[3:0] setup to rising edge of TXC | 10 | — | — | ns |
| $t_{SU2}$ | TXEN setup to rising edge of TXC | 10 | — | — | ns |
| $t_{HD1}$ | TXD[3:0] hold from rising edge of TXC | 0 | — | — | ns |
| $t_{HD2}$ | TXEN hold from rising edge of TXC | 0 | — | — | ns |
| $t_{CRS1}$ | TXEN high to CRS asserted latency | — | 72 | — | ns |
| $t_{CRS2}$ | TXEN low to CRS de-asserted latency | — | 72 | — | ns |

## 7.5 MII Receive Timing (100BASE-TX)

**FIGURE 7-5: MII RECEIVE TIMING (100BASE-TX)**

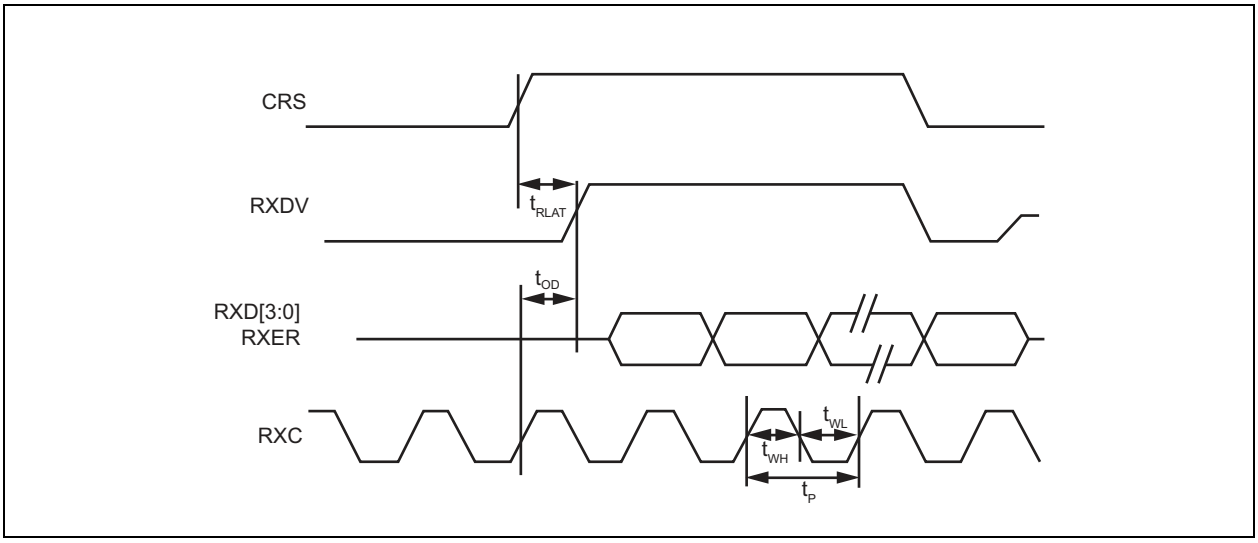



**TABLE 7-5: MII RECEIVE TIMING (100BASE-TX) PARAMETERS**

| Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_P$ | RXC period | — | 40 | — | ns |
| $t_{WL}$ | RXC pulse width low | — | 20 | — | ns |
| $t_{WH}$ | RXC pulse width high | — | 20 | — | ns |
| $t_{OD}$ | (RXDV, RXD[3:0], RXER) output delay from rising edge of RXC | 16 | 21 | 25 | ns |
| $t_{RLAT}$ | CRS to (RXDV, RXD[3:0]) latency | — | 170 | — | ns |

## 7.6 Auto-Negotiation Timing

**FIGURE 7-6: AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING**

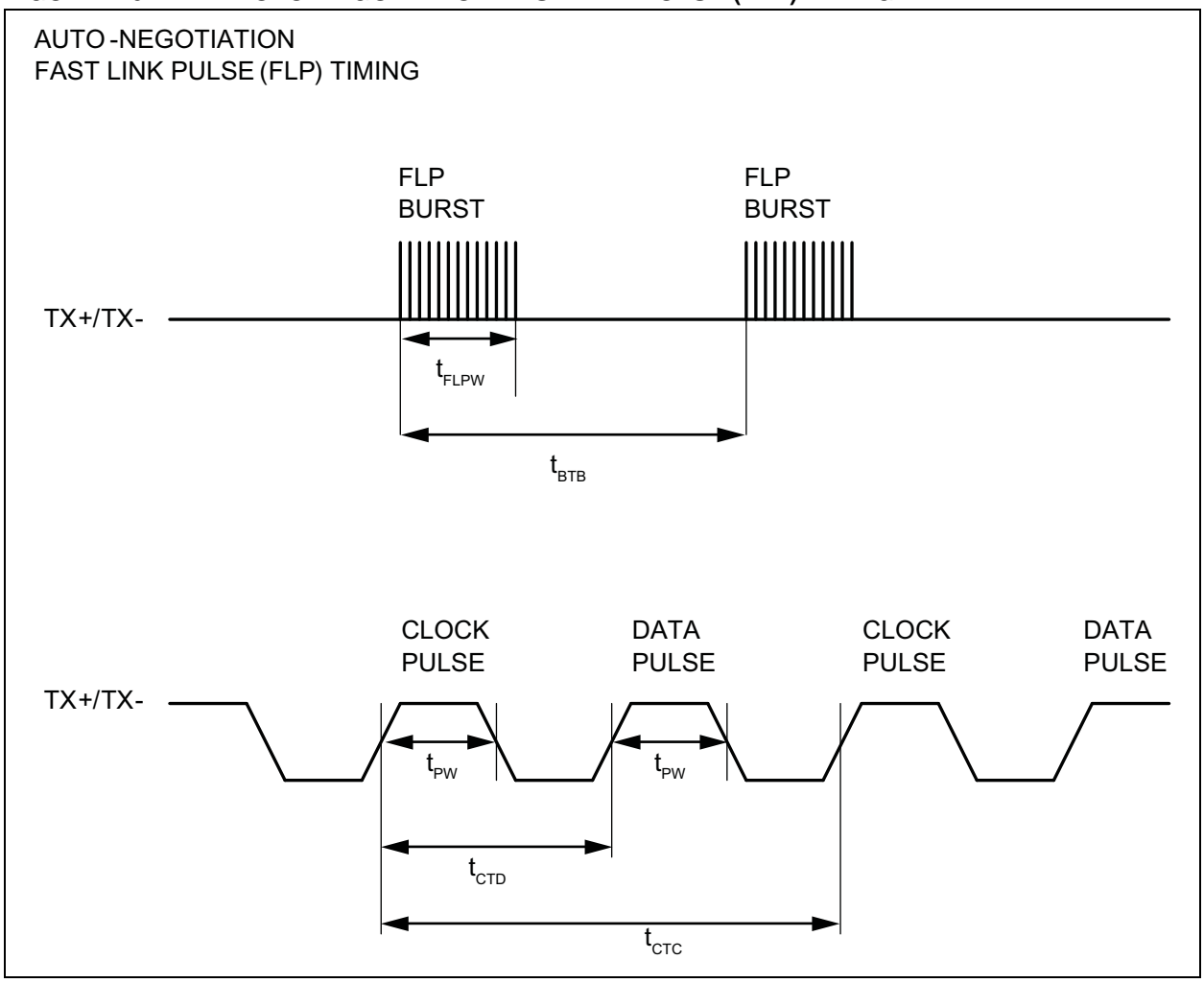



**TABLE 7-6: AUTO-NEGOTIATION FAST LINK PULSE TIMING PARAMETERS**

| Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{BTB}$ | FLP burst to FLP burst | 8 | 16 | 24 | ms |
| $t_{FLPW}$ | FLP burst width | — | 2 | — | ms |
| $t_{PW}$ | Clock/Data pulse width | — | 100 | — | ns |
| $t_{CTD}$ | Clock pulse to data pulse | 55.5 | 64 | 69.5 | µs |
| $t_{CTC}$ | Clock pulse to clock pulse | 111 | 128 | 139 | µs |
| — | Number of clock/data pulses per FLP burst | 17 | — | 33 | — |

## 7.7 MDC/MDIO Timing

**FIGURE 7-7: MDC/MDIO TIMING**

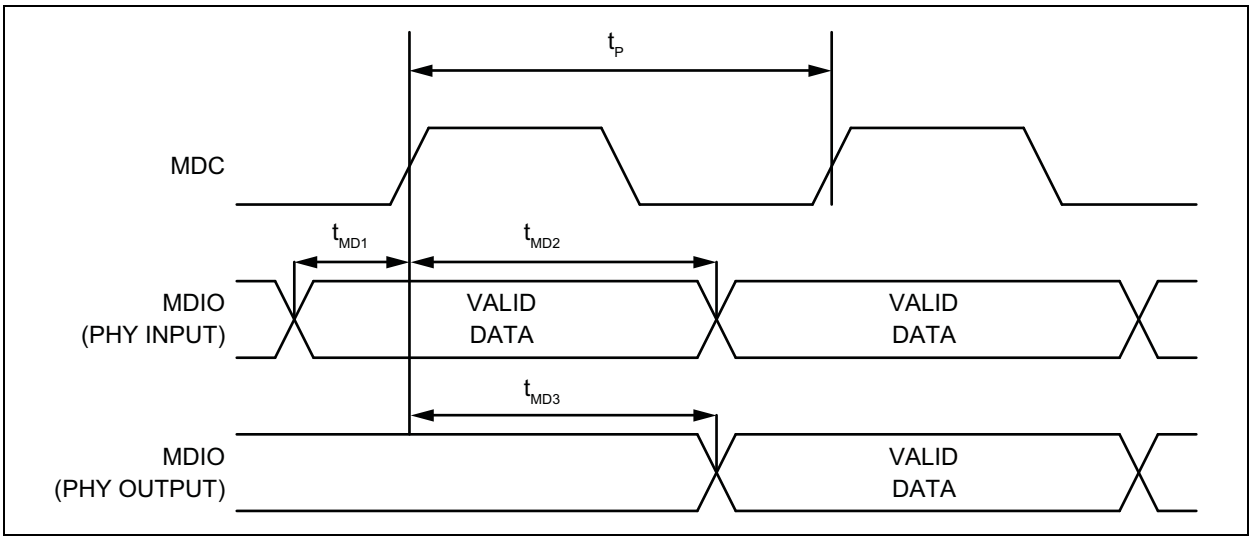



**TABLE 7-7: MDC/MDIO TIMING PARAMETERS**

| Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_c$ | MDC Clock Frequency | — | 2.5 | 10 | MHz |
| $t_P$ | MDC period | — | 400 | — | ns |
| $t_{MD1}$ | MDIO (PHY input) setup to rising edge of MDC | 10 | — | — | ns |
| $t_{MD2}$ | MDIO (PHY input) hold from rising edge of MDC | 4 | — | — | ns |
| $t_{MD3}$ | MDIO (PHY output) delay from rising edge of MDC | 5 | 222 | — | ns |

## 7.8 Power-Up/Reset Timing

The KSZ8091MLX reset timing requirement is summarized in Figure 7-8 and Table 7-8.

**FIGURE 7-8: POWER-UP/RESET TIMING**

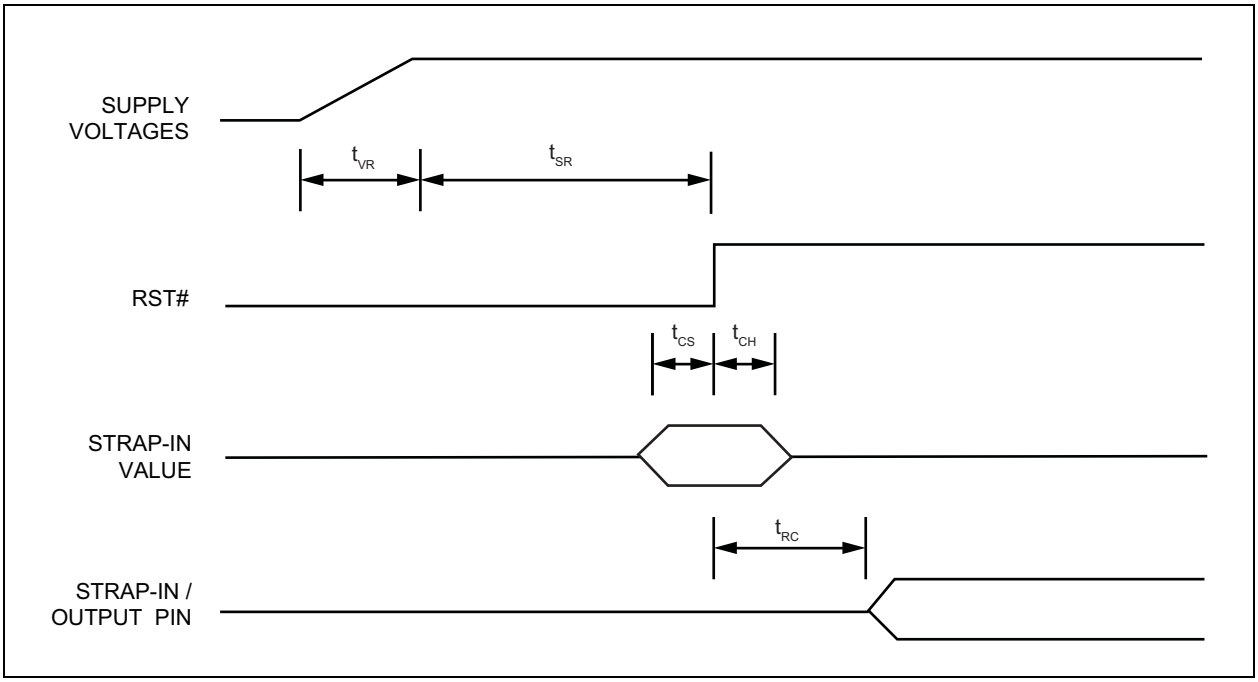



**TABLE 7-8: POWER-UP/RESET TIMING PARAMETERS**

| Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{VR}$ | Supply voltage ($V_{DDIO}$, $V_{DDA\_3.3}$) rise time | 300 | — | — | µs |
| $t_{SR}$ | Stable supply voltage ($V_{DDIO}$, $V_{DDA\_3.3}$) to reset high | 10 | — | — | ms |
| $t_{CS}$ | Configuration setup time | 5 | — | — | ns |
| $t_{CH}$ | Configuration hold time | 5 | — | — | ns |
| $t_{RC}$ | Reset to strap-in pin output | 6 | — | — | ns |

The supply voltage ($V_{DDIO}$ and $V_{DDA\_3.3}$) power-up waveform should be monotonic. The 300 µs minimum rise time is from 10% to 90%.

For warm reset, the reset (RST#) pin should be asserted low for a minimum of 500 µs. The strap-in pin values are read and updated at the de-assertion of reset.

After the de-assertion of reset, wait a minimum of 100 µs before starting programming on the MIIM (MDC/MDIO) interface.

## 8.0 RESET CIRCUIT

Figure 8-1 shows a reset circuit recommended for powering up the KSZ8091MLX if reset is triggered by the power supply.

**FIGURE 8-1: RECOMMENDED RESET CIRCUIT**

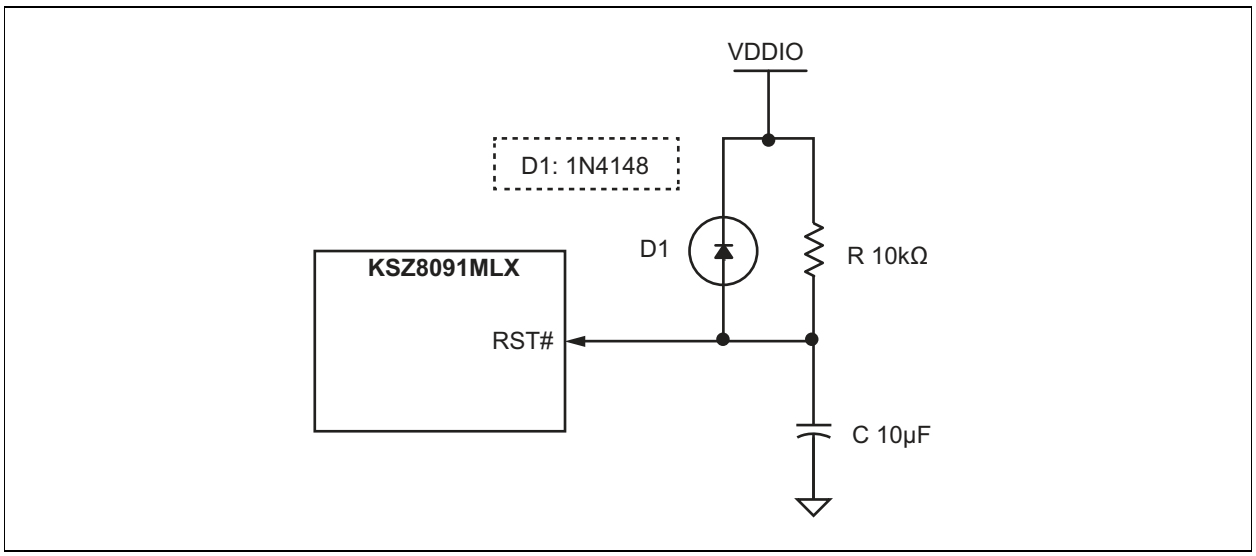
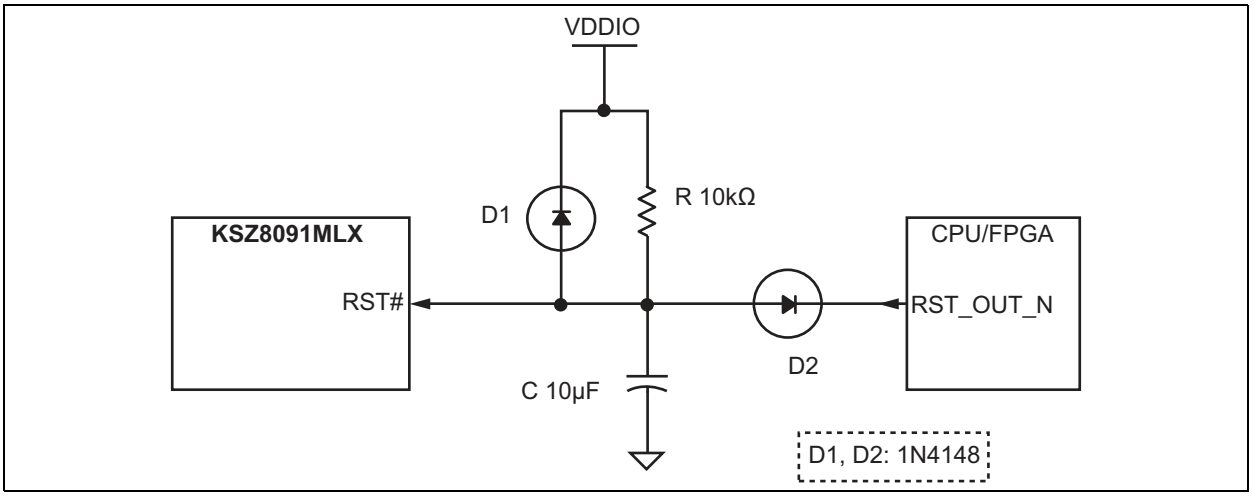



Figure 8-2 shows a reset circuit recommended for applications where reset is driven by another device (for example, the CPU or an FPGA). The reset out RST_OUT_n from CPU/FPGA provides the warm reset after power up reset. D2 is used if using different $V_{DDIO}$ between the switch and CPU/FPGA, otherwise, the different $V_{DDIO}$ will fight each other. If different $V_{DDIO}$ have to use in a special case, a low $V_F$ (<0.3V) diode is required (for example, Vishay's BAT54, MSS1P2L and so on), or a level shifter device can be used too. If Ethernet device and CPU/FPGA use same $V_{DDIO}$ voltage, D2 can be removed to connect both devices directly. Usually, Ethernet device and CPU/FPGA should use same $V_{DDIO}$ voltage.

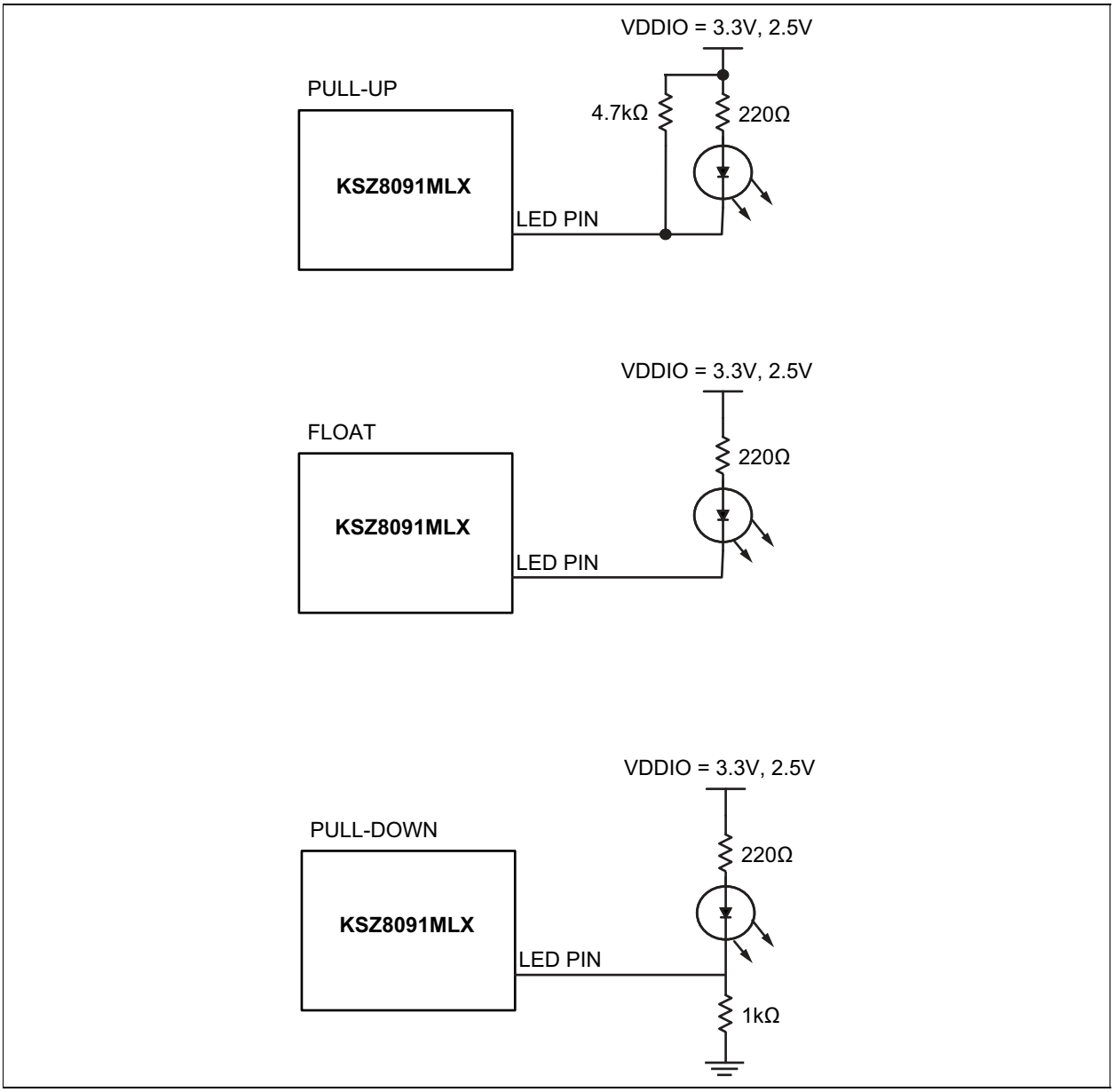
**FIGURE 8-2: RECOMMENDED RESET CIRCUIT FOR CPU/FPGA RESET OUTPUT**



## 9.0 REFERENCE CIRCUITS — LED STRAP-IN PINS

The pull-up, float, and pull-down reference circuits for the LED1/SPEED and LED0/PME_N1/NWAYEN strap-in pins are shown in Figure 9-1 for 3.3V and 2.5V $V_{DDIO}$.

**FIGURE 9-1: REFERENCE CIRCUITS FOR LED STRAP-IN PINS**




For 1.8V $V_{DDIO}$, LED indication support is not recommended due to the low voltage. Without the LED indicator, the SPEED and NWAYEN strap-in pins are functional with a 4.7 kΩ pull-up to 1.8V $V_{DDIO}$ or float for a value of '1', and with a 1.0 kΩ pull-down to ground for a value of '0'.

If using RJ45 jacks with integrated LEDs and 1.8V $V_{DDIO}$, a level shifting is required from LED 3.3V to 1.8V. For example, use a bipolar transistor or a level shift device.

## 10.0 REFERENCE CLOCK - CONNECTION AND SELECTION

A crystal or external clock source, such as an oscillator, is used to provide the reference clock for the KSZ8091MLX.

For the KSZ8091MLX in all operating modes, the reference clock is 25 MHz. The crystal/reference clock connections to XI (Pin 15) and XO (Pin 14), and the crystal/reference clock selection criteria, are provided in Figure 10-1 and Table 10-1.

**FIGURE 10-1: 25 MHZ CRYSTAL/OSCILLATOR REFERENCE CLOCK CONNECTION**

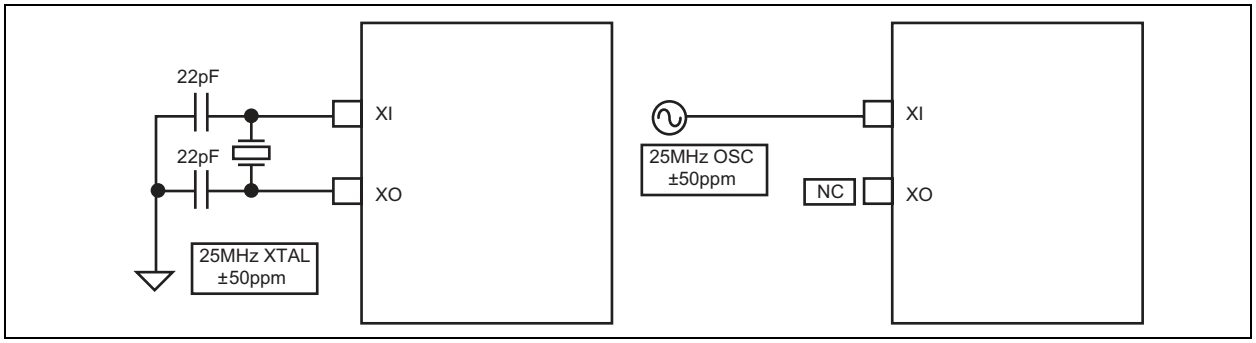



**TABLE 10-1: 25 MHZ CRYSTAL/REFERENCE CLOCK SELECTION CRITERIA**

| Characteristics | Value |
|---|---|
| Frequency | 25 MHz |
| Frequency Tolerance (max.); Note 10-1 | ±50 ppm |
| Crystal Series Resistance (typ.) | 40Ω |
| Crystal Load Capacitance (typ.) | 16 pF |

**Note 10-1** ±60 ppm for overtemperature crystal.

## 11.0 MAGNETIC - CONNECTION AND SELECTION

A 1:1 isolation transformer is required at the line interface. Use one with integrated common-mode chokes for designs exceeding FCC requirements.

The KSZ8091MLX design incorporates voltage-mode transmit drivers and on-chip terminations.

With the voltage-mode implementation, the transmit drivers supply the common-mode voltages to the two differential pairs. Therefore, the two transformer center tap pins on the KSZ8091MLX side should not be connected to any power supply source on the board; instead, the center tap pins should be separated from one another and connected through separate 0.1 µF common-mode capacitors to ground. Separation is required because the common-mode voltage is different between transmitting and receiving differential pairs.

Figure 11-1 shows the typical magnetic interface circuit for the KSZ8091MLX.

**FIGURE 11-1: TYPICAL MAGNETIC INTERFACE CIRCUIT**

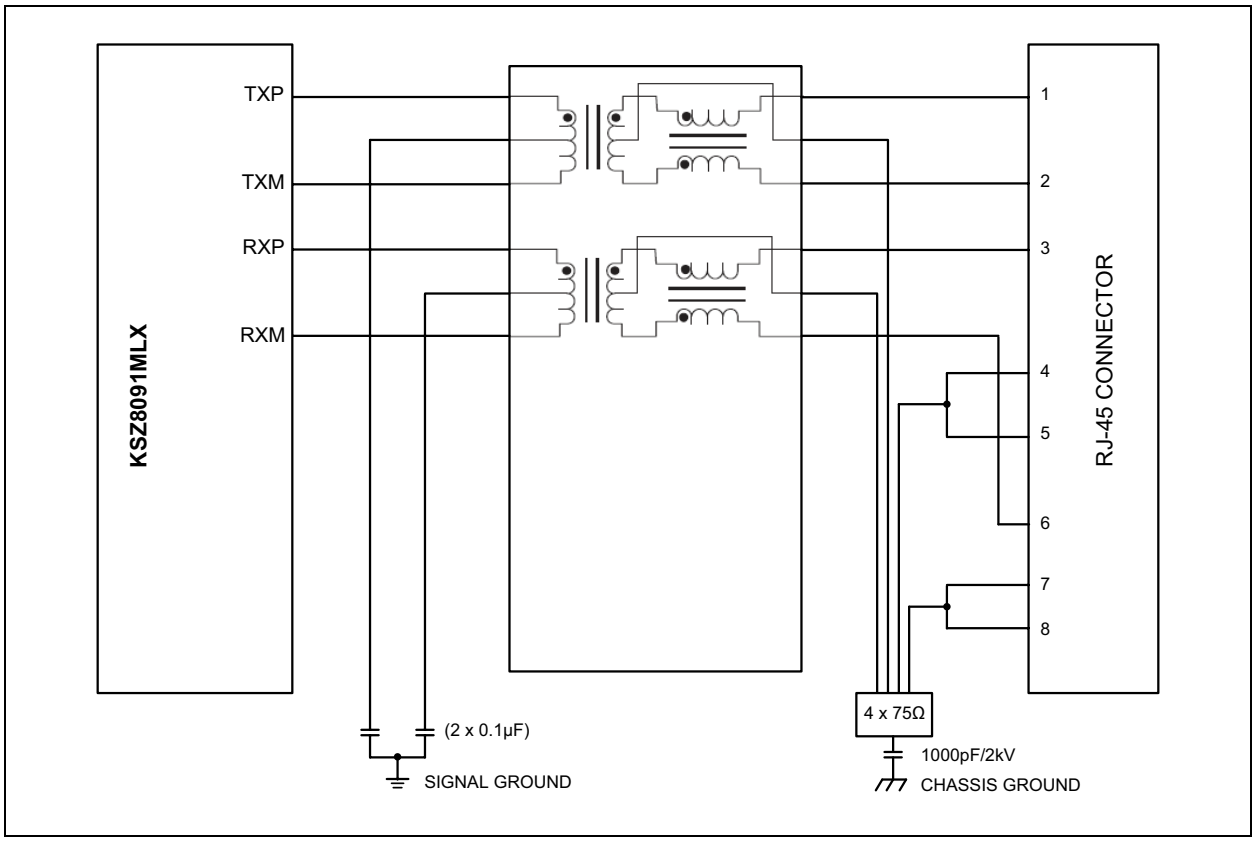



Table 11-1 lists recommended magnetic characteristics.

**TABLE 11-1: MAGNETICS SELECTION CRITERIA**

| Parameter | Value | Test Conditions |
|---|---|---|
| Turns Ratio | 1 CT : 1 CT | — |
| Open-Circuit Inductance (min.) | 350 µH | 100 mV, 100 kHz, 8 mA |
| Insertion Loss (max.) | –1.1 dB | 100 kHz to 100 MHz |
| HIPOT (min.) | 1500 $V_{RMS}$ | — |

Table 11-2 is a list of compatible single-port magnetics with separated transformer center tap pins on the PHY chip side that can be used with the KSZ8091MLX.

**TABLE 11-2: COMPATIBLE SINGLE-PORT 10/100 MAGNETICS**

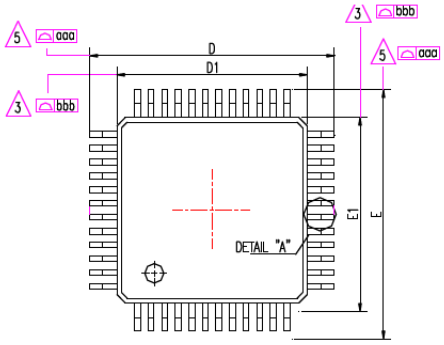
| Manufacturer | Part Number | Temperature Range | Magnetic + RJ-45 |
|---|---|---|---|
| Bel Fuse | S558-5999-U7 | 0°C to 70°C | No |
| Bel Fuse | SI-46001-F | 0°C to 70°C | Yes |
| Bel Fuse | SI-50170-F | 0°C to 70°C | Yes |
| Delta | LF8505 | 0°C to 70°C | No |
| HALO | HFJ11-2450E | 0°C to 70°C | Yes |
| HALO | TG110-E055N5 | –40°C to 85°C | No |
| LANKom | LF-H41S-1 | 0°C to 70°C | No |
| Pulse | H1102 | 0°C to 70°C | No |
| Pulse | H1260 | 0°C to 70°C | No |
| Pulse | HX1188 | –40°C to 85°C | No |
| Pulse | J00-0014 | 0°C to 70°C | Yes |
| Pulse | JX0011D21NL | –40°C to 85°C | Yes |
| TDK | TLA-6T718A | 0°C to 70°C | Yes |
| Transpower | HB726 | 0°C to 70°C | No |
| Wurth/Midcom | 000-7090-37R-LF1 | –40°C to 85°C | No |

## 12.0 PACKAGE OUTLINE

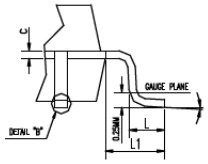
**FIGURE 12-1: 48-LEAD LQFP 7 MM X 7 MM PACKAGE**

**TITLE**
48 LEAD LQFP 7x7mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

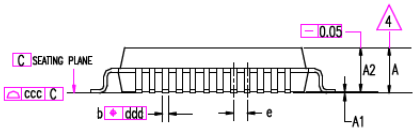
| | | | |
|---|---|---|---|
| **DRAWING #** | LQFP7x7-48LD-PL-5 | **UNIT** | MM [INCHES] |
| **Lead Frame** | Copper Alloy | **Lead Finish** | Matte Tin |



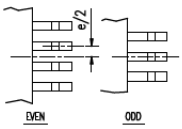

TOP VIEW

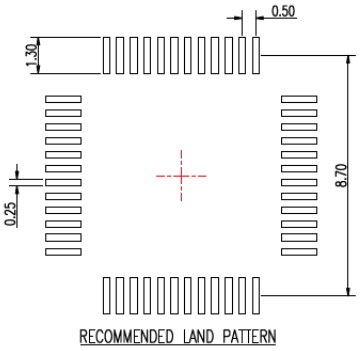



SIDE VIEW 1

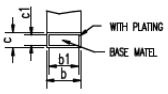



SIDE VIEW 2




RECOMMENDED LAND PATTERN




| SYMBOL | DIMENSION IN MM | | |
|---|---|---|---|
| | MIN. | NOM | MAX. |
| A | – | – | 1.60 |
| A1 | 0.05 | – | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| D | 9.00 BSC | | |
| D1 | 7.00 BSC | | |
| E | 9.00 BSC | | |
| E1 | 7.00 BSC | | |
| c | 0.09 | – | 0.20 |
| c1 | 0.09 | – | 0.16 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF. | | |
| θ | 0 | 3.5 | 7 |

| | b (MM) | | | b1 (MM) | | | e (MM) | | |
|---|---|---|---|---|---|---|---|---|---|
| N | MIN. | NOM | MAX. | MIN. | NOM | MAX. | MIN. | NOM | MAX. |
| 48L | 0.17 | 0.22 | 0.27 | 0.17 | 0.20 | 0.23 | 0.50 BSC. | | |

| TOLERANCE OF FORM AND POSITION | |
|---|---|
| aaa | 0.20 |
| bbb | 0.20 |
| ccc | 0.08 |
| ddd | 0.08 |

NOTES:
1. ALL DIMENSIONS ARE IN MM.
2. REFER TO JEDEC STANDARD MS-026 BBC.
3. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. "D1" AND "E1" ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
4. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
5. TO BE DETERMINED AT SEATING DATUM PLANE C.
6. "aaa" IS THE BILATERAL PROFILE TOLERANCE THAT CONTROLS THE POSITION OF THE PLASTIC BODY SIDES. THE CENTER OF THE PROFILE ZONES ARE DEFINED BY THE BASIC DIMENSIONS "D" AND "E".
7. "bbb" THE TOLERANCE THAT CONTROLS THE POSITION OF THE ENTIRE TERMINAL PATTERN WITH RESPECT TO DATUM'S A AND B. THE CENTER OF THE TOELRANCE ZONE FOR EACH TERMINAL IS DEFINED BY THE BASIC DIMENSION "e" RELATED TO DATUM A AND B.
8. "ccc" THE TOLERANCE RELATED TO THE SEATING PLANE IN WHICH THE TOP SURFACE OF THE PACKAGE MUST BE LOCATED.
9. "ddd" THE TOLERANCE THAT CONTROLS THE POSITION OF THE TERMINALS TO EACH OTHER. THE CENTER OF THE PROFILE ZONES ARE DETERMINED BY THE BASIC DIMENSION "e".
10. THIS DOCUMENT IS FOR AUTOMOTIVE PRODUCT USE ONLY.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

## APPENDIX A: DATA SHEET REVISION HISTORY

**TABLE A-1: REVISION HISTORY**

| Revision | Section/Figure/Entry | Correction |
|---|---|---|
| DS00002297A (11-03-16) | — | Converted Micrel data sheet KSZ8091MLX to Microchip DS00002297A. Minor text changes throughout. |
| | Table 2-1 | Added NAND_Tree statement for Pin 44 (TXER). |
| | **Section 3.9.1 "NAND Tree I/O Testing"** | Added TXER statement. |
| | Register 4h - Auto-Negotiation Advertisement | Changed default value to '1' for address 4.15. |

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| PART NO. | X | X | X | XX | — | XX |
|---|---|---|---|---|---|---|
| Device | Interface | Package | Special Attribute | Temperature | | Media Type |

| | |
|---|---|
| **Device:** | KSZ8091 |
| **Interface:** | M = MII |
| **Package:** | L = 48-Lead LQFP |
| **Special Attribute:** | X = None |
| **Temperature:** | CA = 0°C to +70°C (Commercial)<br>IA = –40°C to +85°C (Industrial) |
| **Media Type:** | blank = Tray<br>TR = Tape & Reel |

**Examples:**

a) KSZ8091MLXCA
MII Interface
48-Lead LQFP
No Special Attribute
Commercial Temperature
Tray

b) KSZ8091MLXIA
MII Interface
48-Lead LQFP
No Special Attribute
Industrial Temperature
Tray

c) KSZ8091MLXCA-TR
MII Interface
48-Lead LQFP
No Special Attribute
Commercial Temperature
Tape & Reel

d) KSZ8091MLXIA-TR
MII Interface
48-Lead LQFP
No Special Attribute
Industrial Temperature
Tape & Reel

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