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# FDD6796A / FDU6796A\_F071

## N-Channel PowerTrench<sup>®</sup> MOSFET

25 V, 5.7 mΩ

### Features

- Max  $r_{DS(on)}$  = 5.7 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 20\text{ A}$
- Max  $r_{DS(on)}$  = 15.0 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 15.2\text{ A}$
- 100% UIL tested
- RoHS Compliant

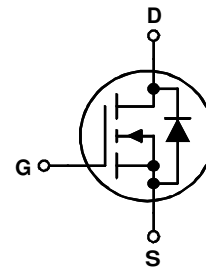
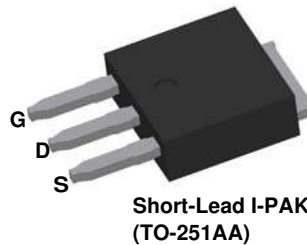
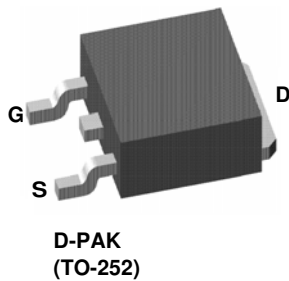


### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $r_{DS(on)}$  and fast switching speed.

### Applications

- Vcore DC-DC for Desktop Computers and Servers
- VRM for Intermediate Bus Architecture



### MOSFET Maximum Ratings $T_C = 25\text{ °C}$ unless otherwise noted

| Symbol         | Parameter  | Ratings     | Units |
|----------------|--|-------------|-------|
| $V_{DS}$       | Drain to Source Voltage  | 25          | V     |
| $V_{GS}$       | Gate to Source Voltage   | ±20         | V     |
| $I_D$          | Drain Current -Continuous (Package limited) $T_C = 25\text{ °C}$ | 40          | A     |
|                | -Continuous (Silicon limited) $T_C = 25\text{ °C}$               | 67          |       |
|                | -Continuous $T_A = 25\text{ °C}$ (Note 1a)                       | 20          |       |
|                | -Pulsed  | 150         |       |
| $E_{AS}$       | Single Pulse Avalanche Energy (Note 3)                           | 40          | mJ    |
| $P_D$          | Power Dissipation $T_C = 25\text{ °C}$                           | 42          | W     |
|                | Power Dissipation $T_A = 25\text{ °C}$ (Note 1a)                 | 3.7         |       |
| $T_J, T_{STG}$ | Operating and Storage Junction Temperature Range                 | -55 to +175 | °C    |

### Thermal Characteristics

|                 |   |     |      |
|-----------------|---|-----|------|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case              | 3.6 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 40  |      |

### Package Marking and Ordering Information

| Device Marking | Device        | Package        | Reel Size | Tape Width | Quantity   |
|----------------|---------------|----------------|-----------|------------|------------|
| FDD6796A       | FDD6796A      | D-PAK (TO-252) | 13"       | 16 mm      | 2500 units |
| FDU6796A       | FDU6796A_F071 | TO-251AA       | N/A(Tube) | N/A        | 75 units   |

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
|--------|-----------|-----------------|-----|-----|-----|-------|

### Off Characteristics

|                                      |   |   |    |    |           |               |
|--------------------------------------|---|---|----|----|-----------|---------------|
| $BV_{DSS}$                           | Drain to Source Breakdown Voltage         | $I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$                    | 25 |    |           | V             |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$ |    | 16 |           | mV/°C         |
| $I_{DSS}$                            | Zero Gate Voltage Drain Current           | $V_{DS} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$                            |    |    | 1         | $\mu\text{A}$ |
| $I_{GSS}$                            | Gate to Source Leakage Current            | $V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$                        |    |    | $\pm 100$ | nA            |

### On Characteristics

|  |  |  |     |      |      |            |
|--|--|--|-----|------|------|------------|
| $V_{GS(th)}$                           | Gate to Source Threshold Voltage                         | $V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$                               | 1.0 | 1.9  | 3.0  | V          |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$        |     | -6   |      | mV/°C      |
| $r_{DS(on)}$                           | Static Drain to Source On Resistance                     | $V_{GS} = 10\text{ V}$ , $I_D = 20\text{ A}$                                     |     | 4.3  | 5.7  | m $\Omega$ |
|  |  | $V_{GS} = 4.5\text{ V}$ , $I_D = 15.2\text{ A}$                                  |     | 11.1 | 15.0 |            |
|  |  | $V_{GS} = 10\text{ V}$ , $I_D = 20\text{ A}$ , $T_J = 150\text{ }^\circ\text{C}$ |     | 6.5  | 8.6  |            |
| $g_{FS}$                               | Forward Transconductance                                 | $V_{DS} = 5\text{ V}$ , $I_D = 20\text{ A}$                                      |     | 118  |      | S          |

### Dynamic Characteristics

|           |                              |  |  |      |      |          |
|-----------|------------------------------|--|--|------|------|----------|
| $C_{iss}$ | Input Capacitance            | $V_{DS} = 13\text{ V}$ , $V_{GS} = 0\text{ V}$ ,<br>$f = 1\text{ MHz}$ |  | 1336 | 1780 | pF       |
| $C_{oss}$ | Output Capacitance           |  |  | 298  | 400  | pF       |
| $C_{rss}$ | Reverse Transfer Capacitance |  |  | 266  | 400  | pF       |
| $R_g$     | Gate Resistance              |  |  | 1.2  |      | $\Omega$ |

### Switching Characteristics

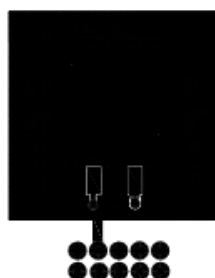
|              |                               |  |   |    |     |    |    |
|--------------|-------------------------------|--|---|----|-----|----|----|
| $t_{d(on)}$  | Turn-On Delay Time            | $V_{DD} = 13\text{ V}$ , $I_D = 20\text{ A}$ ,<br>$V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$ |   | 8  | 16  | ns |    |
| $t_r$        | Rise Time                     |  |   | 7  | 14  | ns |    |
| $t_{d(off)}$ | Turn-Off Delay Time           |  |   | 19 | 34  | ns |    |
| $t_f$        | Fall Time                     |  |   | 4  | 10  | ns |    |
| $Q_g$        | Total Gate Charge             |  | $V_{GS} = 0\text{ V to } 10\text{ V}$           |    | 24  | 34 | nC |
| $Q_g$        | Total Gate Charge             | $V_{GS} = 0\text{ V to } 5\text{ V}$   | $V_{DD} = 13\text{ V}$ ,<br>$I_D = 20\text{ A}$ |    | 14  | 20 | nC |
| $Q_{gs}$     | Gate to Source Charge         |  |   |    | 4.0 |    | nC |
| $Q_{gd}$     | Gate to Drain "Miller" Charge |  |   |    | 5.7 |    | nC |

### Drain-Source Diode Characteristics

|          |                                       |  |  |     |     |    |
|----------|---------------------------------------|--|--|-----|-----|----|
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS} = 0\text{ V}$ , $I_S = 3.1\text{ A}$ (Note 2)    |  | 0.8 | 1.2 | V  |
|          |                                       | $V_{GS} = 0\text{ V}$ , $I_S = 20\text{ A}$ (Note 2)     |  | 0.9 | 1.3 |    |
| $t_{rr}$ | Reverse Recovery Time                 | $I_F = 20\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ |  | 15  | 27  | ns |
| $Q_{rr}$ | Reverse Recovery Charge               |  |  | 4   | 10  | nC |

#### Notes:

- 1:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a)  $40\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b)  $96\text{ }^\circ\text{C/W}$  when mounted on a minimum pad

2: Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle <  $2.0\%$ .

3:  $E_{AS}$  of  $40\text{ mJ}$  is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = 9\text{ A}$ ,  $V_{DD} = 23\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 21\text{ A}$ .

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

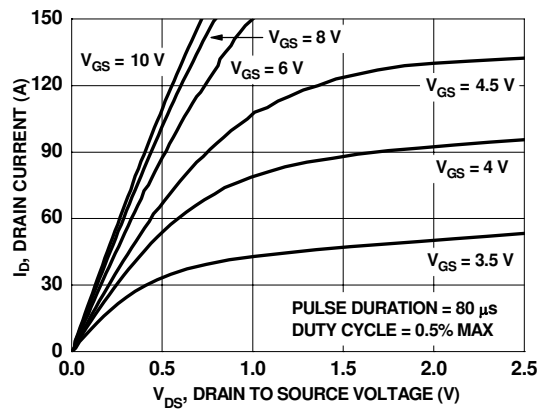


Figure 1. On Region Characteristics

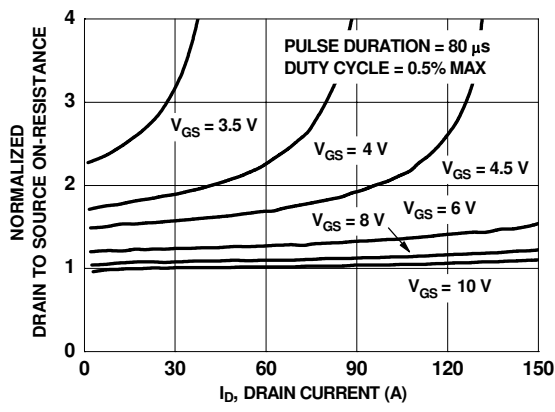


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

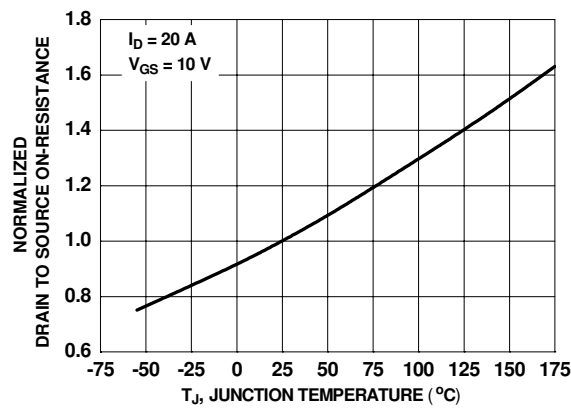


Figure 3. Normalized On Resistance vs Junction Temperature

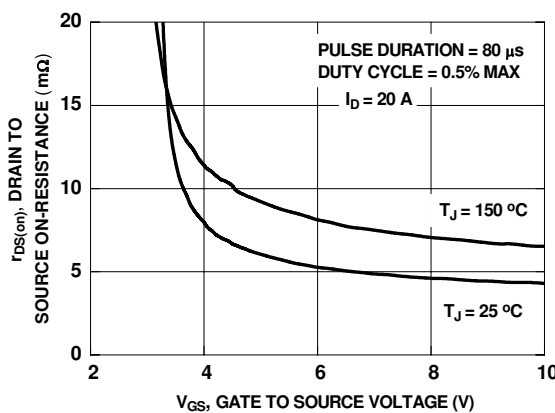


Figure 4. On-Resistance vs Gate to Source Voltage

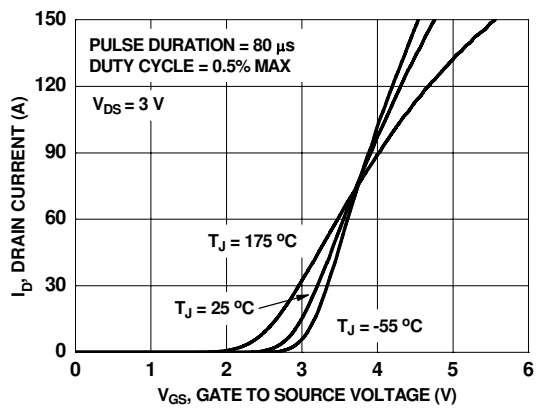


Figure 5. Transfer Characteristics

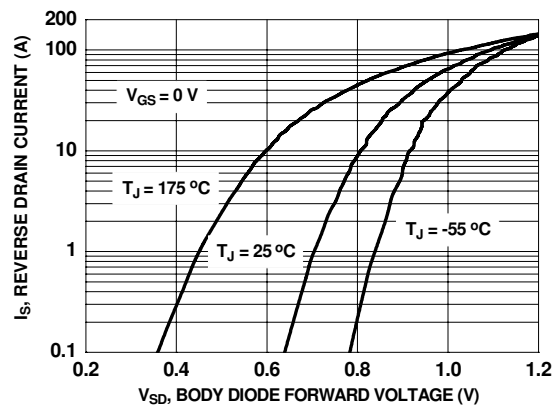
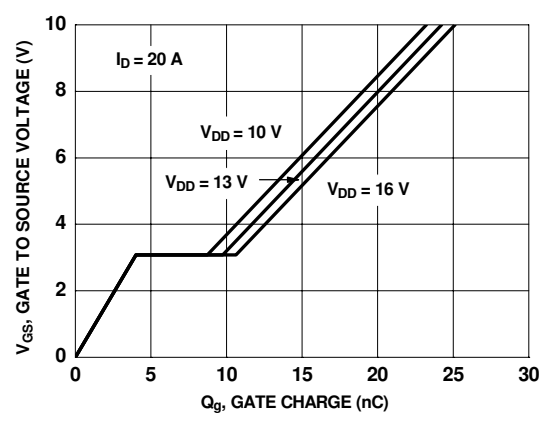
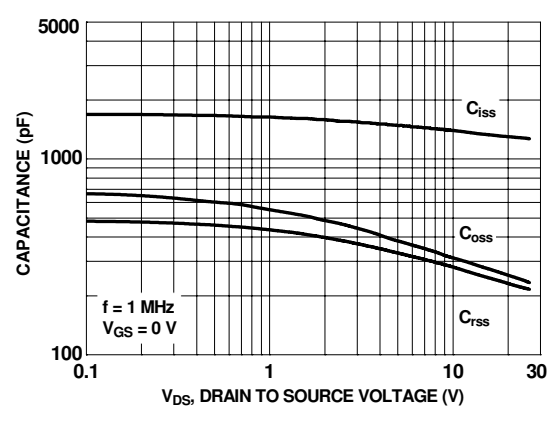


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

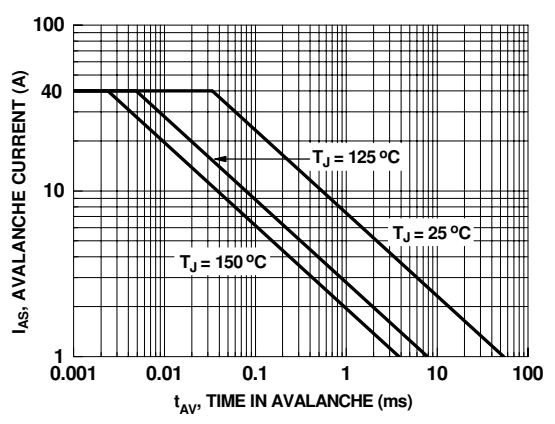
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



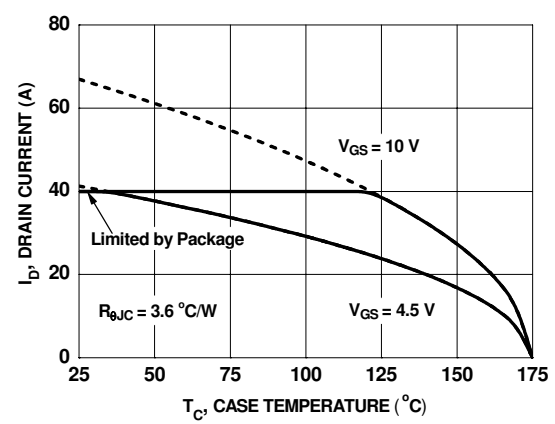
**Figure 7. Gate Charge Characteristics**



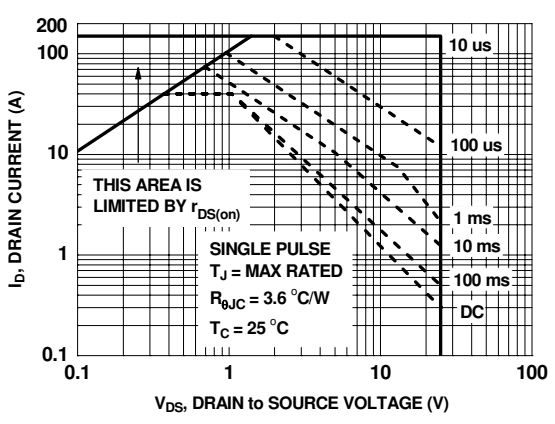
**Figure 8. Capacitance vs Drain to Source Voltage**



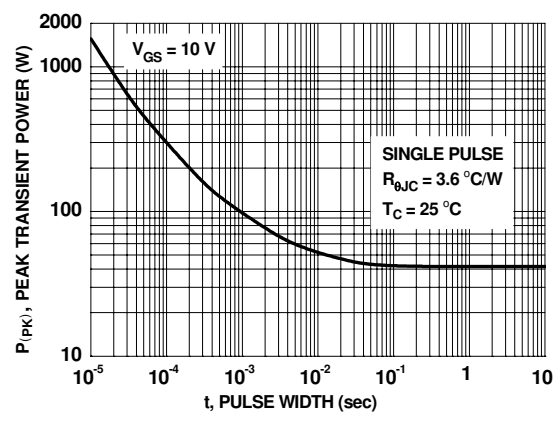
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

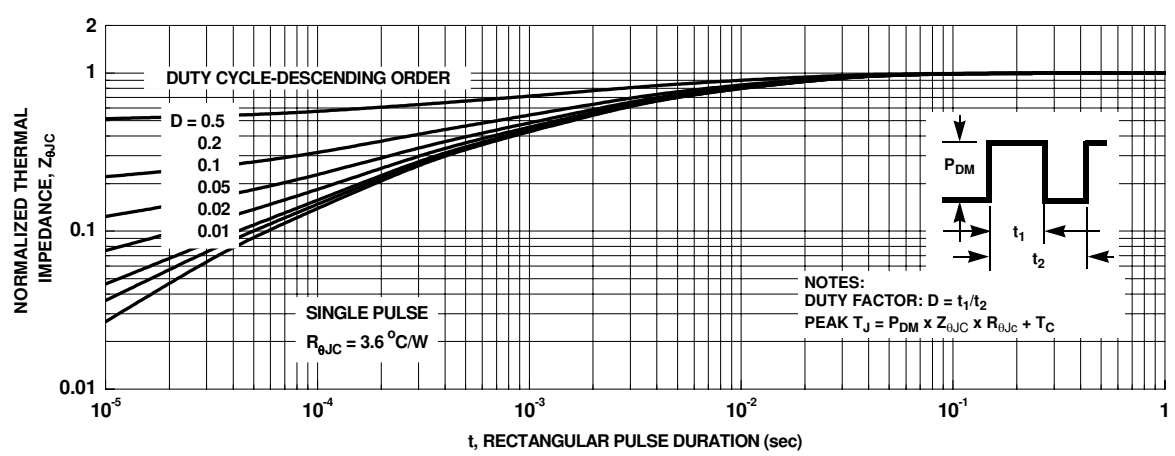


**Figure 11. Forward Bias Safe Operating Area**

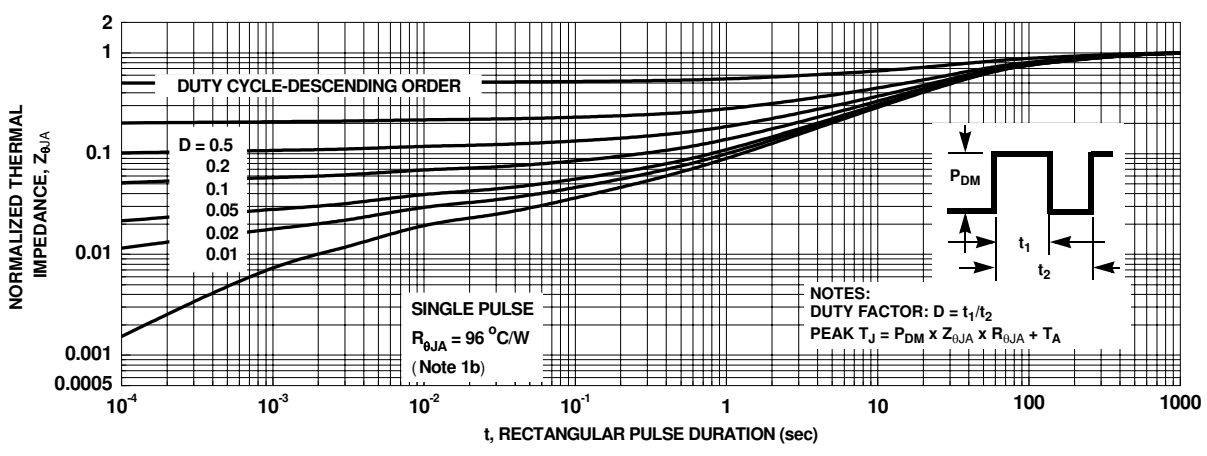


**Figure 12. Single Pulse Maximum Power Dissipation**

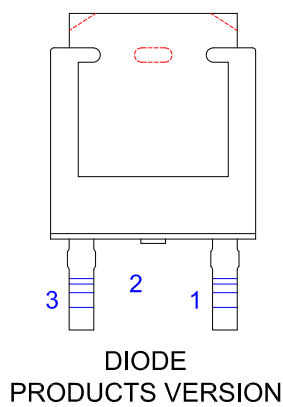
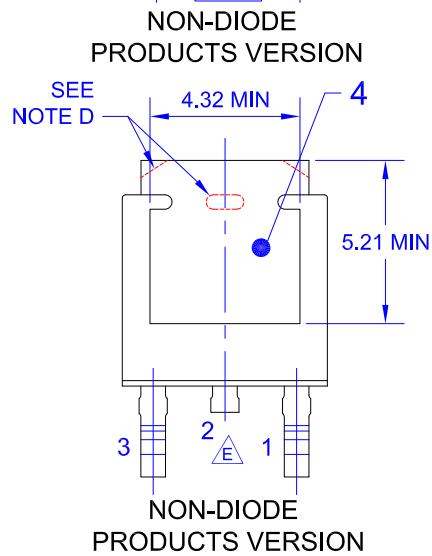
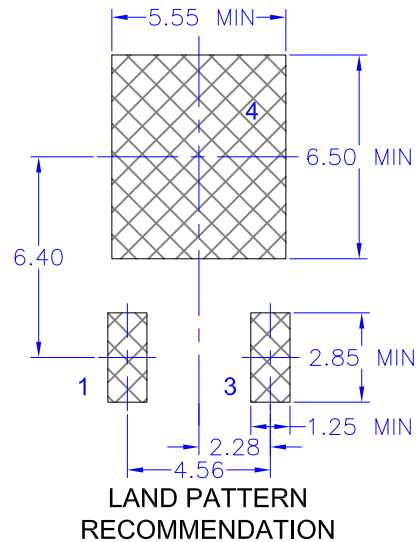
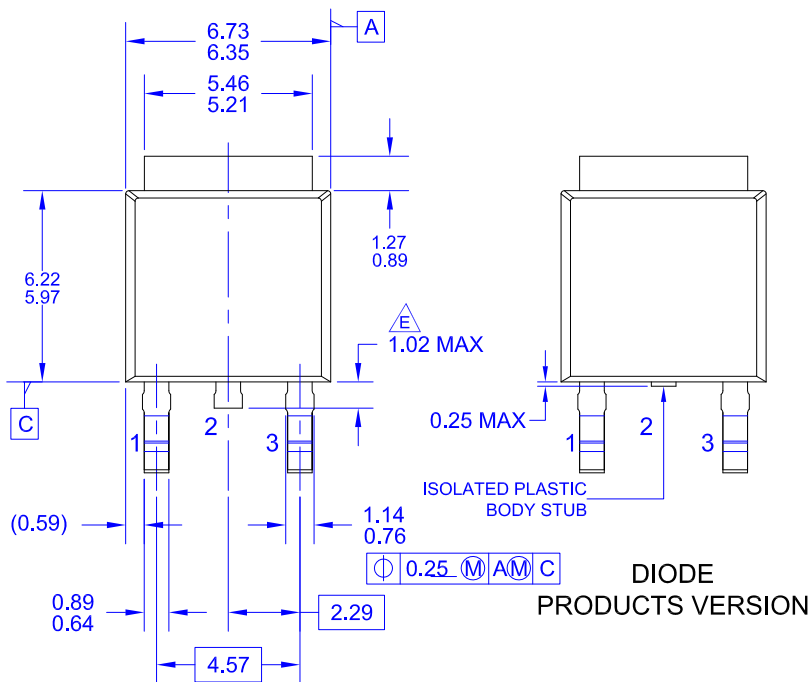
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Case Transient Thermal Response Curve**

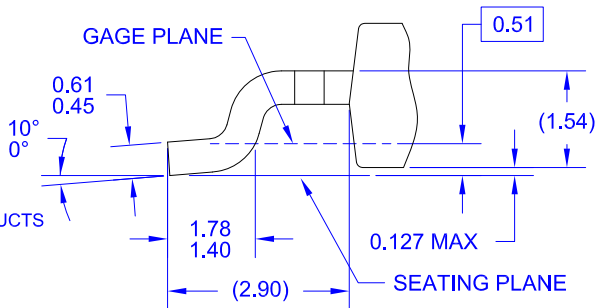


**Figure 14. Junction-to-Ambient Transient Thermal Response Curve**



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



DETAIL A  
(ROTATED -90°)  
SCALE: 12X



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