Silicon Image

PanelLink®

Technology

SiI 1362/A & SiI 1364/A
SDVO PanelLink Transmitter

Data Sheet

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Silicon Image, Inc.

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Revision History

Revision	Date	Comment
A	07/04	Revision A Release
A1	08/05	Added 1362A and 1364A part number.
A2	08/05	Adjusted 64 pin A1 & A2 overlap.
B	10/05	Added SiI 1362A & 1364A new power numbers. Updated PVCC1 Voltage range to 3.30V ± 10%. Voltage Regulation for PVCC1 omitted for SiI 1362A & SiI 1364A.
B1	03/06	Included new QFN package dimensions and ordering number.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

General Description

The SiI 1362/A & SiI 1364/A TMDS transmitter uses PanelLink® Digital technology to support displays ranging from VGA to UXGA resolutions in a single link interface. The chip supports the Intel-proprietary SDVO serial interface to provide a display interface to DVI monitors.

Designed explicitly to accommodate the ultra high-speeds needed for SDVO signaling, the SiI 1362/A & SiI 1364/A transmitter reduces pin count yet provides an upgrade path for future feature expansion. The innovative design of the SiI 1362/A & SiI 1364/A eases board design requirements as well.

PanelLink Digital technology simplifies PC design by resolving many of the system level issues associated with high-speed mixed signal design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.

Features

- Scaleable Output Bandwidth: 25 - 165 megapixels per second
- SiI 1362/1364 fully compliant with Intel SDVO 1.0
- SiI 1362A/1364A fully compliant with Intel SDVO 1.1
- I^2C Slave interface for access to internal registers
- Dual I^2C pass-through interfaces for host I^2C access of EDID (via DDC) and configuration EEPROM (on 64-pin package only)
- Monitor Detection supported through Hot Plug or Receiver Sense
- Low Power: 1.8V core operation; power down mode
- Cable Distance Support: greater than 10 meters
- DVI 1.0 compliant, with significantly greater margin than competitive solutions
- SiI 1362/A: 48-pin LQFP without EEPROM interface
- SiI 1364: 64-pin TQFP package with EEPROM interface
- SiI 1364A: 64-pin TQFP or QFN package with EEPROM interface.

SiI 1362/A & SiI 1364/A Pin Diagrams

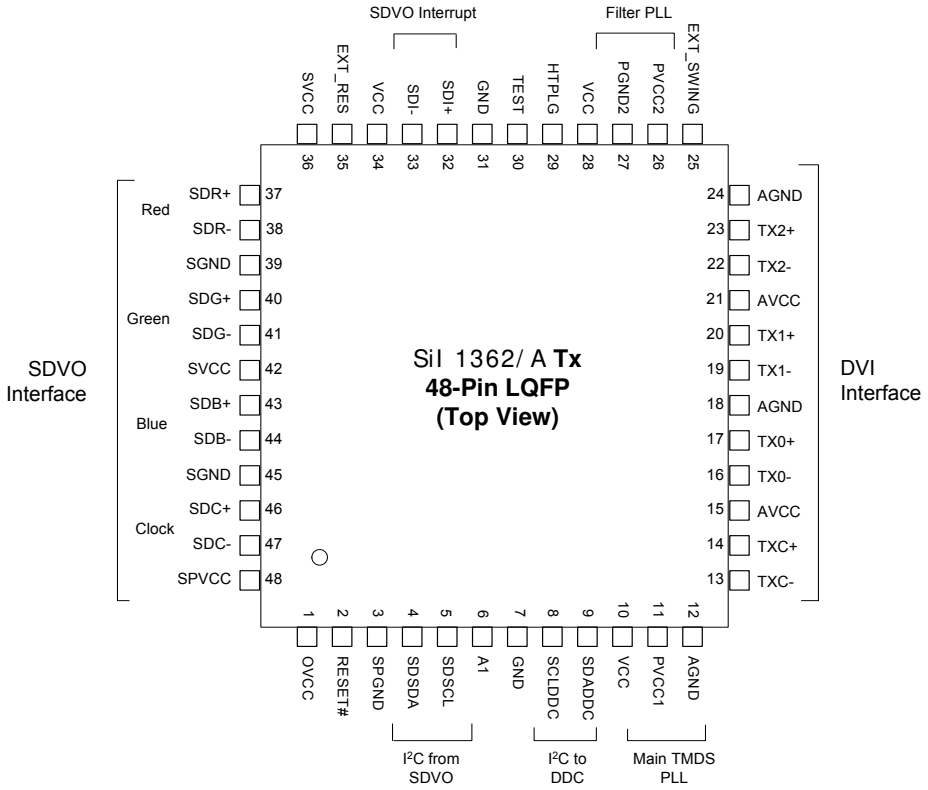


Figure 1. SiI 1362/A Pin Diagram - 48-pin package

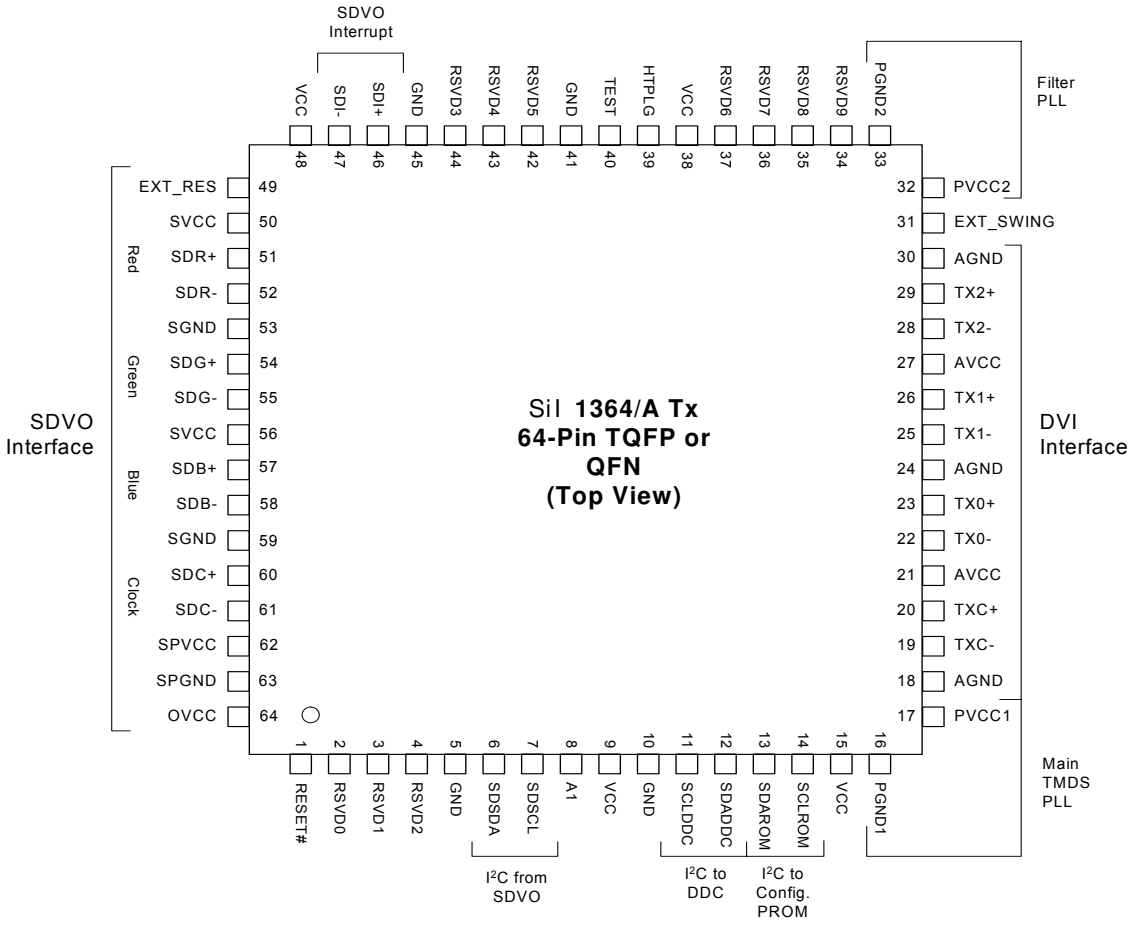


Figure 2. Sil 1364/A Pin Diagram - 64-pin package

Functional Blocks

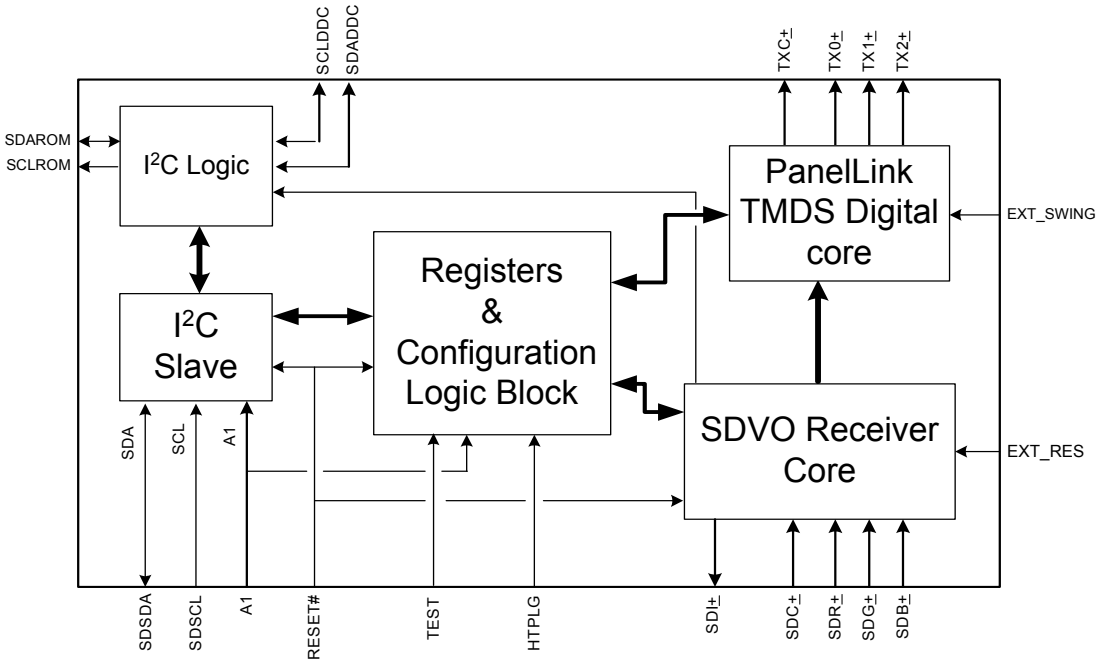


Figure 3. Functional Block Diagram

PanelLink TMDS Digital Core

The PanelLink TMDS core encodes video information onto three TMDS differential data lines and the differential clock. Decoded video input data comes from the SDVO Receiver Core. A resistor tied to the EXT_SWING pin is used to control the TMDS swing amplitude.

SDVO Receiver Core

Data is input to the SiI 1362/A & SiI 1364/A by way of the SDVO bus. SDVO data is encoded, therefore this core decodes the data per the Intel specification before passing it to the TMDS Receiver Core. Refer to the Intel “Serial Digital Video Out (SDVO) Port” specification for further details. A resistor (value specified in the Pin Description section) must be connected between the EXT_RES pin and ground to set the SDVO circuit bias. The device may be powered down with an internal register. It is initialized or reset by using the RESET# pin.

The SDVO Clock rate will always fall between 100MHz and 200MHz. Anytime the effective PCLK is below 100MHz, the SDVO clock will be a multiple of the Pixel rate as listed in the Multiplier column of Table 1.

Table 1. SDVO Clock Multiplication

Mode	Resolution (pixels)	Refresh (Vsync) (Hz)	DVI CLK (MHz)	Multiplier	SDVO CLK (MHz)
VGA	640x480	60	25	X4	100
SVGA	800x600	60	40	X4	160
XGA	1024x768	60	65	X2	130
SXGA	1280x1024	60	108	X1	108
SXGA (Hi Ref)	1280x1024	75	135	X1	135
UXGA	1600x1200	60	162	X1	162

I^2C Slave Interface and Display Detection

The SiI 1362/A & SiI 1364/A supports only I^2C mode of operation. There is no strap option mode. The logic uses a slave I^2C interface capable of running up to 1MHz for communication with the host chipset. This slave interface is 3.3V-tolerant and accepts 2.5V and 1.8V signaling as well. If the switching levels from the host are greater than 3.3V, then a voltage level shifter must be used.

The SiI 1362/A & SiI 1364/A Tx provides I^2C ports to communicate with a configuration EEPROM and the DDC bus with an attached monitor. The SDVO I^2C port operates at 2.5V and does not require level shifters. The EEPROM I^2C port operates at 3.3V level, via internal 3.3V pull ups, for direct connection to a 3.3V EEPROM. To operate the EEPROM I^2C port at 5V an external 3.3V to 5V level shifter is required. The DDC I^2C port is set to operate at 5V without requiring any level shifters.

A connected display EDID may be detected using the DVI Hot Plug signal, through the HTPLG pin. A powered up attached receiver can be detected with the Receiver Sense logic internal to the SiI 1362/A & SiI 1364/A. The state of the detection may be read from the registers and can optionally be signaled to the host by an interrupt. For systems with multiple SDVO devices, pin A1 can be used to change the slave I^2C address of the SiI 1362/A & SiI 1364/A.

Electrical Specifications

Absolute Maximum Conditions

Absolute Maximum Conditions are defined as the worst-case condition the part will tolerate without sustaining damage. Permanent device damage may occur if absolute maximum conditions are exceeded. Proper operation under these conditions is not guaranteed. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Table 2. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
	All 1.8V Supply Voltages	-0.3		2.5	V
	All 3.3V Supply Voltages	-0.3		4.0	V
V_I	Input Voltage	-0.3		V_{CC}+ 0.3	V
V_O	Output Voltage	-0.3		V_{CC}+ 0.3	V
T_J	Junction Temperature (with power applied)			125	°C
T_{STG}	Storage Temperature	-65		150	°C

Normal Operating Conditions

Table 3. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
	All 1.8V Supply Voltages	1.8 - 10%	1.8	1.8 + 10%	V
	Analog supply AVCC	3.0	3.3	3.6	V
	Main PLL supply PVCC1	3.3	3.3[3]or 3.45[2]	3.6	V
	Filter PLL supply PVCC2	3.0	3.3[3]or 3.45[2]	3.6	V
	SDVO PLL supply SPVCC	3.0	3.3[3] or 3.45[2]	3.6	V
	Output driver supply OVCC	3.0	3.3	3.6	V
V_{CCN}	PLL Supply Voltage Noise			100	mV_{P-P}
T_A	Ambient Temperature (with power applied)	0	25	70	°C
$\theta_{JA-64QFP}$	64-pin Thermal Resistance (Junction to Ambient)			50	°C/W
$\theta_{JA-64QFN}$	64-pin Thermal Resistance (Junction to Ambient)[4]			25	°C/W
θ_{JA-48}	48-pin Thermal Resistance (Junction to Ambient)			60	°C/W

Notes:

1. Airflow at 0m/s.
2. SiI 1362 and SiI 1364 only requirement 3.45V should be used when sharing the power supply with PVCC1.
3. SiI 1362A and SiI 1364A can operate within 3.30V ± 10% for all 3.30V power supply pins.
4. SiI 1364A QFN Package only with ePad soldered to landing area on four-layer board.

DC Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

Table 4. DC Digital I/O Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage – digital input pins		2.0		VCC + 0.3	V
V_{IL}	Low-level Input Voltage – digital input pins		-0.3		0.8	V
V_{IH5V}	High-level Input Voltage – 5V-tolerant pins		2.0		5.5	V
V_{IL5V}	Low-level Input Voltage – 5V-tolerant pins		-0.3		0.8	V
V_{CINL}	Input Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{CIPL}	Input Clamp Voltage[1]	I_{CL} = 18mA			VCC + 0.8	V
I_{IL}	Input Leakage Current		-10		10	µA

Notes:

1. Guaranteed by design. Voltage undershoot or overshoot cannot exceed absolute maximum conditions.

DC Specifications

Under normal operating conditions with R_{EXT_SWING} = 360Ω and source termination present unless otherwise specified.

Table 5. DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DOS}	Differential Output Short Circuit Current[1]	V_{OUT} = 0V			5	µA
I_{PDQ}	Quiet Power-down Current[2]	25°C ambient, V_{cc} = 3.3V			3	mA
I_{PD18}	Power-down Current[3]	Standby mode[3]			5	mA
I_{PD33}					5/0.5[6]	mA
I_{CCT18}	1.8V Transmitter Supply Current	Typical[4]		240		mA
		Worst Case[5]			320	mA
I_{CCT33}	3.3V Transmitter Supply Current	Typical[4]		50/80[6]		mA
		Worst Case[5]			80/110[6]	mA
All SDVO-related DC specifications are met. SDVO specifications are Intel-proprietary and are not published here.						

Notes:

1. Guaranteed by Characterization.
2. Quiet Power-down current measured with no transmitter input pins toggling, but includes source termination current.
3. Power-down current measured with device in D3 state and no SDVO input present.
4. Typical uses a pattern containing a gray scale area, a checkerboard area and a text area.
5. Worst Case uses a pattern containing a black and white checkerboard; each checker is one pixel wide.
6. SiI 1362A and SiI 1364A power consumption only.

AC Specifications

Under normal operating conditions unless otherwise specified.

Table 6. AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
F_{CIP}	Internal IDCK Frequency	one pixel per clock	25		165	MHz		2
T_{I2CDVD}	SDA Data Valid Delay from SCL high to low transition	C_L = 400pf			1000	ns	Figure 4	1
		C_L = 10pf			300			
T_{RESET}	ISEL/RST# Signal Low Time required for valid reset		50			µs	Figure 5	
All SDVO-related AC specifications are met by design but are Intel-proprietary and are not published here.								

Notes:

1. All Standard mode (100kHz and 400kHz) & SDVO 1MHz I^2C timing requirements are guaranteed by design.
2. Minimum frequency (maximum IDCK period) defined per DVI 1.0 Specification, section 2.3.1.
3. Typical VCC is defined at 3.3V.

Input Timing Diagrams

All SDVO timings are met according to Intel specifications and are not illustrated here.

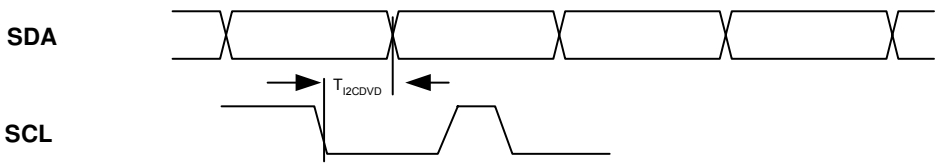


Figure 4. I^2C Data Valid Delay (driving Read Cycle data)

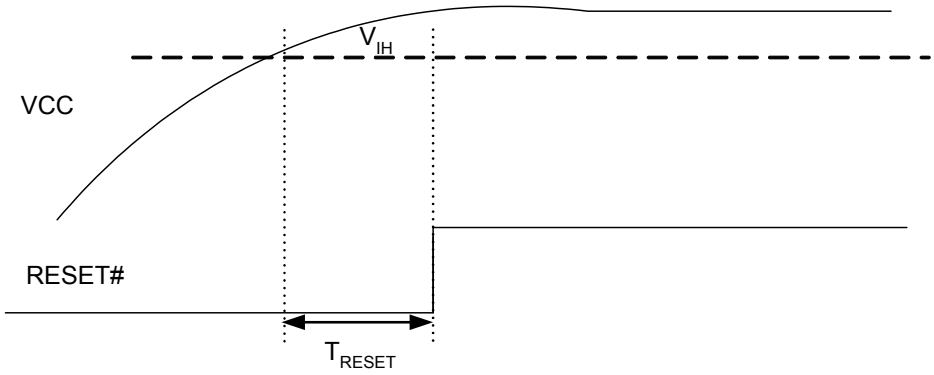


Figure 5. RESET# Minimum Timing

Note that VCC must be stable between its limits for Normal Operating Conditions for T_{RESET} before RESET# is high.

Pin Descriptions

SDVO Receiver Core Pins

Pin Name	64-pin #	48-pin #	Type	Description
SDR+ SDR– SDG+ SDG– SDB+ SDB–	51 52 54 55 57 58	37 38 40 41 43 44	Analog	SDVO Input Data. This bus receives encoded serial data from the host graphics chipset. The signals are AC-coupled through capacitors that are typically present on the motherboard and therefore not needed on an ADD2 card.
SDC+ SDC–	60 61	46 47	Analog	SDVO Input Clock. The SDVO clock signal comes in on this signal pair. The signals are AC-coupled through capacitors that are typically present on the motherboard and therefore not needed on an ADD2 card.
SDI+ SDI–	46 47	32 33	Analog	Interrupt. Enabled interrupts are transmitted to the host chipset on this signal pair. The signals are AC-coupled through capacitors that are typically NOT present on the motherboard, so separate 100nF coupling capacitors are required on these pins on an ADD2 card.
EXT_RES	49	35	Analog	External Resistor. A resistor value 1.0KΩ is connected from this pin to SGND to generate a reference bias current for the SDVO analog circuits.

Configuration/Programming Pins

Pin Name	64-pin #	48-pin #	Type	Description
RESET#	1	2	Digital In	Reset. When LOW, the chip logic is reset and all register values are set to their initial default state.
SDSCL	7	5	In/Out 5V-tolerant	SDVO Register Access I^2C Clock. This 5V-tolerant pin operates with an external pull-up resistor to 1.8-3.3V. It is typically pulled up to 2.5V with a 5.6KΩ resistor for proper operation with the SDVO host.
SDSDA	6	4	In/Out 5V-tolerant	SDVO Register Access I^2C Data. This 5V-tolerant pin uses an open collector output driver and requires a pull-up resistor to 1.8-3.3V for proper operation. It is typically pulled up to 2.5V with a 5.6KΩ resistor for proper operation with the SDVO host.
A1	8	6	Digital In	Slave I^2C Address bit A1. This pin selects bit 1 of the I^2C slave address. It has an internal weak pull-down resistor, so if the pin is left unconnected the address will default to 0x70. LOW: Address = 0x70 HIGH: Address = 0x72
HTPLG	39	29	Digital In 5V-tolerant	Hot Plug input. This pin is used to monitor the “Hot Plug” detect signal (refer to the DVI Specification). This input is 5V-tolerant and includes an internal pull down.

Differential Signal Data Pins

Pin Name	64-pin #	48-pin #	Type	Description
TX0+ TX0– TX1+ TX1– TX2+ TX2–	23 22 26 25 29 28	17 16 20 19 23 22	Analog	TMDS Low Voltage Differential Signal output data pairs.
TXC+ TXC–	20 19	14 13	Analog	TMDS Low Voltage Differential Signal output clock pair.
EXT_SWING	31	25	Analog	Voltage Swing Adjust. A resistor should tie this pin to AVCC. This resistor sets the amplitude of the voltage swing. A smaller resistor value sets a larger voltage swing and vice versa. Recommended value is 360Ω, 5% tolerance used with source termination as described in the Design Recommendations section. This recommendation may change with future silicon revisions.

I^2C Master Interface Pins

Pin Name	64-pin #	48-pin #	Type	Description
SDADDC	12	9	In/Out 5V-tolerant	DDC Access I^2C Data. This pin should be connected to the DDC I^2C Data pin on the DVI connector. It uses an open collector output driver and requires a 2.2KΩ pull-up resistor to 5V for proper operation.
SCLDDC	11	8	In/Out 5V-tolerant	DDC Access I^2C Clock. This pin should be connected to the DDC I^2C Clock pin on the DVI connector. It uses an open collector output driver and requires a 2.2KΩ pull-up resistor to 5V for proper operation.
SDAROM	13	na	In/Out	ROM Access II^2C Data. Only available on the 64-pin SiI 1364/A, this pin should be connected to the EEPROM I^2C Data pin. It uses an open collector output driver. This pin incorporates an internal pull-up resistor to 3.3V and does not require an external 3.3V pull up.
SCLROM	14	na	Out	ROM Access I^2C Clock. Only available on the 64-pin SiI 1364/A, this pin should be connected to the EEPROM I^2C Clock pin. It uses an open collector output driver. This pin incorporates an internal pull-up resistor to 3.3V and does not require an external 3.3V pull up.

Factory Test Mode Pins

Pin Name	64-pin #	48-pin #	Type	Description
TEST	40	30	Digital In	Factory Test Mode strap. Tie this pin LOW for normal operation.
RSVD0-9	2, 3, 4, 44, 43, 42, 37,36, 35, 34	na	Digital In/Out	Reserved Factory Test Mode signals. Tie to GND or leave as No Connects.

Power and Ground Pins

Pin Name	64-pin #	48-pin #	Type	Description
VCC	9, 15, 38, 48	10, 28, 34	Power	Digital Core VCC, must be set to 1.8V nominal.
AVCC	21, 27	15, 21	Power	Analog VCC for TMDS Tx Core, must be set to 3.3V nominal.
PVCC1	17	11	Power	TMDS Main PLL Analog VCC, must be set to 3.3-3.45V nominal for SiI1362 and SiI1364 only. SiI1362A and SiI1364A can be set to 3.3V nominal.
PVCC2	32	26	Power	Filter PLL Analog VCC, must be set to 3.3-3.45V nominal for SiI1362 and SiI1364 only. SiI1362A and 1364A can be set to 3.3V nominal.
SVCC	50, 56	36, 42	Power	SDVO Analog VCC, must be set to 1.8V nominal.
SPVCC	62	48	Power	SDVO PLL Analog VCC, must be set to 3.3-3.45V nominal for SiI1362 and SiI1364 only. SiI1362A and 1364A can be set to 3.3V nominal.
OVCC	64	1	Power	Digital I/O VCC, must be set to 3.3V nominal.
GND	5, 10, 41, 45	7, 31 (39, 45)	Ground	Digital Ground (shared with SDVO Ground on 48-pin package)
AGND	18, 24, 30	12, 18, 24	Ground	Analog Ground.
PGND1	16	(12)	Ground	TMDS Main PLL Ground (shared with AGND on 48-pin package)
PGND2	33	27	Ground	TMDS Filter PLL Ground.
SGND	53, 59	39, 45	Ground	SDVO Analog Ground
SPGND	63	3	Ground	SDVO PLL Ground.

Notes
1. Connect all ground pins to main PCB ground plane. **Do not split planes.**
2. Apply **separate filters** to each PLL VCC/GND pair as noted in the Design Recommendations section.

Feature Information

I²C Slave Interface

The SiI 1362/A & SiI 1364/A slave state machine does not require an internal clock. It supports byte-read and byte-write operations, and also burst read/write to both the internal registers and to the EEPROM and DDC.

The 7-bit binary address of the I²C machine is "0111 00A_1R" where R =1 sets a read operation while R=0 sets a write operation. Pin A1 by default has an internal pull down resistor. Therefore, the port address is 0x70/0x71 by default. To set the I²C address for the SiI 1362/A & SiI 1364/A to 0x72/0x73, pin A1 must be pulled up through a resistor to VCC.

The interface also accepts accesses at ports 0xA0/0xA1 that are destined for the EEPROM or DDC.

See Figure 6 for a byte read operation and Figure 7 for a byte write operation.

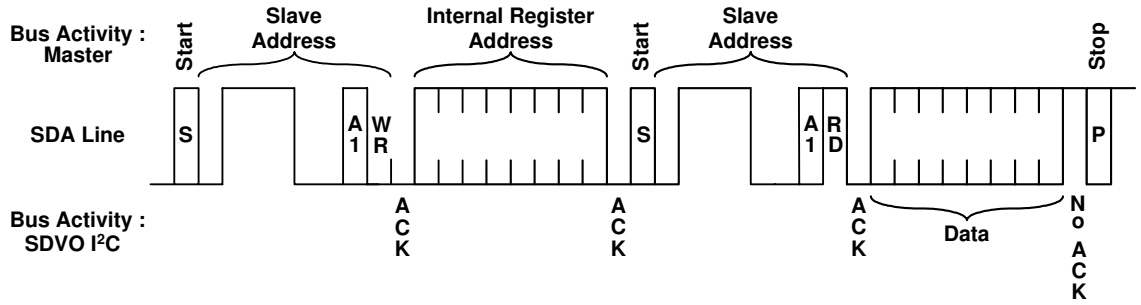


Figure 6. I²C Byte Read

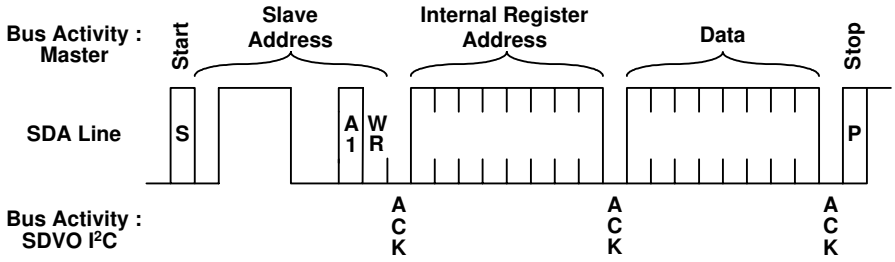


Figure 7. I²C Byte Write

Multiple data bytes may be transferred in each transaction, regardless of whether a read or a write is taking place. The operations will be similar to those in the figures except that there will be more than one data phase. An ACK will follow each byte, except the last byte in a read operation. Byte addresses increment, with the least significant byte transferred first, and the most significant byte last.

For more detailed information on I²C protocols refer to the I²C Bus Specification version 2.1 available from Philips Semiconductors Inc.

Design Recommendations

EXT_SWING Selection

The recommended R_{EXT_SWING} resistor value for the EXT_SWING pin is provided in the Pin Descriptions section. This value can be adjusted as needed to optimize the DVI signal swing levels according to the needs of the application. This adjustment might become necessary, for example, when deviating from the recommended source termination values (described in the Source Termination Resistors on Differential Outputs section) to optimize for a specific board layout. Figure 8 illustrates the relationship of the R_{EXT_SWING} resistor to the differential swing voltage, across representative extremes of the chip.

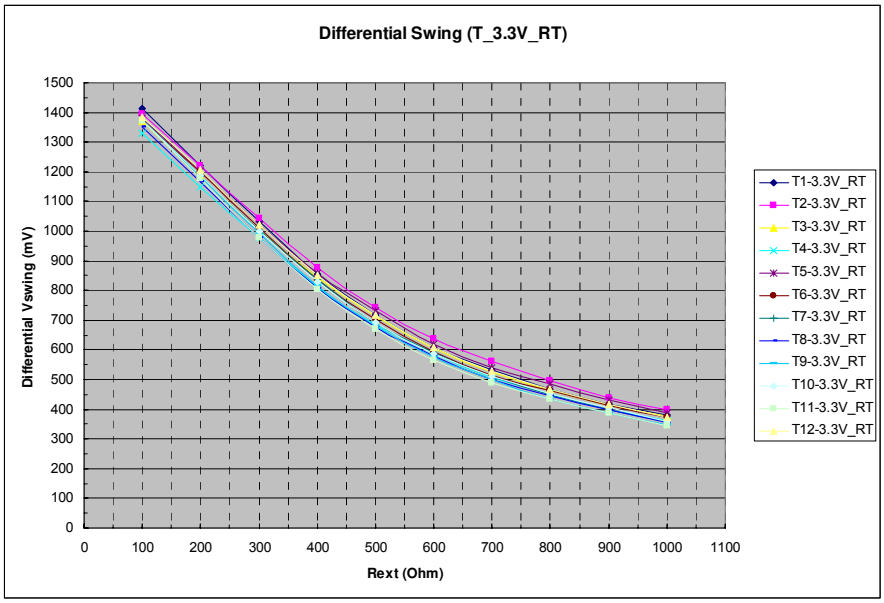


Figure 8. Variation of Differential Swing versus R_{EXT_SWING} Value

EXT_RES Selection

The resistor value specified in the Pin Descriptions section must connect the EXT_RES pin to SGND. The resistor is used to generate a reference bias current for SDVO analog circuits.

SDVO I²C Bus Interface

To program the SiI 1362/A & SiI 1364/A via its slave I²C bus connection with the SDVO host, SDSDA and SDSCL swing level should be 2.5V. This is the standard SDVO signaling level for this interface. These pins should be pulled to 2.5V with 5.6KΩ resistors.

DDC I²C Bus Interface

The VESA DDC Specification (available at http://www.vesa.org) defines the DDC interconnect bus to be a 100kbit/s 5V signaling path. The DDC I²C pins on the SiI 1362/A & SiI 1364/A Tx chip are 5V-tolerant. Therefore, board designers can connect the pins without using a level-shifting circuit. These pins should be pulled to 5V with 2.2KΩ resistors.

If the host system is using a DVI-I connector to support both a DVI and a VGA (analog) connection, only the host VGA I²C interface should be connected to the DVI-I connector. The DDC interface of the SiI 1362/A & SiI 1364/A Tx chip should be tied only to 2.2KΩ resistors to 5V but should not connect to the DVI-I connector.

EEPROM I²C Bus Interface

The 64-pin version of the SiI 1362/A & SiI 1364/A Tx provides a communications path from the SDVO host to a configuration EEPROM. The interface can support up to 400Kb/s with commonly available EEPROMs. The interface pins are internally pulled up to 3.3V, and therefore do not require external pull-up resistors.

PCB Ground Planes

All ground pins on the device should be connected to the same, contiguous ground plane in the PCB. This helps to avoid ground loops and inductances from one ground plane segment to another. Such low-inductance ground paths are critical for return currents, which affect EMI performance. The entire ground plane surrounding the PanelLink transmitter should be in one piece and include the ground vias for the DVI connector.

Power Plane Sequencing and Switching

As with any device using multiple power rails, the SiI 1362/A & SiI 1364/A Tx employs ESD protection diodes that can allow a current flow between the 3.3V and 1.8V planes. No special sequencing or voltage ramping precautions are necessary as long as both planes reach their nominal operating voltage within a few seconds of each other. However, if the 1.8V plane voltage remains greater than any 3.3V plane voltage by more than one diode drop (0.7V), there will be a continuous current flow through the protection diodes that could damage the device over time. For this reason, it is recommended that the 1.8V power plane voltage not be allowed to exceed any 3.3V power plane voltage by more than 0.7V under any steady-state operating condition.

Voltage Ripple Regulation

The power supply to PVCC pins is very important to the proper operation of the transmitter. Table 7 provides simple regulator circuits that are appropriate for each chip power plane. **Please note that** SiI **1362A &** SiI **1364A do not require 3.45V regulation and as such designers can omit the Voltage Regulation component and use the 3.30V power supply available from the motherboard.** Tx Sample regulator circuits are shown in the figures noted. Note that alternative voltage regulator circuits should be considered only if they meet the LM317 standards of line/load regulation.

Table 7. Power Regulator Circuit Suggestions

Voltage to be Regulated	Max current	Power Plane, % of Total Load	Voltage Regulation Description	Active Voltage Regulator Components	Figure
3.45V **(For** SiI **1362** /SiI **1364 only)**	60mA	PVCC1: 60-75% PVCC2: 5-15% SPVCC: 15-35%	12V to 3.42 V	LM317EMP	Figure 9
3.3V	20mA	AVCC: 5-15% OVCC: 80-95%	Use available 3.3V	none	--
5V	55mA	external	12V to 5V	LM317LM	Figure 10
1.8V	320mA	SVCC: 70-85% VCC: 25-35%	3.3V to 1.8V, Low Drop Out regulation	LM1117_1.8V	Figure 11
2.5V	10mA	external	3.3V to 2.5V	Simple Voltage Divider R1= 316Ω 1%, R2 = 1.0KΩ 1%	Figure 12

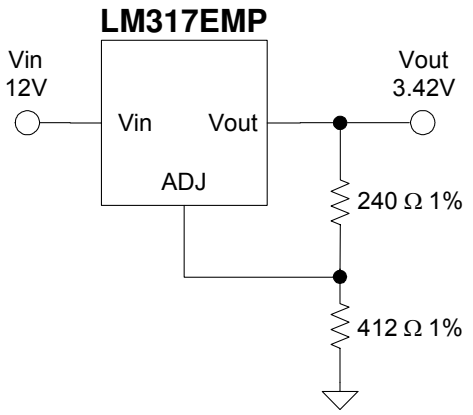


Figure 9. Suggested 3.42V Voltage Supply Circuit for SiI 1362 and SiI 1364 only

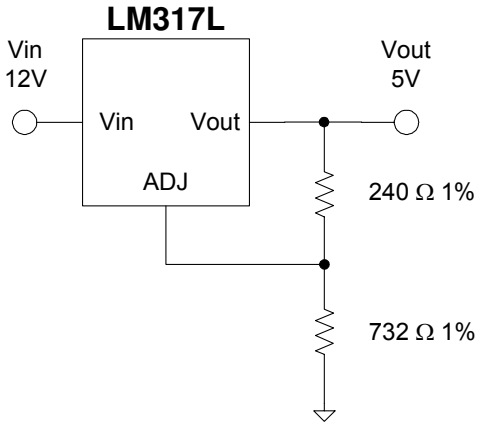


Figure 10. Suggested 5V Voltage Supply Circuit

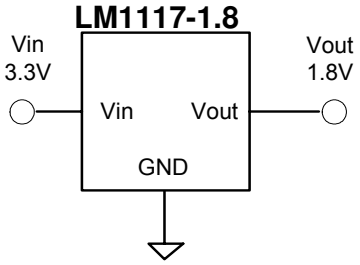


Figure 11. Suggested 1.8V Voltage Supply Circuit

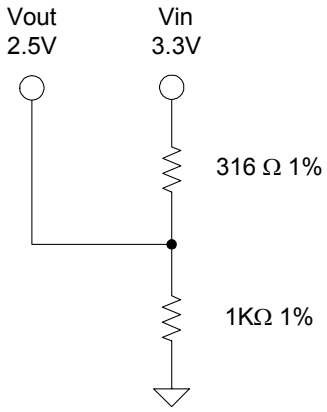


Figure 12. Suggested 2.5V Voltage Supply Circuit

Power Plane Filters

Recommended power plane filtering is shown in Table 8. The value of the capacitors is chosen to approximately cover the range of 162.5MHz to 2.5GHz for high frequency noise. Any higher frequency noise will be filtered by the inherent capacitance of the trace line followed by internal high frequency capacitors in the SiI 1362/A & SiI 1364/A Tx. Each group of pins should have one Ferrite whose impedance value must be greater than 100Ω but smaller than 300Ω.

Table 8. Power Plane Filter Recommendations for SiI 1362/A & SiI 1364/A

Power Supply	Component Applications			
	High Frequency C1	Mid Band C2	Storage C3	Ferrite Bead and Voltage Regulator
AVCC	1nF - One per pin	0.1uF - One per pin	10uF - One shared for two AVCC pins	One Ferrite Bead
OVCC	None required	0.1uF - One per pin	10uF - One on OVCC	None required
PVCC1	1nF - Two per pin	0.1uF - Two per pin	None required	Regulator required, shared by PVCC1, PVCC2 and SPVCC. Each power plane requires its own Ferrite Bead
PVCC2	1nF - Two per pin	0.1uF - Two per pin	None required	
SPVCC	1nF - Two per pin	0.1uF - Two per pin	None required	
SVCC	1nF - One per pin	0.1uF - One per pin	10uF - One shared for three SVCC pins	One Ferrite Bead
VCC	1nF - One per pin	0.1uF - One per pin	10uF - One shared for all VCC pins	One Ferrite Bead

Filter Capacitor and Ferrite Placement

Designers should include decoupling and bypass capacitors at each power pin in the layout. Place these components as close as possible to the PanelLink device pins, and avoid routing through vias if possible, as shown in Figure 13, which is representative of the various types of power pins on the transmitter.

Ensure that the correct Power and Ground pin are coupled with the filter capacitors as illustrated in Figure 13. For example, PVCC1 should have PGND1 as its ground pin and PVCC2 should have PGND2 as its ground pin. Note that for the 48-pin package, pin 12 should be used for the PGND1 capacitor connection.

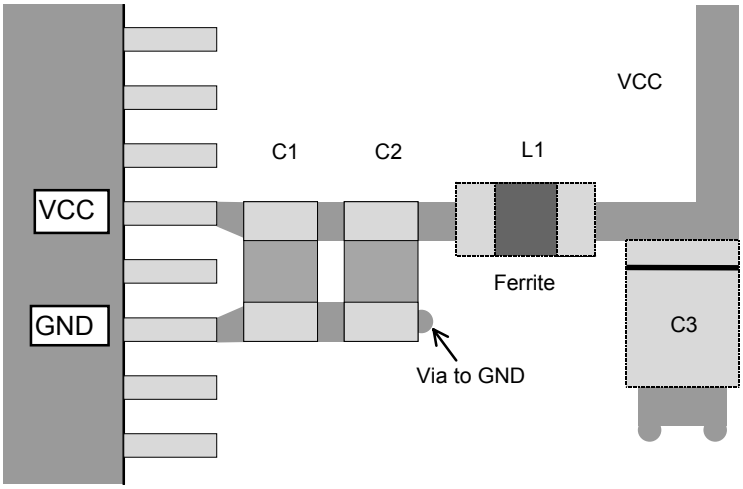


Figure 13. Decoupling and Bypass Capacitor Placement

Source Termination Resistors on Differential Outputs

Source termination, consisting of a 300Ω resistor and a 0.1µF capacitor, should be used on the differential outputs of the SiI 1362/A & SiI 1364/A to improve signal swings. See Figure 14 for an illustration. Repeat the circuit for each of the four differential output pairs: TX0±, TX1±, TX2±, TXC±.

Note that the specific value for the source termination resistor and capacitor will depend on the PCB layout and construction. Different values may be needed to create the best DVI-compliant output waveforms.

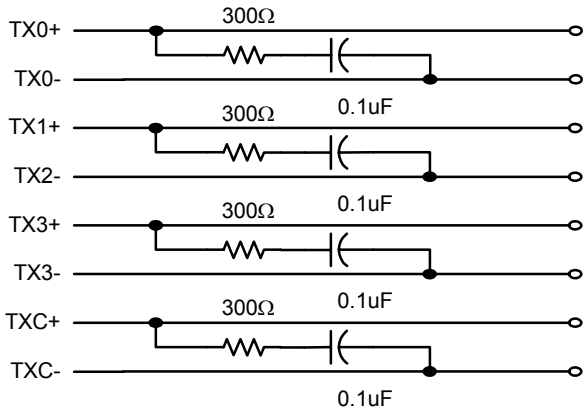
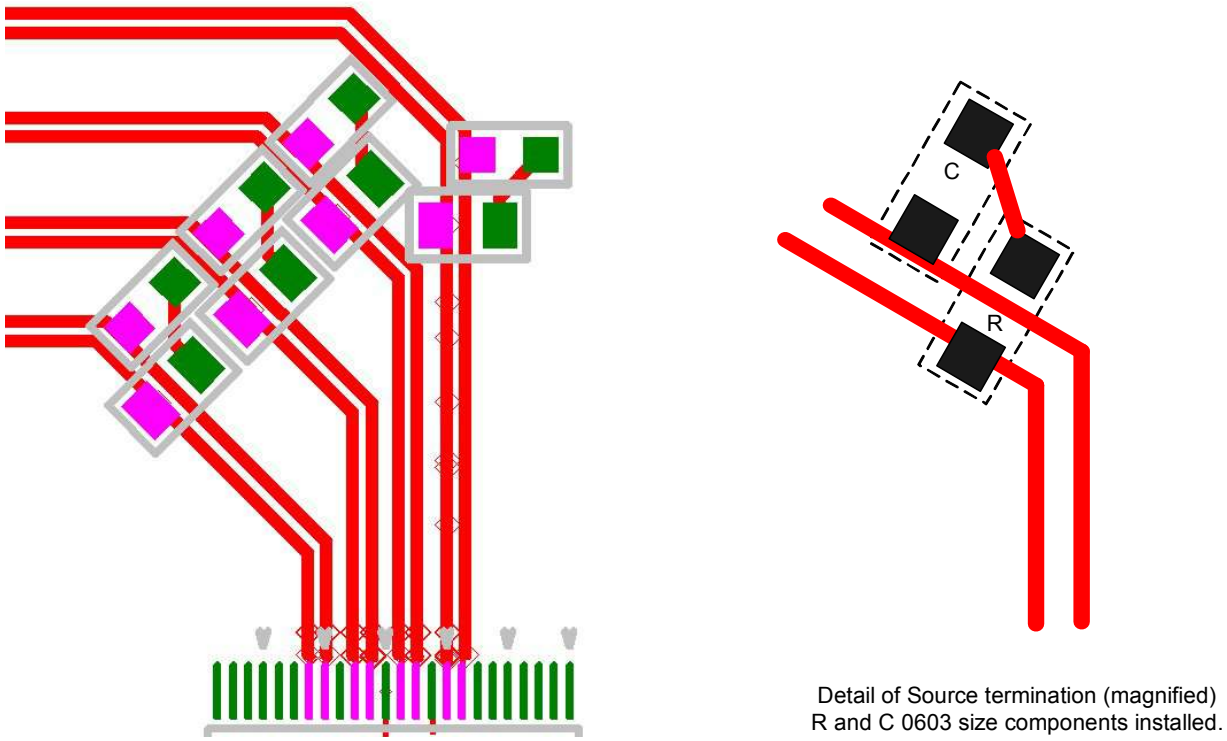


Figure 14. Differential Output Source Terminations

Source termination suppresses signal reflection to prevent non-DVI compliant receivers from erroneously sampling the TMDS signals when operating at high frequencies (beyond ~135MHz). The impact on DVI compliant receivers is minimal. Therefore Silicon Image recommends source termination for applications at all frequencies.



Detail of Source termination (magnified)
R and C 0603 size components installed.

Figure 15. Source Termination Layout Illustration

Note that the capacitor is required to meet DVI idle mode DC offset requirements and must not be omitted. Note also that the signal suppression requires the R_{EXT_SWING} value to be changed. Power consumption will be slightly higher when using source termination.

The layout shown has been developed to minimize trace stubs on the differential TMDS lines, while providing pads for the source termination components (left-hand magnified view). Source termination components should be placed close to the transmitter pins. The resistor and capacitor are shown installed on the pads provided (right-hand magnified view).

Transmitter Layout

The routing for the SiI 1362/A & SiI 1364/A chip is relatively simple since no spiral skew compensation is needed. However, a few small precautions are required to achieve the full performance and reliability of DVI.

The Transmitter can be placed fairly far from the output connector, but care should be taken to route each differential signal pair together and achieve impedance of 100Ω between the differential signal pair. However, note that the longer the differential traces are between the transmitter and the output connector, the higher the chance that external signal noise will couple onto the low-voltage signals and affect image quality.

Do not split or have asymmetric trace routing between the differential signal pair. Vias are very inductive and can cause phase delay if applied unevenly within a differential pair. Vias should be minimized or avoided if possible by placing all differential traces on the top layer of the PCB.

Figure 16 illustrates an incorrect routing of the differential signal from the SiI 1362/A & SiI 1364/A to the DVI connector.

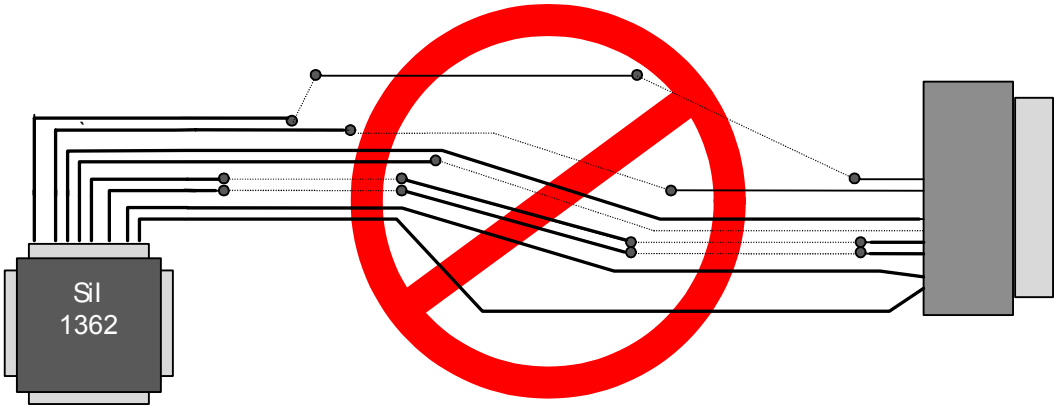


Figure 16. Example of Incorrect Differential Signal Routing

Figure 17 illustrates the correct method to route the differential signal from the SiI 1362/A & SiI 1364/A to the DVI connector. Figure 18 illustrates recommended routing for differential traces at the DVI connector.

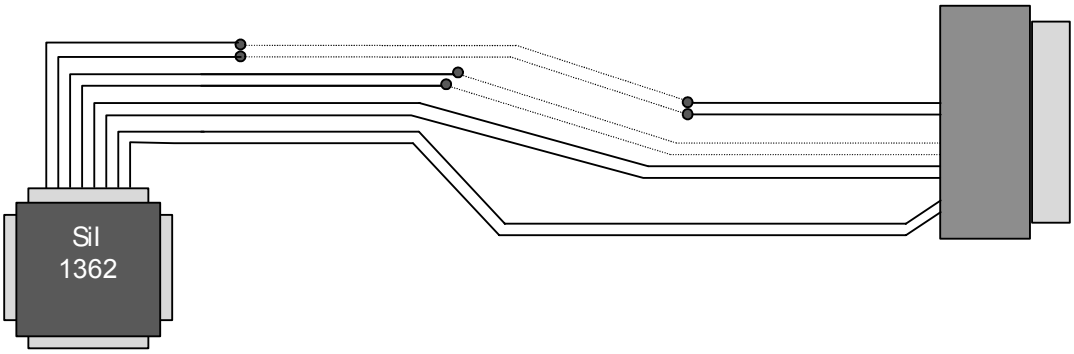


Figure 17. Example of Correct Differential Signal Routing

In addition to following the trace routing recommendations, length differences between intra-pair traces and inter-pair traces should be controlled to minimize DVI skew. Spacing between inter-pair DVI traces should be observed to reduce trace-to-trace couplings. For example, having wider gaps between inter-pair DVI traces will minimize noise coupling. It is also strongly advised that ground not be placed adjacent to the DVI traces on the same layer. Table 9 lists the recommended limits for the parameters listed above.

Table 9. Routing Guidelines for DVI Traces

Parameter	Intra-Pair (differential pair) Length	Inter-Pair (differential pair to differential pair) Length	Recommended Inter–pair Trace Separation Based on 2 Layer Board	Recommended Inter–pair Trace Separation Based on 4 Layer Board
Max	±0.75”	±3”		
Min			2x trace width	2x trace width

The layout in Figure 18 illustrates an optimized ADD2 Card with source termination and DVI connector mapping that follows the guidelines listed above. The trace length from the SiI 1362/A & SiI 1364/A to the DVI connector can be long; however, it is strongly recommended that the intra-pair and inter-pair trace lengths follow the guidelines provided above.

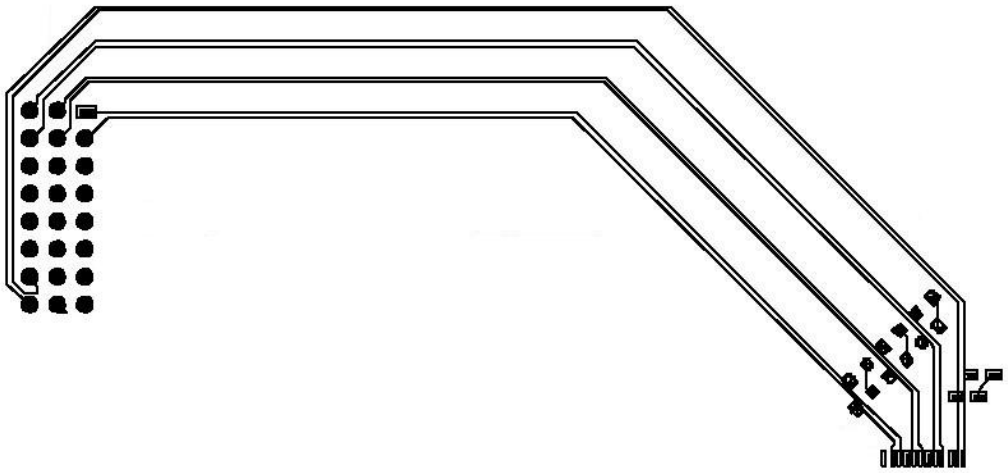


Figure 18. Source Termination to DVI Connector Illustration

Hot Plug Circuit

The Hot Plug pin on the DVI connector carries a 5V return signal from the monitor to indicate that its EDID is available for reading. The SiI 1362/A & SiI 1364/A chip can indicate a display-attached status) or generate an interrupt by monitoring this pin. The HTPLG input of the chip is 5V-tolerant. However, a protection circuit such as that shown in Figure 19 is recommended to bring the DVI connector hot plug detect signal to the HTPLG pin on the SiI 1362/A & SiI 1364/A.

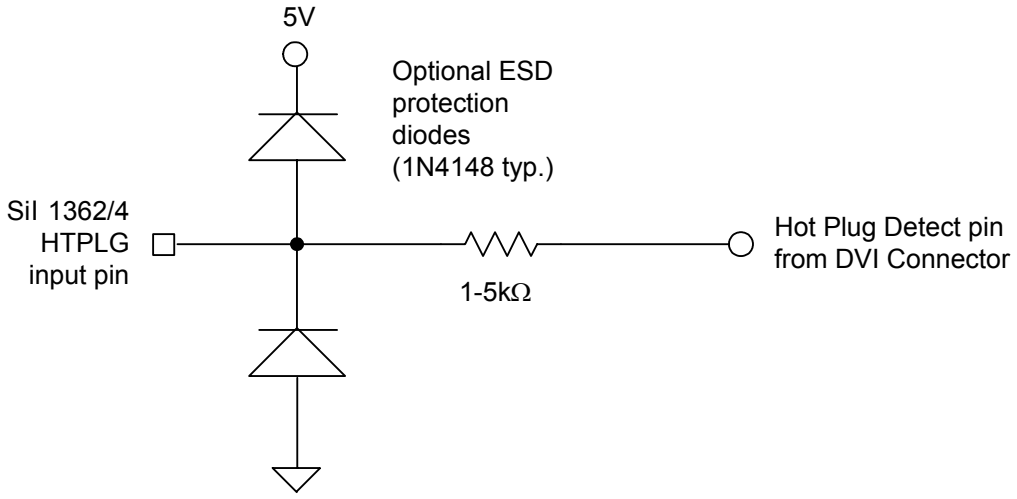


Figure 19. Recommended Hot Plug Connection

Receiver sense indicates that a powered monitor is attached, but will not indicate the presence of a monitor that is powered off. Therefore, in this default configuration the host system must read EDID at power-up regardless of the attach state reported by the SiI 1362/A & SiI 1364/A device, and must re-read EDID any time the attach state changes.

The chip defaults to using the receiver sense function, **not** the HTPLG input, for display-attached status after a Reset. However, Intel SDVO drivers automatically initializes the SiI 1362/A & SiI 1364/A Tx to support the Hot Plug function.

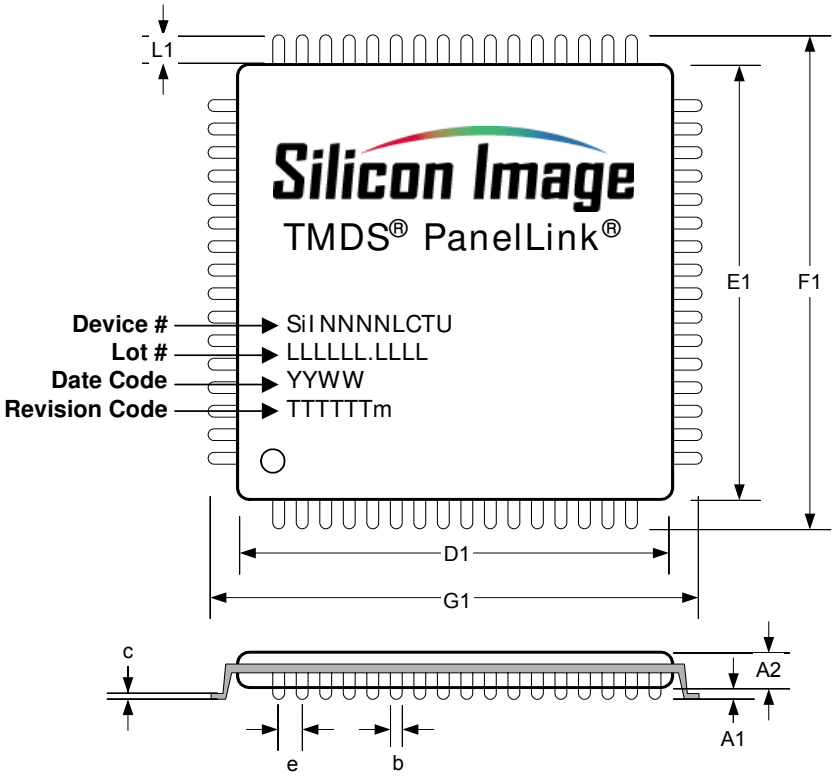
Package Dimensions and Marking Specification

64-pin TQFP Ordering Information

Part Numbers of Universal package for both Standard and Pb-free applications:

SiI 1364 Tx (SDVO 1.0 Compliant): SiI1364CTU

SiI 1364A Tx (SDVO 1.1 Compliant): SiI1364ACTU



JEDEC Package Code MS026-ACD

		typ	max
A	Thickness		1.20
A1	Stand-off		0.15
A2	Body Thickness	1.00	1.05
D1	Body Size	10.00	
E1	Body Size	10.00	
F1	Footprint	12.00	
G1	Footprint	12.00	
L1	Lead Length	1.00	
b	Lead Width	0.20	0.27
c	Lead Thickness		0.20
e	Lead Pitch	0.50	

Dimensions in millimeters.

Overall thickness A=A1+A2.

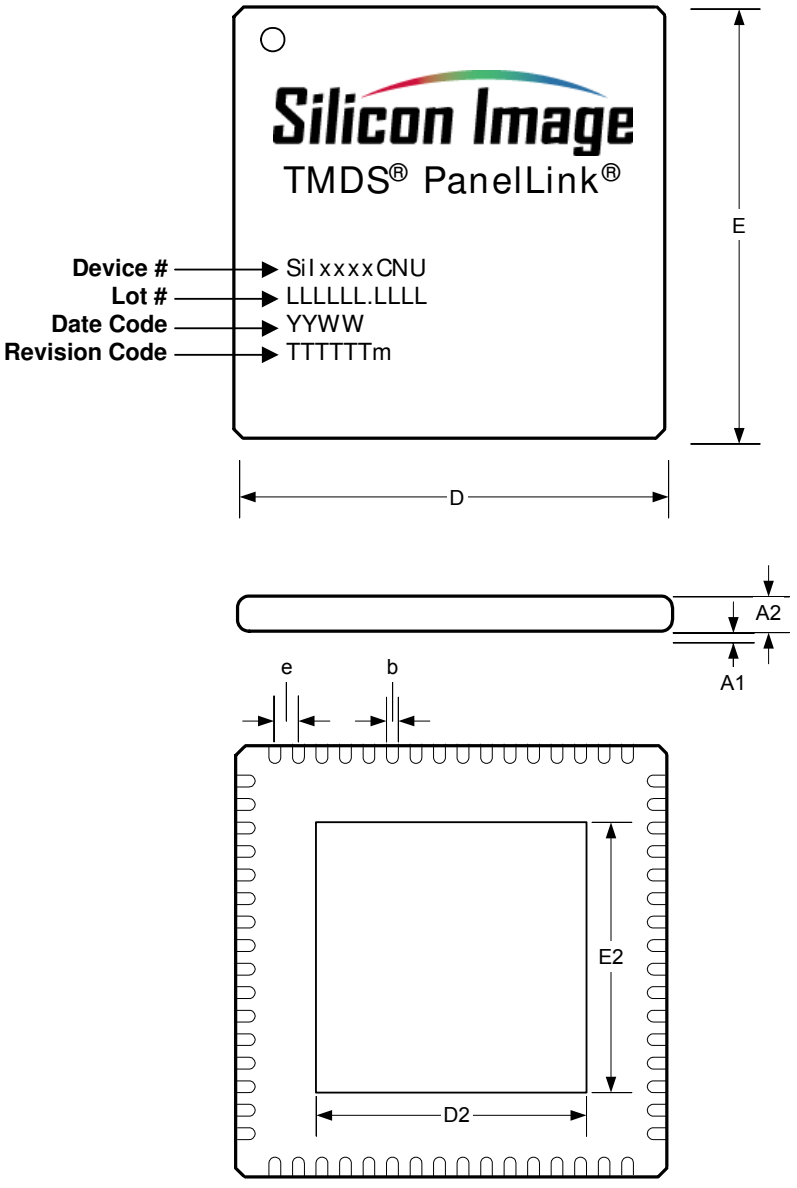
Legend	Description
SiINNNNLCTU	Device number SiI1364CTU or SiI1364ACTU
LLLLLL.LLLL	Lot Number
YY	Year of Mfr
WW	Week of Mfr
TTTTTT	Trace Code
m	Maturity Code

Figure 20. 64-pin TQFP Package Dimensions

64-pin QFN Ordering Information

Part Number of Universal package for both Standard and Pb-free applications:

Sil 1364A Tx(SDVO 1.1 Compliant): Sil1364ACNU



JEDEC Package Code MO-220

		typ	max
A	Thickness		0.90
A1	Stand-off		0.05
A2	Body Thickness	.65	0.70
D	Body Size	9.00	
E	Body Size	9.00	
L1	Terminal Length	0.40	
b	Terminal Width	0.25	0.30
e	Terminal Pitch	0.50	

Dimensions in millimeters.

Overall thickness A=A1+A2.

Universal Package: Sil **xxxxCNU**

Legend	**Description**
LLLLLL.LLLL	Lot Number
YY	Year of Mfr
WW	Week of Mfr
TTTTTT	Trace Code
m	Maturity Code

ePad Dimensions

		typ	max
D2	ePad Height		6.30
E2	ePad Width		6.30
ΔT	Tolerance		± 0.05

Dimensions in millimeters.

ePad is centered on the package center lines.

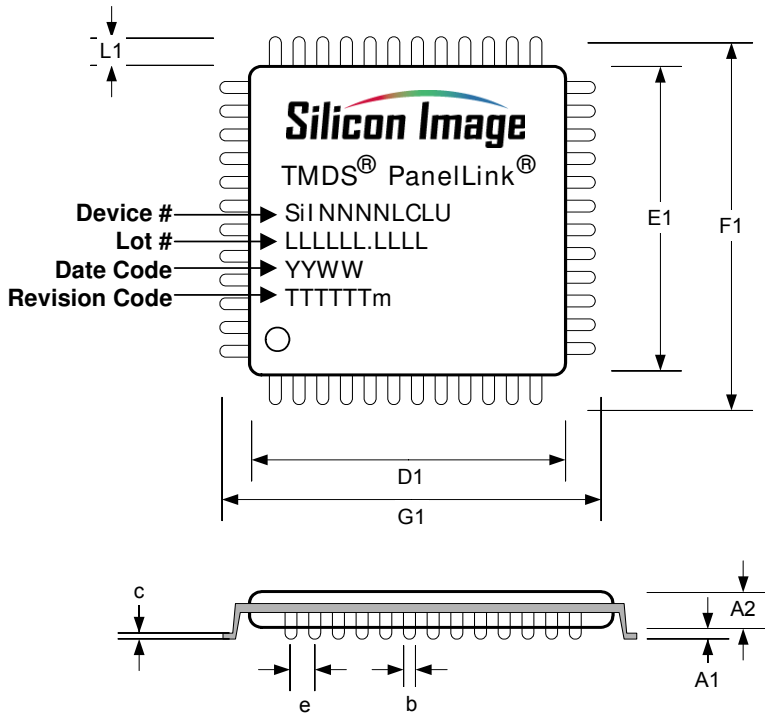
Figure 21. 64-pin QFN Package Dimensions and ePad Diagram

48-pin Ordering Information

Part Numbers of Universal package for both Standard and Pb-free applications:

SiI 1362 Tx (SDVO 1.0 Compliant): SiI1362CLU

SiI 1362A Tx (SDVO 1.1 Compliant): SiI1362ACLU



JEDEC Package Code MS026-BBC

		typ	max
A	Thickness		1.60
A1	Stand-off		0.15
A2	Body Thickness	1.40	1.45
D1	Body Size	7.00	
E1	Body Size	7.00	
F1	Footprint	9.00	
G1	Footprint	9.00	
L1	Lead Length	1.00	
b	Lead Width	0.20	0.27
c	Lead Thickness		0.20
e	Lead Pitch	0.50	

Dimensions in millimeters.
Overall thickness A=A1+A2.

Legend	Description
SiINNNNLCLU	Device number SiI1362CLU or SiI1362ACLU
LLLLLL.LLLL	Lot Number
YY	Year of Mfr
WW	Week of Mfr
TTTTTT	Trace Code
m	Maturity Code

Figure 22. 48-pin LQFP Package Dimensions

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