ISL95810

Single Digitally Controlled Potentiometer (XDCP™) Low Noise, Low Power I^2C Bus, 256 Taps

FN8090
Rev.3.01
Jun 5, 2020

The ISL95810 integrates a digitally controlled potentiometer (XDCP) on a monolithic CMOS integrated circuit.

The digitally controlled potentiometer is implemented with a combination of resistor elements and CMOS switches. The position of the wiper is controlled by you through the I^2C bus interface. The potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR) that can be directly written to and read. The content of the WR controls the position of the wiper. At power-up, the device recalls the contents of the DCP's IVR to the WR.

The DCP can be used as a 3-terminal potentiometer or as a 2-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

Related Literature

For a full list of related documents, visit our website:

- ISL95810 device page

Features

- 256 resistor taps - 0.4% resolution
- I^2C serial interface
- Wiper resistance: 70Ω typical at 3.3V
- Non-volatile storage of wiper position
- Standby current 5µA max
- Power supply: 2.7V to 5.5V
- 50kΩ, 10kΩ total resistance
- High reliability
  - Endurance: 200,000 data changes per bit per register
  - Register data retention: 50 years at T ≤ +75°C
- 8 Ld MSOP and 8 Ld TDFN packaging
- Pb-free plus anneal available (RoHS compliant)

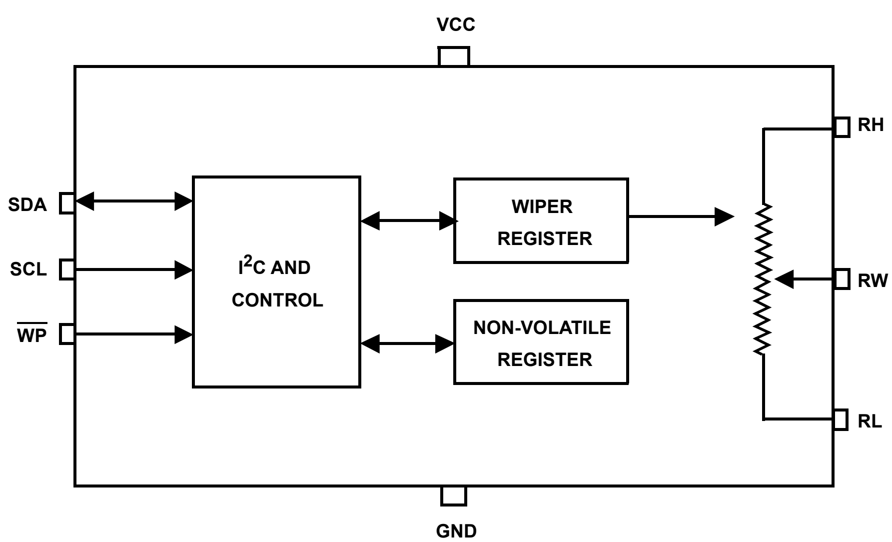


FIGURE 1. BLOCK DIAGRAM

Ordering Information

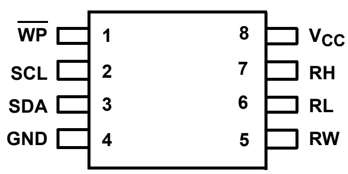
PART NUMBER (Notes 2, 3)	PART MARKING	R_{TOTAL} (kΩ)	TAPE AND REEL (UNITS) (Note 1)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)
ISL95810WIU8Z	APN	10	-	-40 to +85	8 Ld MSOP
ISL95810WIU8Z-T	APN		2.5k	-40 to +85	8 Ld MSOP
ISL95810WIRT8Z	APO		-	-40 to +85	8 Ld 3x3 TDFN
ISL95810WIRT8Z-T	APO		6k	-40 to +85	8 Ld 3x3 TDFN
ISL95810UIU8Z	AOK	50	-	-40 to +85	8 Ld MSOP
ISL95810UIU8Z-T	AOK		2.5k	-40 to +85	8 Ld MSOP
ISL95810UIRT8Z	APP		-	-40 to +85	8 Ld 3x3 TDFN
ISL95810UIRT8Z-T	APP		2.5k	-40 to +85	8 Ld 3x3 TDFN
ISL95810UART8Z-T	ADR		2.5k	-40 to +105	8 Ld 3x3 TDFN

NOTES:

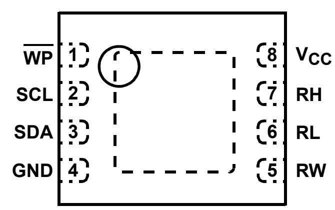
1. See TB347 **for details on reel specifications**.
2. Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL95810 device page. For more information about MSL, see TB363.

Pinouts

8 LD MSOP
TOP VIEW



8 LD TDFN
TOP VIEW



Pin Descriptions

TSSOP PIN	SYMBOL	DESCRIPTION
1	$\overline{WP}$	Hardware write protection. Active low. Prevents any “Write” operation of the I^2C interface.
2	SCL	I^2C interface clock
3	SDA	Serial data I/O for the I^2C interface
4	GND	Ground
5	RW	“Wiper” terminal of the DCP
6	RL	“Low” terminal of the DCP
7	RH	“High” terminal of the DCP
8	V_{CC}	Power supply

Absolute Maximum Ratings

Storage Temperature . . . .-65°C to +150°C
Voltage at Any Digital Interface Pin
with Respect to V_{SS} . . . . -0.3V to V_{CC}+0.3
V_{CC} . . . .-0.3V to +6V
Voltage at Any DCP Pin with
Respect to V_{SS} . . . . -0.3V to V_{CC}
Lead Temperature (Soldering, 10s) . . . .+300°C
I_W (10s) . . . . ±6mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld DFN Package (Notes 4, 5)	48	6
8 Ld MSOP Package (Notes 6, 7)	151	50

Recommended Operating Conditions

Industrial . . . .-40°C to +85°C
Extended Range . . . .-40°C to +105°C
V_{CC} . . . . 2.7V to 5.5V
Power Rating of Each DCP 5mW
Wiper Current of Each DCP. . . . .±3.0mA
Pb-Free Reflow Profile. . . . . see TB493

***CAUTION**: Stresses above those listed in “Absolute Maximum Ratings” can cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
5. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.
6. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board. See TB379.
7. For θ_{JC}, the case temperature location is taken at the package top center.

Analog Specifications

Over recommended operating conditions unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP (Note 8)	MAX	UNIT
R_H to R_L Resistance	R_{TOTAL}	W, U versions respectively		10, 50		kΩ
R_H to R_L Resistance Tolerance			-20		+20	%
Wiper Resistance	R_W	V_{CC} = 3.3V at +25°C Wiper current = V_{CC}/R_{TOTAL}		70	200	Ω
Potentiometer Capacitance (Note 22)	$C_H/C_L/C_W$			10/10/25		pF
Leakage on DCP Pins (Note 22)	I_{LkgDCP}	Voltage at pin from GND to V_{CC}		0.1	1	µA
VOLTAGE DIVIDER MODE (0V at RL; V_{CC} at RH; measured at RW, unloaded)						
Integral Non-Linearity	INL (Note 13)		-1		1	LSB (Note 9)
Differential Non-Linearity	DNL (Note 12)	Monotonic over all tap positions — W option	-0.75		-0.75	LSB (Note 9)
		U option	-0.5		-0.5	LSB (Note 9)
Zero-Scale Error	ZSerror (Note 10)	W option	0	1	7	LSB (Note 9)
		U option	0	0.5	2	
Full-Scale Error	FSerror (Note 11)	W option	-7	-1	0	LSB (Note 9)
		U option	-2	-0.5	0	
Ratiometric Temperature Coefficient	TC_V (Notes 14, 15 22)	DCP Register set to 80 hex		±4		ppm/°C
RESISTOR MODE (Measurements between RW and RL with RH not connected, or between RW and RH with RL not connected)						
Integral Non-Linearity	RINL (Note 19)	DCP register set between 20 hex and FF hex. Monotonic over all tap positions	-1		1	MI (Note 16)
Differential Non-Linearity	RDNL (Note 12)	DCP register set between 20 hex and FF hex. Monotonic over all tap positions — W option	-0.75		-0.75	MI (Note 16)
		U option	-0.5		-0.5	MI (Note 16)
Offset	Roffset (Note 17)	W option	0	1	7	MI (Note 16)
		U option	0	0.5	2	MI (Note 16)
Resistance Temperature Coefficient	TC_R (Notes 20, 21, 22)	DCP register set between 20 hex and FF hex		±165		ppm/°C

Operating Specifications

Over the recommended operating conditions unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP (Note 8)	MAX	UNIT
V_{CC} Supply Current (Volatile write/read)	I_{CC1} (Note 24)	f_{SCL} = 400kHz; SDA = Open; (for I^2C, Active, Read and Volatile Write States only)			1	mA
V_{CC} Supply Current (Nonvolatile Write)	I_{CC2} (Note 24)	f_{SCL} = 400kHz; SDA = Open; (for I^2C, Active, Nonvolatile Write State only)			3	mA
V_{CC} Current (Standby)	I_{SB} (Note 24)	V_{CC} = +5.5V, I^2C Interface in Standby State			5	µA
		V_{CC} = +3.6V, I^2C Interface in Standby State			2	µA
Leakage Current, at Pins SDA, SCL, and WP Pins	I_{LkgDig}	Voltage at pin from GND to V_{CC}	-10		10	µA
DCP Wiper Response Time	t_{DCP} (Note 22)	SCL falling edge of last bit of DCP Data Byte to wiper change			1	µs
Power-On Recall Voltage	Vpor	Minimum V_{CC} at which memory recall occurs	1.8		2.6	V
V_{CC} Ramp Rate	V_{CC}Ramp		0.2			V/ms
Power-Up Delay	t_D (Note 22)	V_{CC} above Vpor, to DCP Initial Value Register recall completed, and I^2C Interface in standby state			3	ms
EEPROM SPECIFICATIONS						
EEPROM Endurance			200,000			Cycles
EEPROM Retention		Temperature ≤ +75°C	50			Years
SERIAL INTERFACE SPECIFICATIONS						
WP, SDA, and SCL Input Buffer LOW Voltage	V_{IL}		-0.3		0.3*V_{CC}	V
WP, SDA, and SCL Input Buffer HIGH Voltage	V_{IH}		0.7*V_{CC}		V_{CC}+0.3	V
SDA and SCL Input Buffer Hysteresis	Hysteresis (Note 13)		0.05*V_{CC}			V
SDA Output Buffer LOW Voltage, Sinking 4mA	V_{OL} (Note 22)		0		0.4	V
WP, SDA, and SCL Pin Capacitance	Cpin (Note 22)				10	pF
SCL Frequency	f_{SCL}				400	kHz
Pulse Width Suppression Time at SDA and SCL Inputs	t_{IN} (Note 22)	Any pulse narrower than the max spec is suppressed.			50	ns
SCL Falling Edge to SDA Output Data Valid	t_{AA} (Note 22)	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window.			900	ns
Time the Bus Must be Free Before the Start of a New Transmission	t_{BUF} (Note 22)	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition.	1300			ns
Clock LOW Time	t_{LOW}	Measured at the 30% of V_{CC} crossing.	1300			ns
Clock HIGH Time	t_{HIGH}	Measured at the 70% of V_{CC} crossing.	600			ns
START Condition Setup Time	$t_{SU:STA}$	SCL rising edge to SDA falling edge. Both crossing 70% of V_{CC}.	600			ns
START Condition Hold Time	$t_{HD:STA}$	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}.	600			ns
Input Data Setup Time	$t_{SU:DAT}$	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}	100			ns
Input Data Hold Time	$t_{HD:DAT}$	From SCL rising edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window.	0			ns
STOP Condition Setup Time	$t_{SU:STO}$	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}.	600			ns
STOP Condition Hold Time for Read, or Volatile Only Write	$t_{HD:STO}$	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{CC}.	600			ns
STOP Condition Hold Time for Non-Volatile Write	$t_{HD:STO:NV}$	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{CC}.	2			µs

Operating Specifications

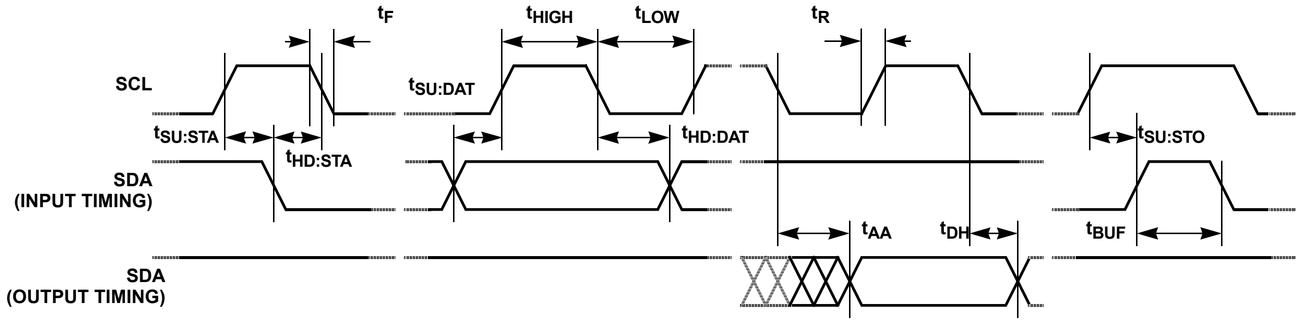
Over the recommended operating conditions unless otherwise specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP (Note 8)	MAX	UNIT
Output Data Hold Time	t_{DH} (Note 22)	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window.	0			ns
SDA and SCL Rise Time	t_R (Note 22)	From 30% to 70% of V_{CC}	20 + 0.1 * Cb		250	ns
SDA and SCL Fall Time	t_F (Note 22)	From 70% to 30% of V_{CC}	20 + 0.1 * Cb		250	ns
Capacitive Loading of SDA or SCL	Cb (Note 22)	Total on-chip and off-chip	10		400	pF
SDA and SCL Bus Pull-Up Resistor Off-Chip	Rpu (Note 22)	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2~2.5kΩ. For Cb = 40pF, max is about 15~20kΩ	1			kΩ
Non-Volatile Write Cycle Time	t_{WP} (Notes 22, 23)			12	20	ms
$\overline{WP}$ Setup Time	$t_{SU:WP}$	Before START condition	600			ns
$\overline{WP}$ Hold Time	$t_{HD:WP}$	After STOP condition	600			ns

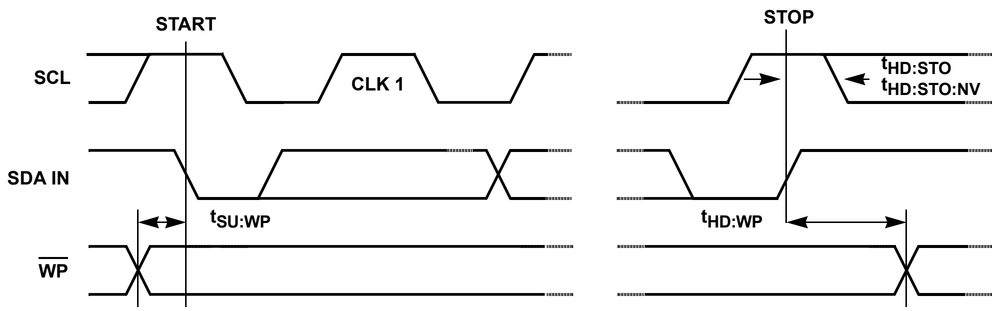
NOTES:

8. Typical values are for T_A = +25°C and 3.3V supply voltage.
9. LSB: $[V(RW)_{255} – V(RW)_0]/255$. $V(RW)_{255}$ and $V(RW)_0$ are V(RW) for the DCP register set to FF hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
10. ZS error = $V(RW)_0/LSB$.
11. FS error = $[V(RW)_{255} – V_{CC}]/LSB$.
12. DNL = {[V(RW)i – V(RW)i-1]/LSB}-1, for i = 1 to 255. i is the DCP register setting.
13. INL = $[V(RW)_i – (i \cdot LSB – V(RW)_0)]/LSB$ for i = 1 to 255.
14. $TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{125°C}$ for i = 16 to 240 decimal, T = -40°C to +85°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
15. $TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{145°C}$ for i = 16 to 240 decimal, T = -40°C to +105°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
16. MI = $|R_{255} – R_0|/255$. R_{255} and R_0 are the measured resistances for the DCP register set to FF hex and 00 hex respectively. Roffset = R_0/MI, when measuring between RW and RL.
17. Roffset = R_{255}/MI, when measuring between RW and RH.
18. RDNL = [(Ri – Ri-1)/MI]-1, for i = 32 to 255.
19. RINL = $[R_i – (MI \cdot i) – R_0]/MI$, for i = 32 to 255.
20. $TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{125°C}$ for i = 32 to 255, T = -40°C to +85°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
21. $TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{145°C}$ for i = 32 to 255, T = -40°C to +105°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
22. This parameter is not 100% tested.
23. t_{WC} is the minimum cycle time to be allowed for any non-volatile Write by the user, unless Acknowledge Polling is used. It is the time from a valid STOP condition at the end of a Write sequence of a I^2C serial interface Write operation, to the end of the self-timed internal non-volatile write cycle.
24. V_{IL} = 0V, V_{IH} = V_{CC}

SDA vs SCL Timing



WP Pin Timing



Typical Performance Curves

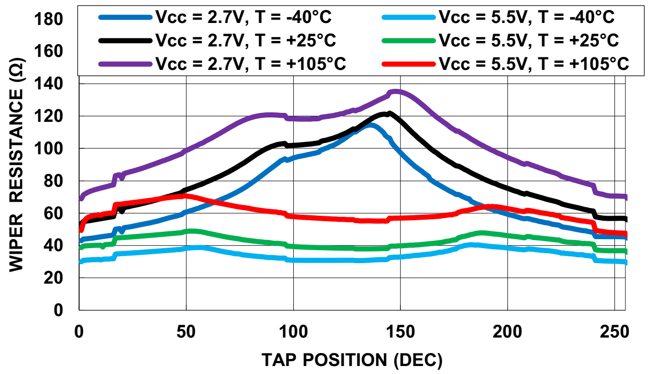


FIGURE 2. WIPER RESISTANCE vs TAP POSITION [I(RW) = V_{CC} / R_{TOTAL}] for 50kΩ

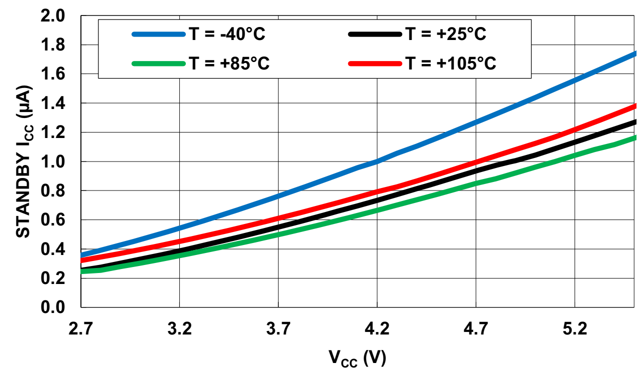


FIGURE 3. STANDBY I_{CC} vs V_{CC}

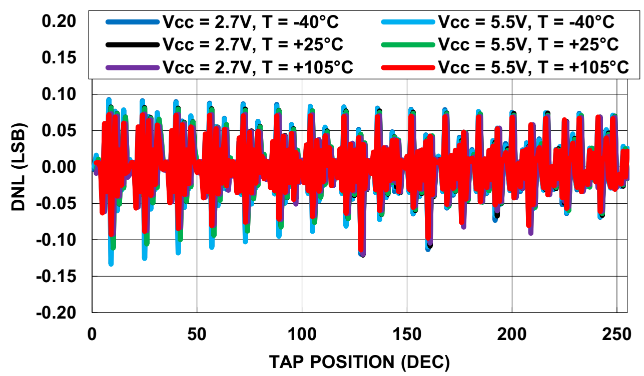


FIGURE 4. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 50kΩ ACROSS -40°C to +105°C

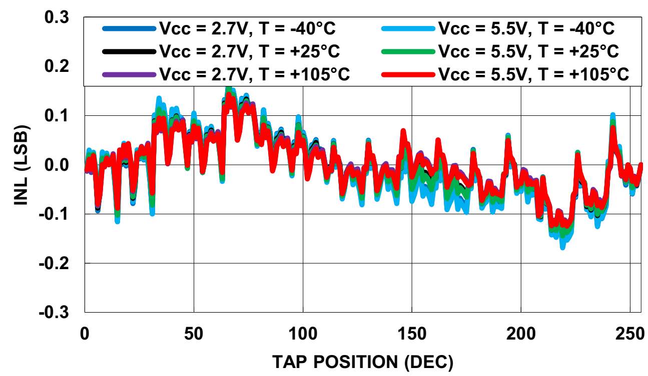


FIGURE 5. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 50kΩ

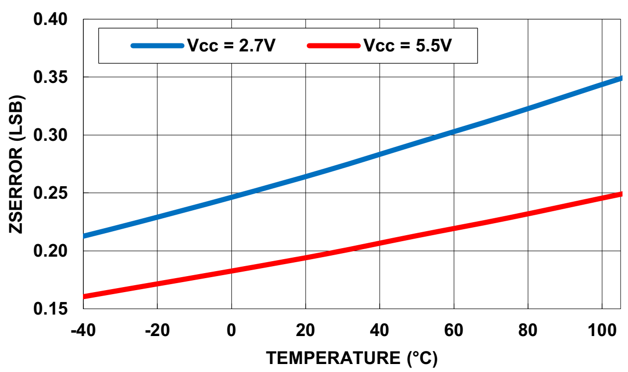


FIGURE 6. ZSERROR vs TEMPERATURE FOR 50kΩ

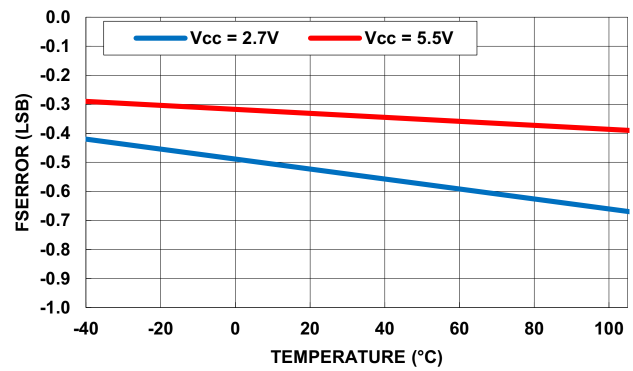


FIGURE 7. FSERROR vs TEMPERATURE FOR 50kΩ

Typical Performance Curves (Continued)

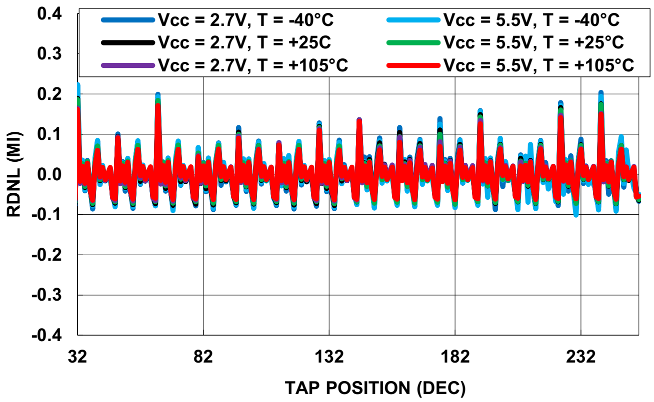


FIGURE 8. DNL vs TAP POSITION IN RHEOSTAT MODE FOR 50kΩ ACROSS -40°C to +105°C

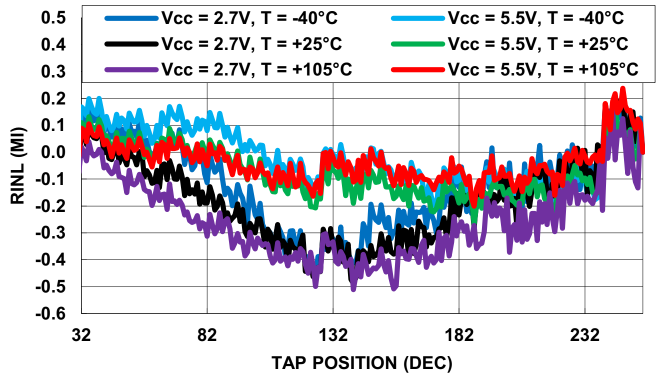


FIGURE 9. INL vs TAP POSITION IN RHEOSTAT MODE FOR 50kΩ ACROSS -40°C to +105°C

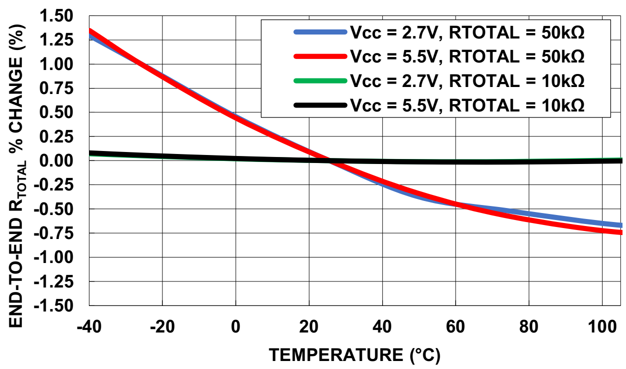


FIGURE 10. END TO END R_{TOTAL} % CHANGE vs TEMPERATURE

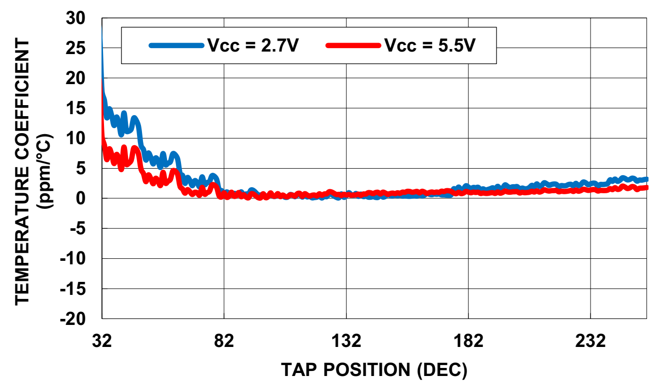


FIGURE 11. TC FOR VOLTAGE DIVIDER MODE IN PPM

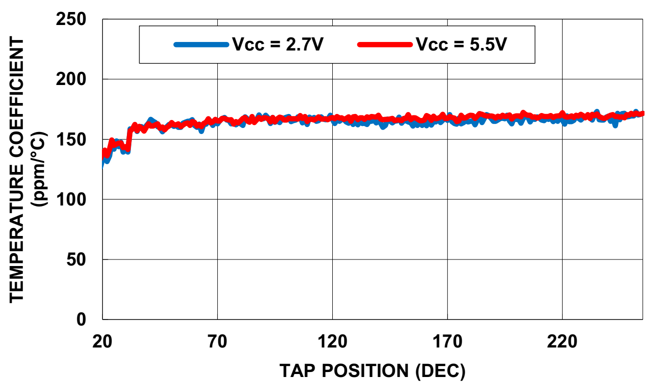


FIGURE 12. TC FOR RHEOSTAT MODE IN PPM

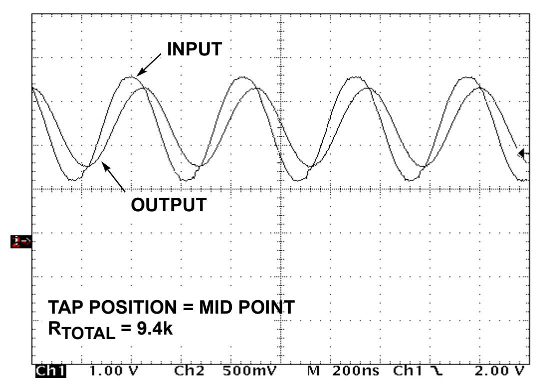


FIGURE 13. FREQUENCY RESPONSE (2.2MHz)

Typical Performance Curves (Continued)

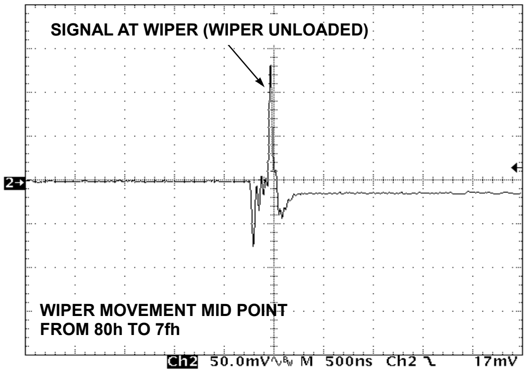


FIGURE 14. MIDSCALE GLITCH, CODE 80h to 7Fh (WIPER 0)

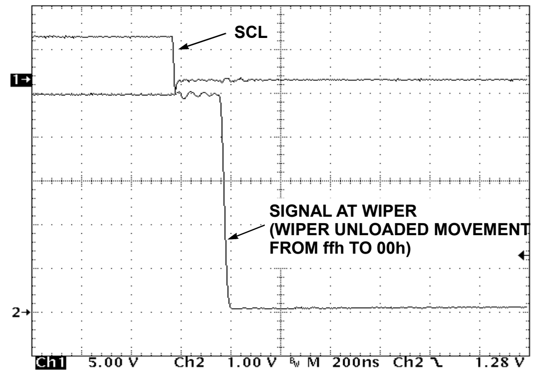


FIGURE 15. LARGE SIGNAL SETTLING TIME

Principles of Operation

The ISL95810 is an integrated circuit incorporating one DCP with its associated registers, non-volatile memory, and a I^2C serial interface providing direct communication between a host and the potentiometer and memory.

DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of the DCP are equivalent to the fixed terminals of a mechanical potentiometer (RH and RL pins). The RW pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Register (WR). The DCP has its own WR. When the WR of the DCP contains all zeroes (WR<7:0>: 00h), its wiper terminal (RW) is closest to its “Low” terminal (RL). When the WR of the DCP contains all ones (WR<7:0>: FFh), its wiper terminal (RW) is closest to its “High” terminal (RH). As the value of the WR increases from all zeroes (00h) to all ones (255 decimal), the wiper moves monotonically from the position closest to RL to the closest to RH. At the same time, the resistance between RW and RL increases monotonically, while the resistance between RH and RW decreases monotonically.

While the ISL95810 is being powered up, The WR is reset to 80h (128 decimal), which locates RW roughly at the center between RL and RH. Soon after the power supply voltage becomes large enough for reliable non-volatile memory reading, the ISL95810 reads the value stored in non-volatile Initial Value Registers (IVRs) and loads it into the WR.

Note: The ISL95810 is programmed from the factory with the wiper set to mid-point (128) position: 0x80

The WR and IVR can be read or written directly using the I^2C serial interface as described in the following sections.

Memory Description

The ISL95810 volatile and non-volatile registers are accessed by I^2C interface operations at addresses 0 and 2 decimal. The non-volatile byte at addresses 0 contains the initial value loaded at power-up into the volatile Wiper Register (WR) of the DCP. The byte at address 1 is reserved; the user should not write to it, and its value should be ignored if read.

The volatile WR, and the non-volatile Initial Value Register (IVR) of the DCP are accessed with the same Address Byte, set to 00 hex in both cases.

A volatile byte at address 2 decimal, controls what byte is read or written when accessing DCP registers: the WR, the IVR, or both.

When the byte at address 2 is all zeroes, which is the default at power-up:

- A read operation to addresses 0 outputs the value of the non-volatile IVR.
- A write operation to addresses 0 writes the same value to the WR and IVR of the corresponding DCP.

When the byte at address 2 is 80h (128 decimal):

- A read operation to addresses 0 outputs the value of the volatile WR.
- A write operation to addresses 0 only writes to the corresponding volatile WR.

It is not possible to write to an IVR without writing the same value to its corresponding WR.

00h and 80h are the only values that should be written to address 2. All other values are reserved and must not be written to address 2.

The ISL95810 is pre-programed with 80h in the IVR.

TABLE 1. MEMORY MAP

ADDRESS	NON-VOLATILE	VOLATILE
2	-	Access Control
1	Reserved	
0	IVR	WR
NOTE: WR: Wiper Register, IVR: Initial value Register.		

I^2C Serial Interface

The ISL95810 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations; therefore, the ISL95810 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 16 on page 10). On power-up of the ISL95810 the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL95810 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 16). A START condition is ignored during the power-up sequence and during internal non-volatile write cycles.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 16). A STOP condition at the end of a read operation, or at the end of a write operation to volatile bytes only places the device in its standby mode. A STOP condition during a write operation to a non-volatile byte, initiates an internal non-volatile write cycle. The device enters its standby state when the internal non-volatile write cycle is completed.

An Acknowledge (ACK), is a software convention that indicates a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 17 on page 11).

The ISL95810 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and responds again after successful receipt of an Address Byte. The ISL95810 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

A valid Identification Byte contains 0101000 as the seven MSBs. The LSB in the Read/$\overline{\text{Write}}$ bit. Its value is “1” for a Read operation, and “0” for a Write operation (see Table 2).

TABLE 2. IDENTIFICATION BYTE FORMAT

0	1	0	1	0	0	0	R/$\overline{\text{W}}$
(MSB)							(LSB)

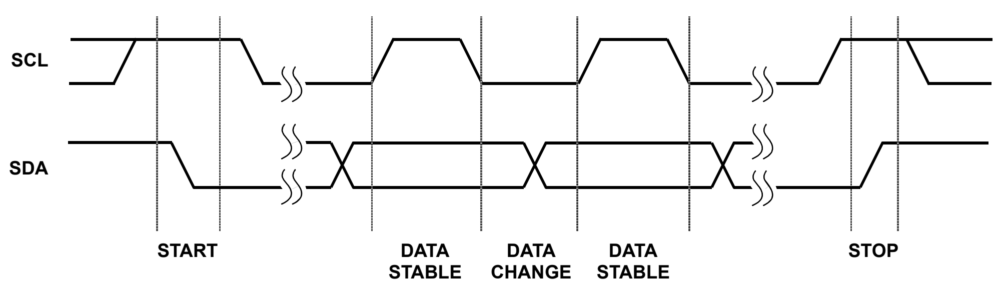


FIGURE 16. VALID DATA CHANGES, START, AND STOP CONDITIONS

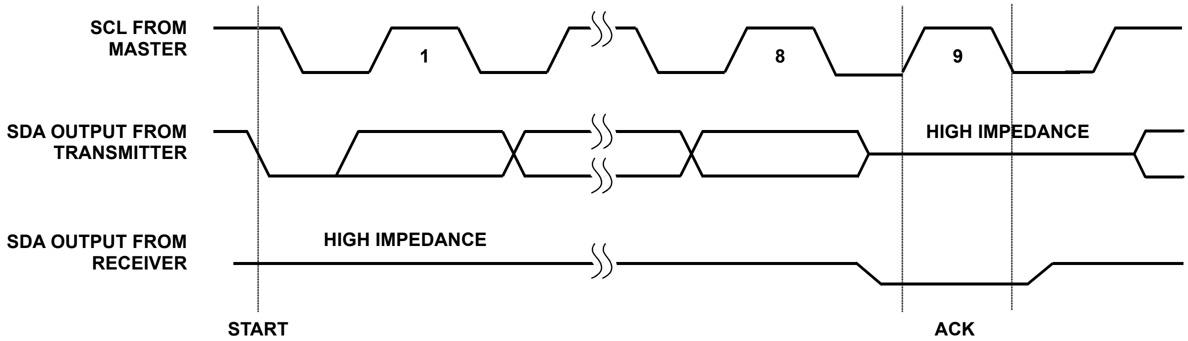


FIGURE 17. ACKNOWLEDGE RESPONSE FROM RECEIVER

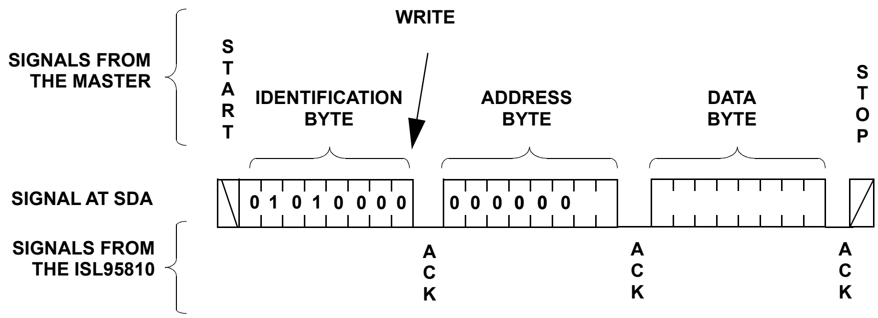


FIGURE 18. BYTE WRITE SEQUENCE

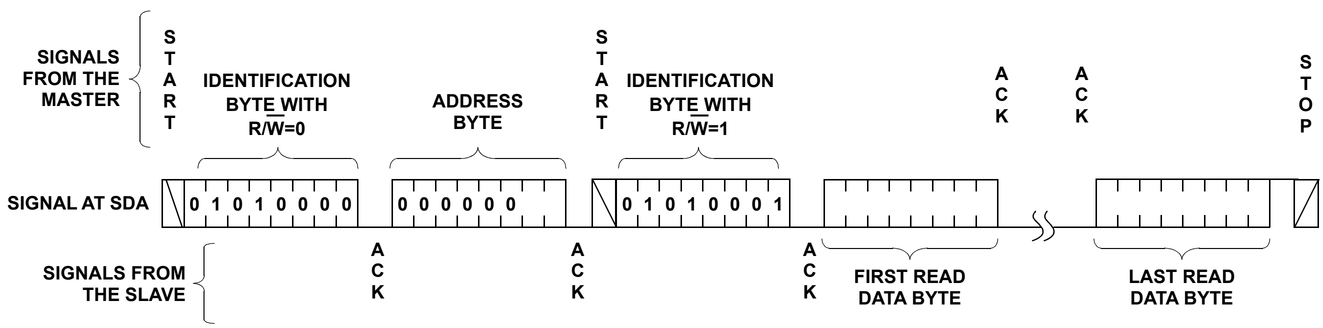


FIGURE 19. READ SEQUENCE

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL95810 responds with an ACK. At this time, if the Data Byte is to be written only to volatile registers, then the device enters its standby state. If the Data Byte is to be written also to non-volatile memory, the ISL95810 begins its internal write cycle to non-volatile memory. During the internal non-volatile write cycle, the device ignores transitions at the SDA and SCL pins, and the SDA output is at a high impedance state. When the internal non-volatile write cycle is completed, the ISL95810 enters its standby state (see Figure 18 on page 11).

The byte at address 02h determines if the Data Byte is to be written to volatile and/or non-volatile memory (see "Memory Description" on page 9).

Data Protection

The $\overline{WP}$ pin has to be at logic HIGH to perform any Write operation to the device. When the $\overline{WP}$ is active (LOW) the device ignores Data Bytes of a Write Operation, does not respond to the Data Bytes with an ACK, and instead, goes to its standby state waiting for a new START condition.

A STOP condition also acts as a protection of non-volatile memory. A valid Identification Byte, Address Byte, and total number of SCL pulses act as a protection of both volatile and non-volatile registers. During a Write sequence, the Data Byte is loaded into an internal shift register as it is received. If the Address Byte is 0 or 2, the Data Byte is transferred to the Wiper Register (WR) or to the Access Control Register respectively, at the falling edge of the SCL pulse that loads the Last Significant Bit (LSB) of the Data Byte. If the Address Byte is 0, and the Access Control Register is all zeros (default), then the STOP condition initiates the internal write cycle to non-volatile memory.

Read Operation

A Read operation consist of a three byte instruction followed by one or more Data Bytes (see Figure 19 on page 11). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to "0", an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to "1". After each of the three bytes, the ISL95810 responds with an ACK. Then the ISL95810 then transmits the Data Byte. The master then terminates the read operation (issuing a STOP condition) following the last bit of the Data Byte (see Figure 19).

The byte at address 02h determines if the Data Bytes being read are from volatile or non-volatile memory (see "Memory Description" on page 9.)

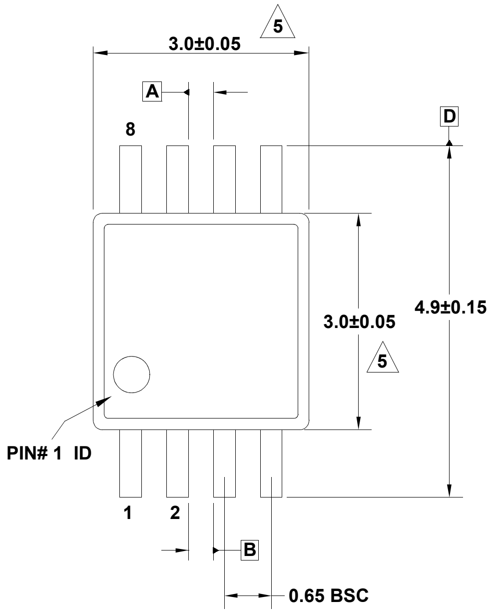
Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

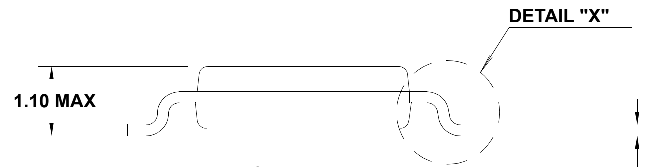
DATE	REVISION	CHANGE
Jun 5, 2020	3.01	Added thermal information to document.
Sep 6, 2019	3.00	Updated links throughout. Added Related Literature section. Updated ordering information table by removing retired parts, adding tape and reel information, added ISL95810UART8Z-T (-40°C to +105°C temperature option), updating notes, and moving to second page. Updated the typical value for the Resistance Temperature Coefficient from ±45 to ±165 on page 4. Added extended range (-40°C to +105°C temperature option) to the recommended operating conditions section. Updated Notes 8 and 14 on page 6. Added Notes 11 and 17. Updated Figures 1 through 11. Added note to DCP Description section. Updated M8.118 to the latest revision changes are as follows: - Updated to new format by adding land pattern and moving dimensions from table onto drawing. - Corrected lead width dimension in side view 1 from "0.25 - 0.036" to "0.25 - 0.36". Replaced POD L8.3X3B with POD L8.3X3A. Updated disclaimer.

Package Outline Drawings

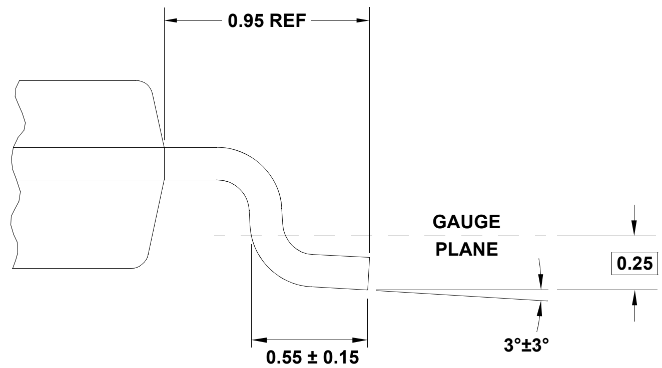
For the most recent package outline drawing, see M8.118.
M8.118
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE
Rev 4, 7/11



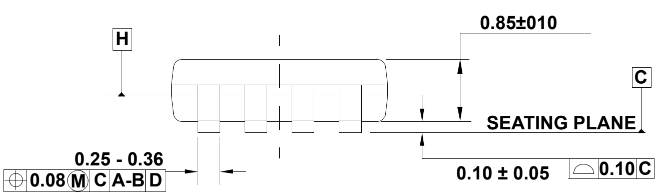
TOP VIEW



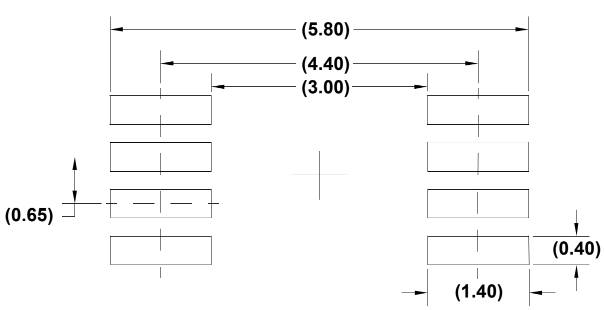
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

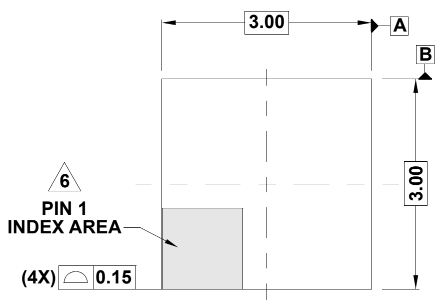
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

For the most recent package outline drawing, see L8.3x3A.

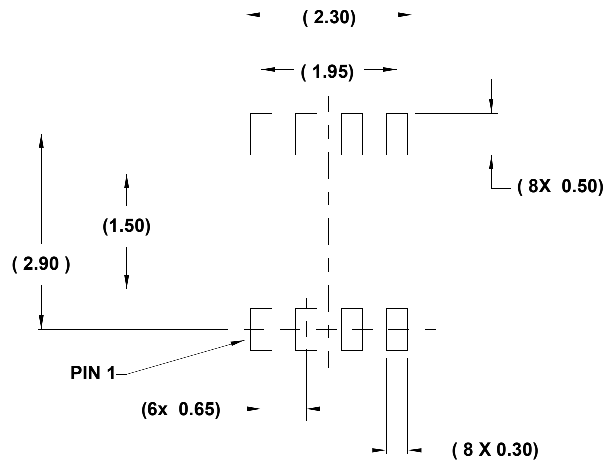
L8.3x3A

8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

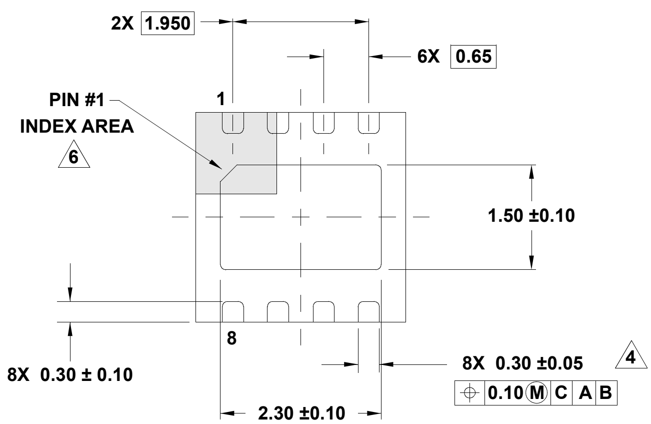
Rev 5, 5/15



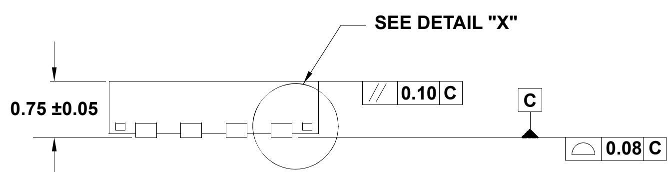
TOP VIEW



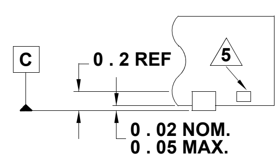
TYPICAL RECOMMENDED LAND PATTERN



BOTTOM VIEW



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.20mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229 WEEC-2 except for the foot length.

IMPORTANT NOTICE AND DISCLAIMER

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/