

256K (32K x 8) Static RAM

Features

- **Temperature Ranges**
 - Industrial: -40°C to 85°C
 - Automotive-A: -40°C to 85°C
- **Single 3.3V power supply**
- **Ideal for low-voltage cache memory applications**
- **High speed: 12 ns**
- **Low active power**
 - 180 mW (max.)
- **Low-power alpha immune 6T cell**
- **Available in Pb-free and non Pb-free Plastic SOJ and TSOP I packages**

expansion is provided by an active LOW Chip Enable (\overline{CE}) and active LOW Output Enable (\overline{OE}) and tristate drivers. The device has an automatic power-down feature, reducing the power consumption by more than 95% when deselected.

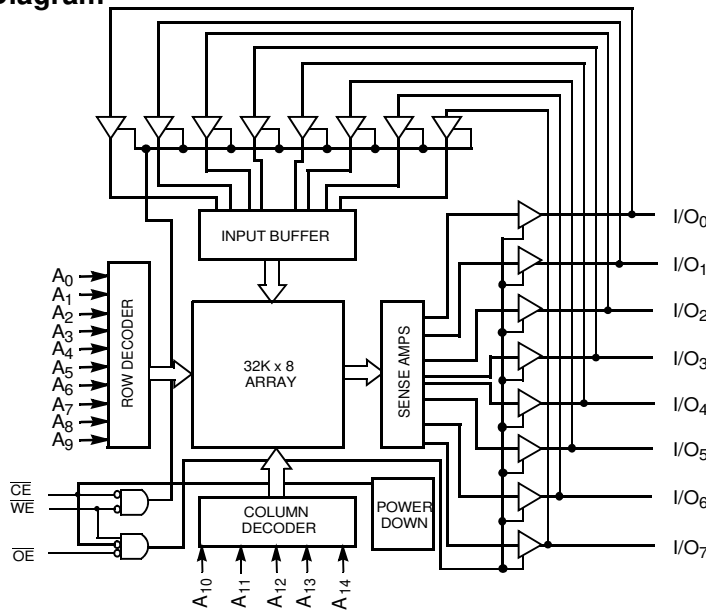
An active LOW Write Enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE} and \overline{WE} inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, \overline{CE} and \overline{OE} active LOW, while \overline{WE} remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and Write Enable (\overline{WE}) is HIGH. The CY7C1399BN is available in 28-pin standard 300-mil-wide SOJ and TSOP Type I packages.

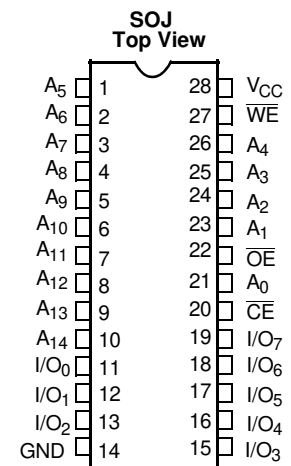
Functional Description^[1]

The CY7C1399BN is a high-performance 3.3V CMOS Static RAM organized as 32,768 words by 8 bits. Easy memory

Logic Block Diagram



Pin Configurations



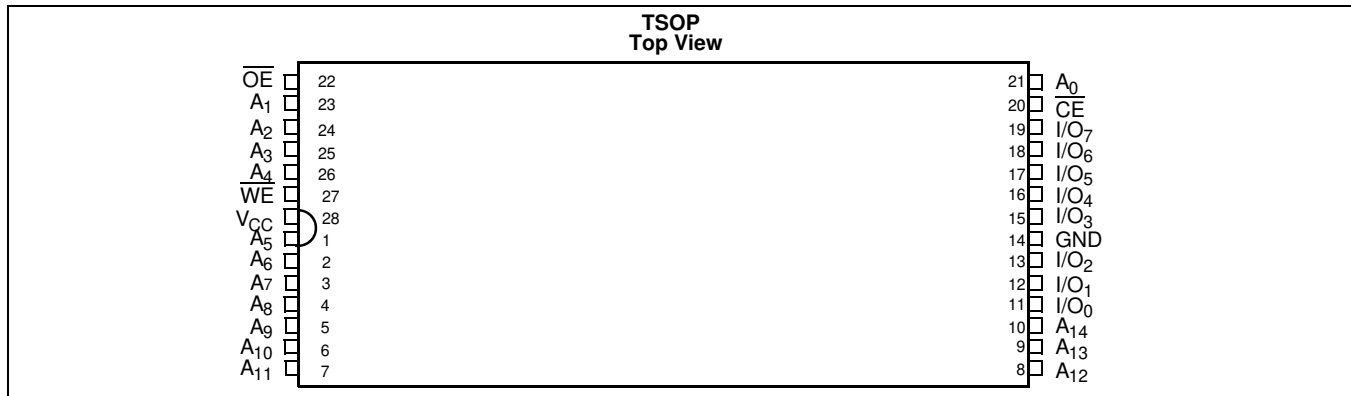
Selection Guide

| | | -12 | -15 |
|-----------------------------------|----------------|-----|-----|
| Maximum Access Time (ns) | | 12 | 15 |
| Maximum Operating Current (mA) | | 55 | 50 |
| Maximum CMOS Standby Current (μA) | Commercial | 500 | |
| | Commercial (L) | 50 | |
| | Industrial | 500 | 500 |
| | Automotive-A | | 500 |

Note:

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature -65°C to +150°C
- Ambient Temperature with Power Applied -55°C to +125°C
- Supply Voltage on V_{CC} to Relative GND^[2] -0.5V to +4.6V
- DC Voltage Applied to Outputs in High Z State^[2] -0.5V to V_{CC} + 0.5V
- DC Input Voltage^[2] -0.5V to V_{CC} + 0.5V

- Output Current into Outputs (LOW) 20 mA
- Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)
- Latch-Up Current >200 mA

Operating Range

| Range | Ambient Temperature | V _{CC} |
|--------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 3.3V ±300 mV |
| Industrial | -40°C to +85°C | |
| Automotive-A | -40°C to +85°C | |

Electrical Characteristics Over the Operating Range^[1]

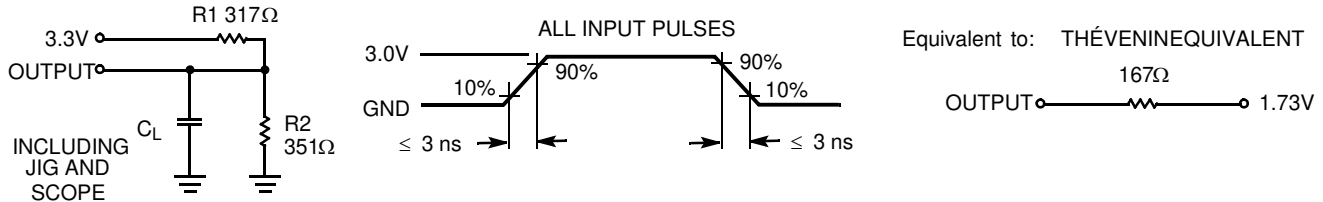
| Parameter | Description | Test Conditions | -12 | | -15 | | Unit |
|------------------|--|---|------------|------------------------|------|------------------------|------|
| | | | Min. | Max. | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -2.0 mA | 2.4 | | 2.4 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 4.0 mA | | 0.4 | | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.2 | V _{CC} + 0.3V | 2.2 | V _{CC} + 0.3V | V |
| V _{IL} | Input LOW Voltage ^[2] | | -0.3 | 0.8 | -0.3 | 0.8 | V |
| I _{IX} | Input Leakage Current | | -1 | +1 | -1 | +1 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _I ≤ V _{CC} , Output Disabled | -5 | +5 | -5 | +5 | μA |
| I _{CC} | V _{CC} Operating Supply Current | V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC} | | 55 | | 50 | mA |
| I _{SB1} | Automatic CE Power-Down Current—TTL Inputs | Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} , or V _{IN} ≤ V _{IL} , f = f _{MAX} | Comm'l | 5 | | | mA |
| | | | Comm'l (L) | 4 | | | mA |
| | | | Ind'l | 5 | | 5 | mA |
| | | | Auto-A | | | 5 | mA |
| I _{SB2} | Automatic CE Power-Down Current—CMOS Inputs ^[3] | Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, WE ≥ V _{CC} - 0.3V or WE ≤ 0.3V, f = f _{MAX} | Comm'l | 500 | | | μA |
| | | | Comm'l (L) | 50 | | | μA |
| | | | Ind'l | 500 | | 500 | μA |
| | | | Auto-A | | | 500 | μA |

Notes:

- 2. Minimum voltage is equal to -2.0V for pulse durations of less than 20 ns.
- 3. Device draws low standby current regardless of switching on the addresses.

Capacitance^[4]

| Parameter | Description | Test Conditions | Max. | Unit |
|-----------------------------|--------------------|---|------|------|
| C _{IN} : Addresses | Input Capacitance | T _A = 25°C, f = 1 MHz, V _{CC} = 3.3V | 5 | pF |
| C _{IN} : Controls | | | 6 | pF |
| C _{OUT} | Output Capacitance | | 6 | pF |

AC Test Loads and Waveforms^[5]

Switching Characteristics Over the Operating Range^[5]

| Parameter | Description | -12 | | -15 | | Unit |
|-------------------------------------|--|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | |
| Read Cycle | | | | | | |
| t _{RC} | Read Cycle Time | 12 | | 15 | | ns |
| t _{AA} | Address to Data Valid | | 12 | | 15 | ns |
| t _{OHA} | Data Hold from Address Change | 3 | | 3 | | ns |
| t _{ACE} | \overline{CE} LOW to Data Valid | | 12 | | 15 | ns |
| t _{DOE} | \overline{OE} LOW to Data Valid | | 5 | | 6 | ns |
| t _{LZOE} | \overline{OE} LOW to Low Z ^[6] | 0 | | 0 | | ns |
| t _{HZOE} | \overline{OE} HIGH to High Z ^[6, 7] | | 5 | | 6 | ns |
| t _{LZCE} | \overline{CE} LOW to Low Z ^[6] | 3 | | 3 | | ns |
| t _{HZCE} | \overline{CE} HIGH to High Z ^[6, 7] | | 6 | | 7 | ns |
| t _{PU} | \overline{CE} LOW to Power-Up | 0 | | 0 | | ns |
| t _{PD} | \overline{CE} HIGH to Power-Down | | 12 | | 15 | ns |
| Write Cycle^[8, 9] | | | | | | |
| t _{WC} | Write Cycle Time | 12 | | 15 | | ns |
| t _{SCE} | \overline{CE} LOW to Write End | 8 | | 10 | | ns |
| t _{AW} | Address Set-Up to Write End | 8 | | 10 | | ns |
| t _{HA} | Address Hold from Write End | 0 | | 0 | | ns |
| t _{SA} | Address Set-Up to Write Start | 0 | | 0 | | ns |
| t _{PWE} | \overline{WE} Pulse Width | 8 | | 10 | | ns |
| t _{SD} | Data Set-Up to Write End | 7 | | 8 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | 0 | | ns |
| t _{HZWE} | \overline{WE} LOW to High Z ^[8] | | 7 | | 7 | ns |
| t _{LZWE} | \overline{WE} HIGH to Low Z ^[6] | 3 | | 3 | | ns |

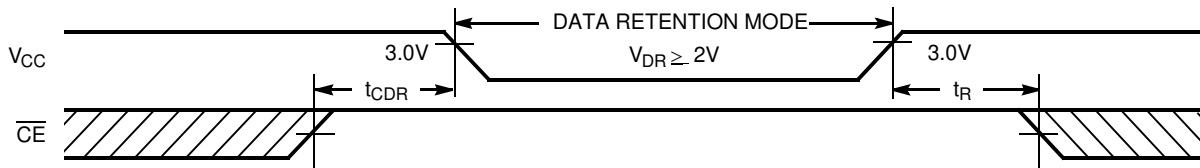
Notes:

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and capacitance C_L = 30 pF.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE}, t_{HZCE}, t_{HZWE} are specified with C_L = 5 pF as in AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for write cycle #3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics (Over the Operating Range - L version only)

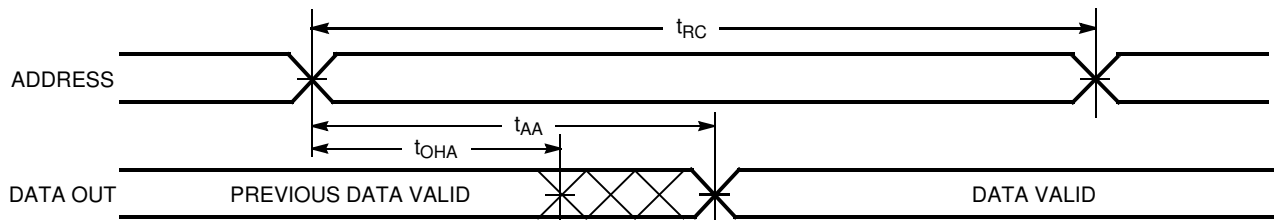
| Parameter | Description | Conditions | Min. | Max. | Unit |
|------------|--------------------------------------|---|----------|------|---------|
| V_{DR} | V_{CC} for Data Retention | | 2.0 | | V |
| I_{CCDR} | Data Retention Current | $V_{CC} = V_{DR} = 2.0V$, $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ | 0 | 20 | μA |
| t_{CDR} | Chip Deselect to Data Retention Time | | 0 | | ns |
| t_R | Operation Recovery Time | | t_{RC} | | ns |

Data Retention Waveform

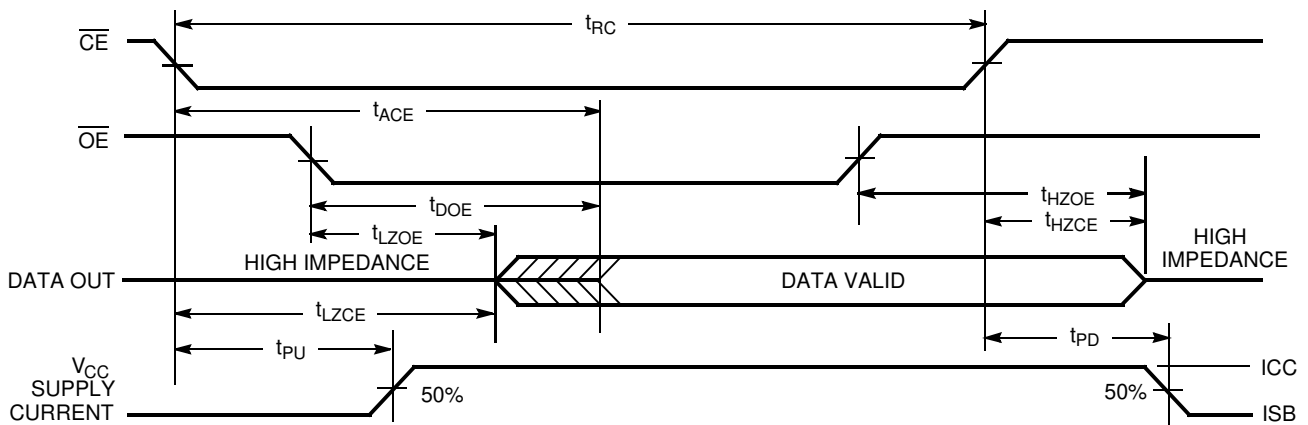


Switching Waveforms

Read Cycle No. 1^[10, 11]



Read Cycle No. 2^[11, 12]

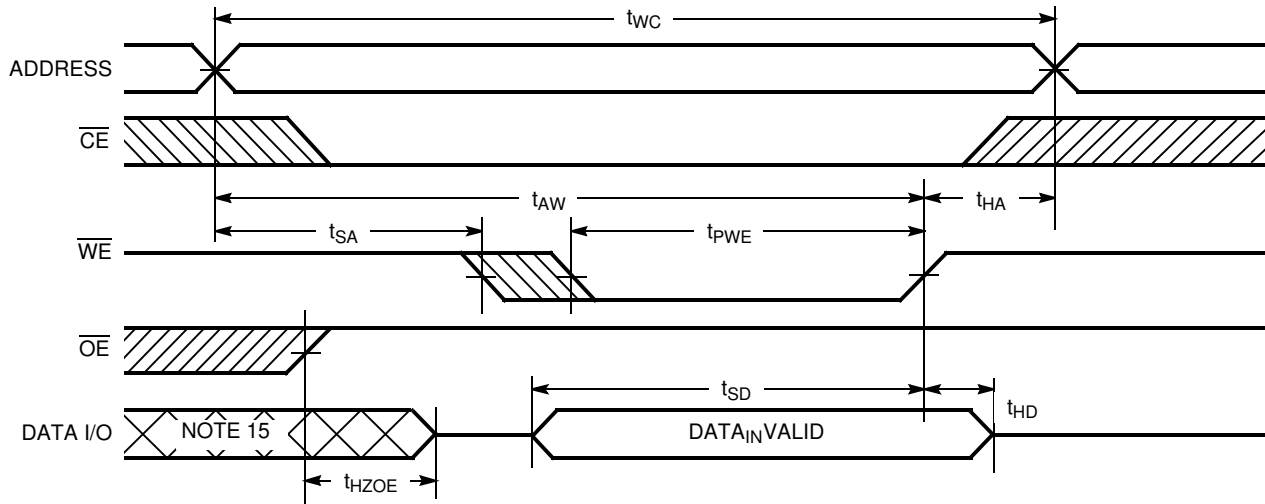


Notes:

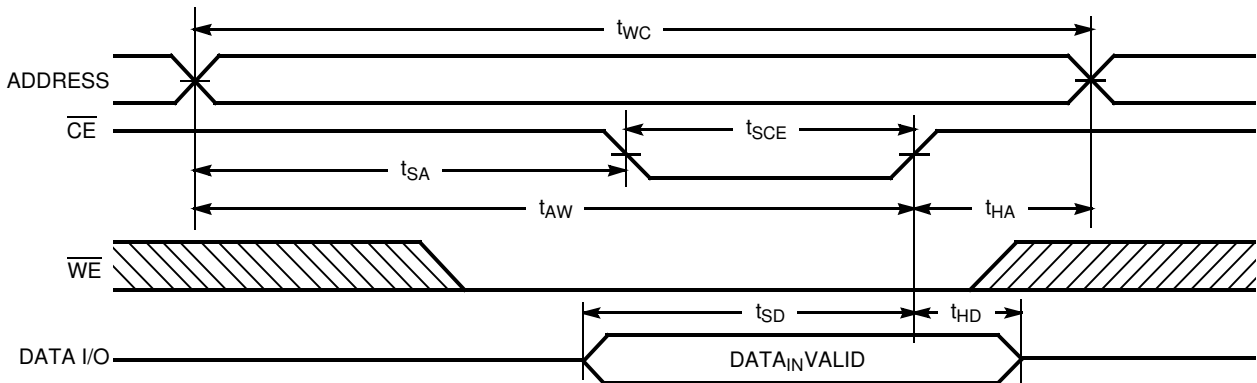
- 10. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
- 11. \overline{WE} is HIGH for read cycle.
- 12. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

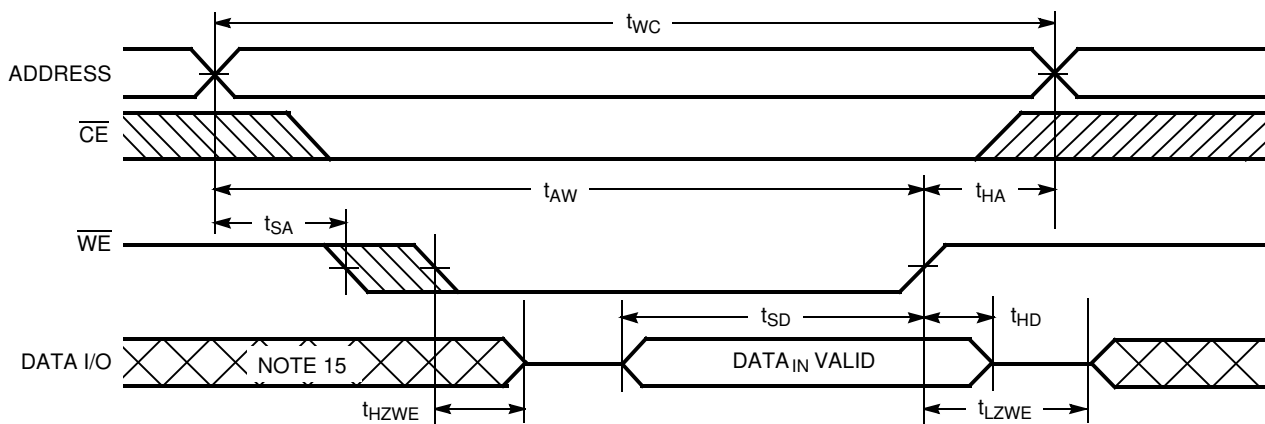
Write Cycle No. 1 (\overline{WE} Controlled)^[8, 13, 14]



Write Cycle No. 2 (\overline{CE} Controlled)^[8, 13, 14]



Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[9, 14]



- Notes:**
- 13. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
 - 14. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
 - 15. During this period, the I/Os are in the output state and input signals should not be applied.

Truth Table

| \overline{CE} | \overline{WE} | \overline{OE} | Input/Output | Mode | Power |
|-----------------|-----------------|-----------------|--------------|---------------------------|----------------------|
| H | X | X | High Z | Deselect/Power-Down | Standby (I_{SB}) |
| L | H | L | Data Out | Read | Active (I_{CC}) |
| L | L | X | Data In | Write | Active (I_{CC}) |
| L | H | H | High Z | Deselect, Output Disabled | Active (I_{CC}) |

Ordering Information

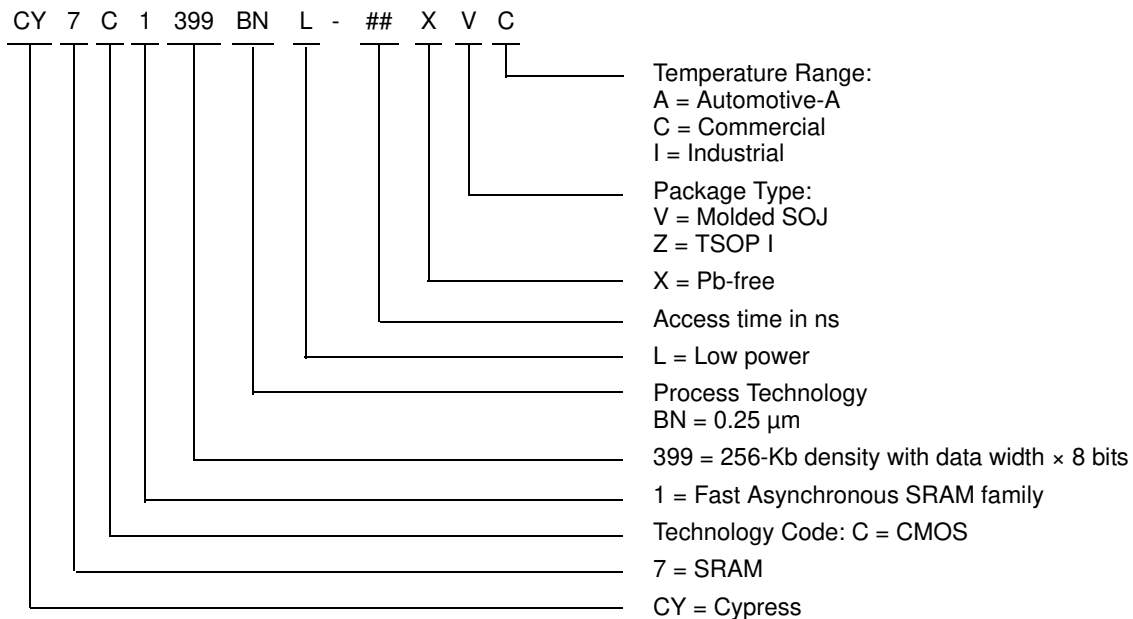
Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available.

For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at <http://www.cypress.com/products> or contact your local sales representative.

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at <http://www.cypress.com/go/datasheet/offices>.

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|-------------------|-----------------|------------------------------|-----------------|
| 12 | CY7C1399BN-12VXC | 51-85031 | 28-Lead Molded SOJ (Pb-free) | Commercial |
| | CY7C1399BN-12ZXC | 51-85071 | 28-Lead TSOP I (Pb-free) | |
| | CY7C1399BNL-12ZXC | | 28-Lead TSOP I (Pb-free) | |
| | CY7C1399BN-12VXI | 51-85031 | 28-Lead Molded SOJ (Pb-free) | Industrial |
| 15 | CY7C1399BN-15ZXI | 51-85071 | 28-Lead TSOP I (Pb-free) | Industrial |
| | CY7C1399BN-15VXA | 51-85031 | 28-Lead Molded SOJ (Pb-free) | Automotive-A |

Please contact local sales representative regarding availability of these parts.

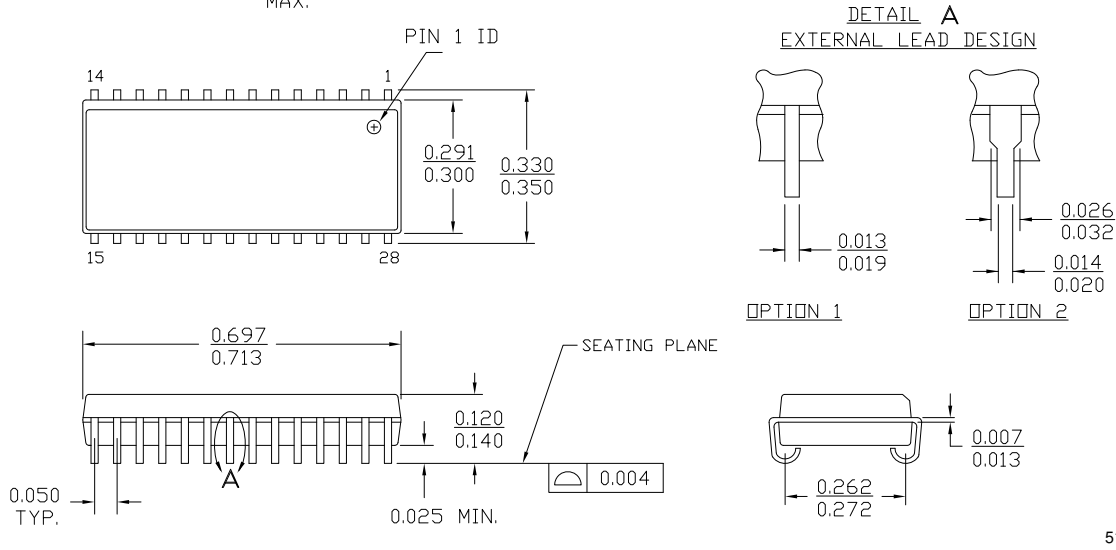
Ordering Code Definitions


Package Diagrams

28-Lead (300-Mil) Molded SOJ (51-85031)

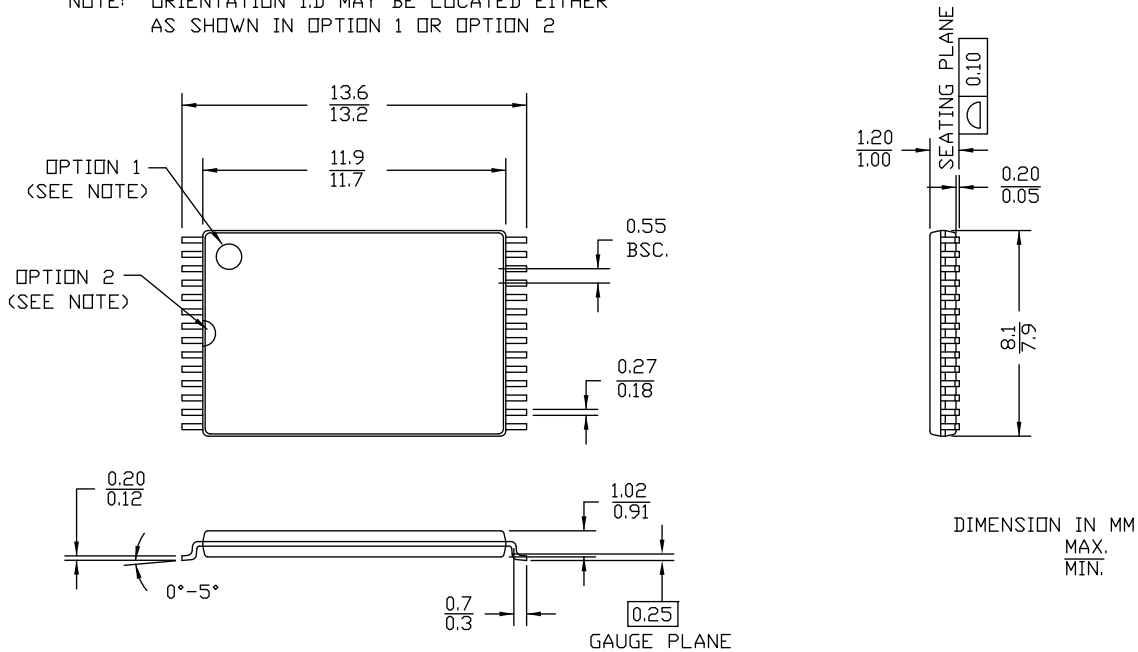
NOTE :

1. JEDEC STD REF MO088
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN INCHES MIN.
MAX.



28-Lead TSOP 1 (8x13.4 mm) (51-85071)

NOTE: ORIENTATION I.D MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



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Document History Page

| Document Title: CY7C1399BN 256K (32K x 8) Static RAM Document Number: 001-06490 | | | | |
|--|---------|------------|-----------------|---|
| REV. | ECN NO. | ISSUE DATE | ORIG. OF CHANGE | DESCRIPTION OF CHANGE |
| ** | 423877 | See ECN | NXR | New Data Sheet |
| *A | 498575 | See ECN | NXR | Added Automotive-A range Removed I _{OS} parameter from DC Electrical Characteristics table Updated Ordering Information table. |
| *B | 2896382 | 03/19/2010 | AJU | Removed obsolete part numbers from Ordering Information table and updated package diagrams. |
| *C | 3053362 | 10/08/2010 | PRAS | Removed pruned part numbers CY7C1399BNL-15VXC and CY7C1399BNL-15VXCT. Added Ordering Code Definitions. |