

Features

- ESD protection for one line with bi-direction
- Provide transient protection for the protected line to
IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air) / $\pm 12\text{kV}$ (contact)
IEC 61000-4-5 (Lightning) 7A (8/20 μs)
- **Ultra-low capacitance: 0.18pF typical**
- For low operating voltage applications: **2.0V and below**
- **0201 small DFN package** saves board space
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green part**

Applications

- 2.5G/5G/10GbE
- Thunderbolt interface
- USB3.1 and USB3.0 interfaces
- USB Type-C interface
- DisplayPort interface
- Hand held portable applications

Description

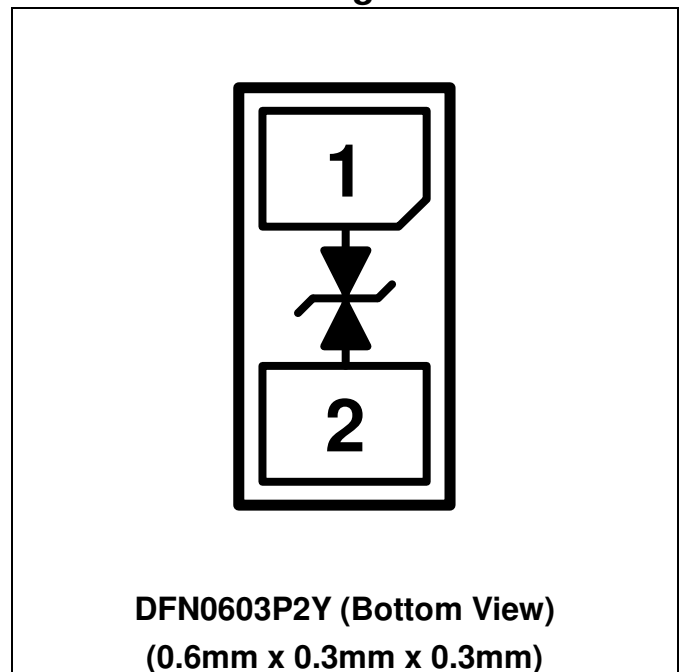
AZ5B0S-01F is a design which includes a bi-directional ESD rated clamping cell to protect high-speed data interfaces in an electronic system. The AZ5B0S-01F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD), Lightning, and Cable Discharge Event (CDE).

AZ5B0S-01F is a unique design which includes proprietary clamping cell with ultra-low capacitance in a small package. During transient conditions, the proprietary clamping cell prevents over-voltage on the control lines, or data lines, protecting any downstream components.

AZ5B0S-01F is bi-directional and may be used on lines where the signal swings above and below ground.

AZ5B0S-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Circuit Diagram / Pin Configuration





Specifications

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$, unless otherwise specified)			
Parameter	Symbol	Rating	Unit
Peak Pulse Current ($t_p=8/20\mu\text{s}$)	I_{pp}	7	A
Operating Voltage	V_{DC}	± 2.2	V
ESD per IEC 61000-4-2 (Air)	V_{ESD-1}	± 15	kV
ESD per IEC 61000-4-2 (Contact)	V_{ESD-2}	± 12	
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	$^\circ\text{C}$
Operating Temperature	T_{OP}	-55 to +125	$^\circ\text{C}$
Storage Temperature	T_{STO}	-55 to +150	$^\circ\text{C}$

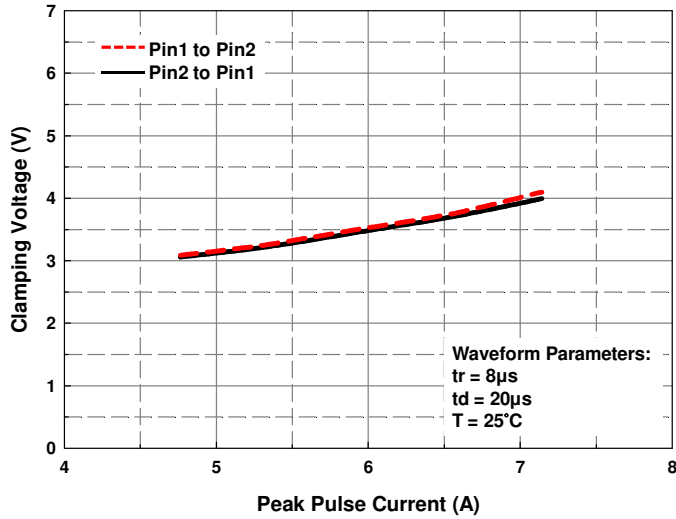
Electrical Characteristics						
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}	$T=25^\circ\text{C}$.	-2		2	V
Reverse Leakage Current	I_{Leak}	$V_{RWM} = \pm 2\text{V}$, $T=25^\circ\text{C}$.			500	nA
Reverse Breakdown Voltage	V_{BV}	$I_{BV} = 1\text{mA}$, $T=25^\circ\text{C}$.	5.5		10	V
Surge Clamping Voltage	$V_{CL-surge}$	$I_{PP} = 7\text{A}$, $t_p = 8/20\mu\text{s}$, $T=25^\circ\text{C}$.		4	5.5	V
ESD Clamping Voltage (Note 1)	V_{CL-ESD}	IEC 61000-4-2 +8kV ($I_{TLP} = 16\text{A}$), contact mode, $T=25^\circ\text{C}$.		5.5		V
ESD Dynamic Turn on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+8kV, contact mode, $T=25^\circ\text{C}$.		0.18		Ω
Channel Input Capacitance	C_{IN}	$V_R = 2\text{V}$, $f = 1\text{MHz}$, $T=25^\circ\text{C}$.		0.18		pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

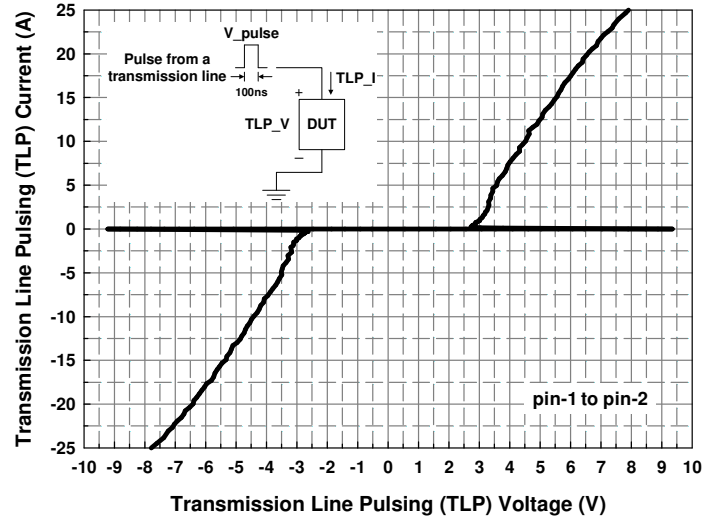
TLP conditions: $Z_0 = 50\Omega$, $t_p = 100\text{ns}$, $t_r = 1\text{ns}$.

Typical Characteristics

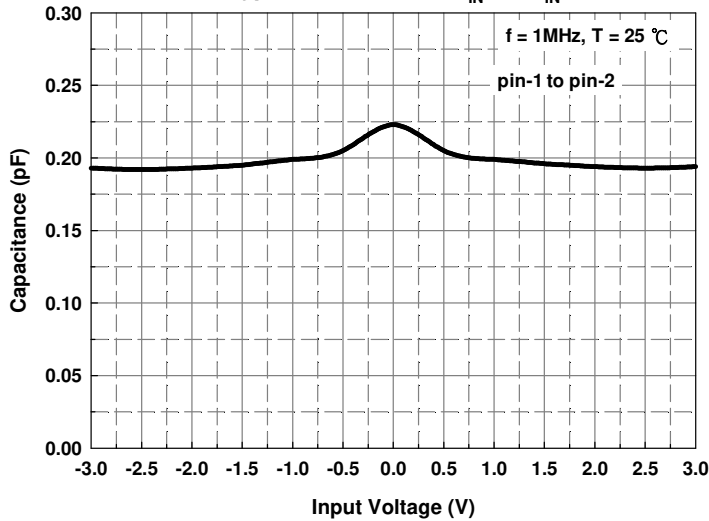
Reverse Clamping Voltage vs. Peak Pulse Current



Transmission Line Pulsing (TLP) Measurement



Typical Variation of C_{IN} vs. V_{IN}



Application Information

The AZ5B0S-01F is designed to protect one line against system ESD pulse by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ5B0S-01F is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ5B0S-01F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5B0S-01F.
- Place the AZ5B0S-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

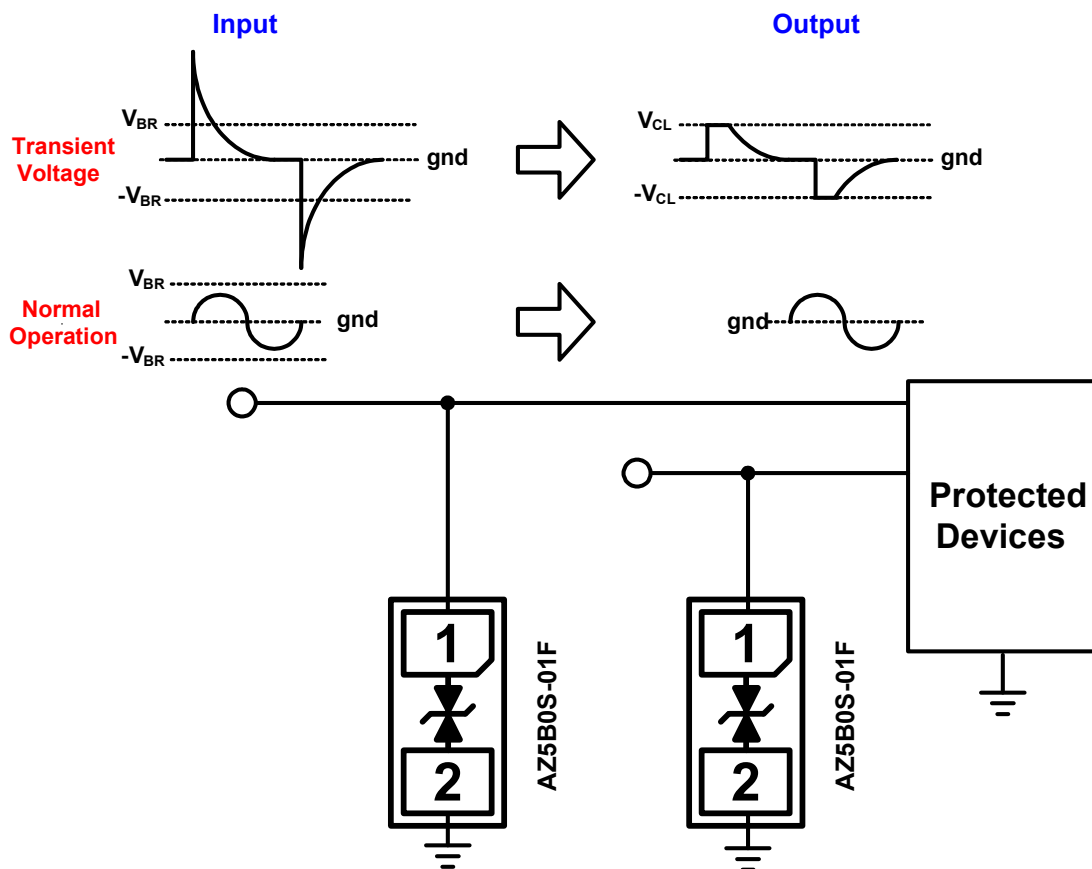
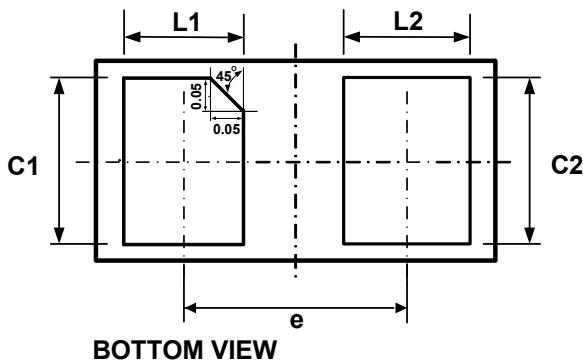
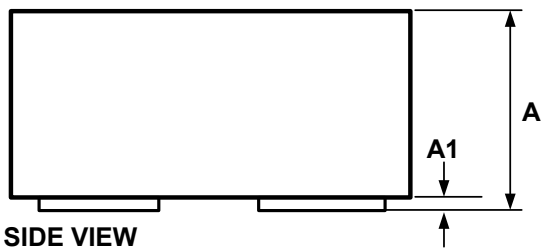
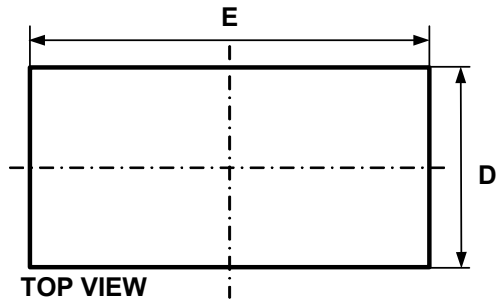


Fig. 1



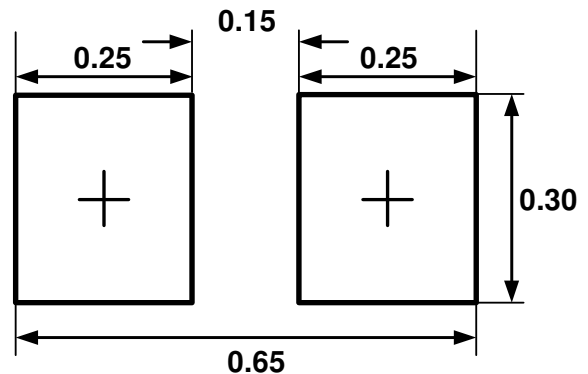
Mechanical Details

DFN0603P2Y PACKAGE DIAGRAMS



Symbol	Millimeters		
	Min.	Nom.	Max.
E	0.55	0.60	0.65
D	0.25	0.30	0.35
A	0.28	0.30	0.32
A1	0.00	0.02	0.05
L1	0.13	0.18	0.23
L2	0.14	0.19	0.24
C1/C2	0.20	0.25	0.30
e	0.35 BSC		

Land Layout

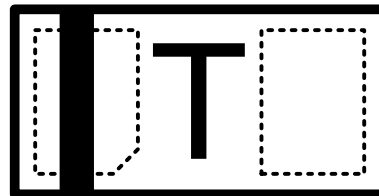


(Unit: mm)

Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

Marking Code



T = Device Code

Part Number	Marking Code
AZ5B0S-01F.R7G (Green Part)	T

Note. Green means Pb-free, RoHS, and Halogen free compliant.



Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ5B0S-01F.R7G	Green	T/R	7 inch	12,000/reel	4 reels= 48,000/box	6 boxes =288,000/carton

Revision History

Revision	Modification Description
Revision 2020/03/02	Formal Release.