DEMO CIRCUIT 892
QUICK START GUIDE

LT6556 and LT6555 in QFN
Triple High-Speed 2:1 Video MUX

DESCRIPTION

Demonstration circuit 892 is a Triple High-Speed 2:1 Video MUX featuring the LT6556 and LT6555 in QFN packaging. The –A version of the board includes the gain-of-2 LT6555 and the –B version features the unity-gain LT6556. This Demo Circuit provides dc-coupled 75Ω I/O and is intended to operate from split power supplies. The ultra high bandwidth and channel-switching rate make the LT6555 and LT6556 ideal for HDTV and UXGA video equipment.

The Performance Summary table below indicates the operating characteristics of this demonstration circuit.

Design files for this circuit board are available. Call the LTC factory.

PERFORMANCE SUMMARY

Specification s are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} V_{EE}	Supply Voltage(s)	Recommended Split supply	±3.3	±5.0	±5.5	V
		Single supply operation (usable range, limitations apply)	4.5		12.6	V
Z_{IN}	Input Impedance, IN1A, IN2A, IN3A, IN1B, IN2B, IN3B	DC-coupled		75		Ω
Z_{OUT}	Output Impedance, OUT1, OUT2, OUT3	DC-coupled		75		Ω
A	Gain (-A version, LT6555)	Outputs terminated into 75Ω		0.0		dB
		Outputs terminated into High impedance		6.0		dB
A	Gain (-B version, LT6556)	Outputs terminated into 75Ω		-6.0		dB
		Outputs terminated into High impedance		0.0		dB
	Crosstalk	Worst-case All Hostile, 10MHz		-75		dB
		Worst-case All Hostile, 100MHz		-50		dB
V_{IN}	Input Signal Voltage Range (note: feedback resistor connections tied to ground on printed circuit)	±3.3V Split Supply, VREF = 0.0V	±0.7 (-A) ±1.5 (-B)			V V
		±5.0V Split Supply, VREF = 0.0V VREF optimized (3V window)	±1.5 (-A) ±4.0 (-B)			V V
		+9.0V Single Supply, VREF = 2.2V VREF optimized (3V window)	1.0 (-A) 1.0 (-B)		3.5 8.0	V V
V_{EN}, V_{SEL}	Control Input Voltage	Logic Low Voltage (Amplifiers ON, Inputs A active), DGND = 0V	-0.3		1.0	V
		Logic High Voltage (Amplifiers OFF, Inputs B active), DGND = 0V	1.8 (EN) 1.8 (SEL)		5.5 8	V V
t_{SEL}	Select Response Time			8		ns
t_{EN}	Enable/Disable Response Time			50/500		ns
I_{CC}, I_{EE}	Supply Current	±5.0V supply, No signal		27		mA

7. For video-signal evaluation, connect a component-video signal source to the A inputs and a monitor and/or video analyzer to the outputs, using equal-length cabling amongst the three video channels. Figure 2 shows a typical pulse response.
8. To evaluate the shutdown mode, disconnect or relocate the JP1 jumper to the EXT position (with no connections made at EN (J1 or E1), or if present, a logic high provided).
9. To evaluate the input selection feature, place the JP4 jumper in either the A or B position to activate the appropriate input. If JP4 is in the B position, a select command signal may be furnished to SEL A/B (J8 or E4) from an external source. Logic low selects input-group A and Logic high selects input-group B.

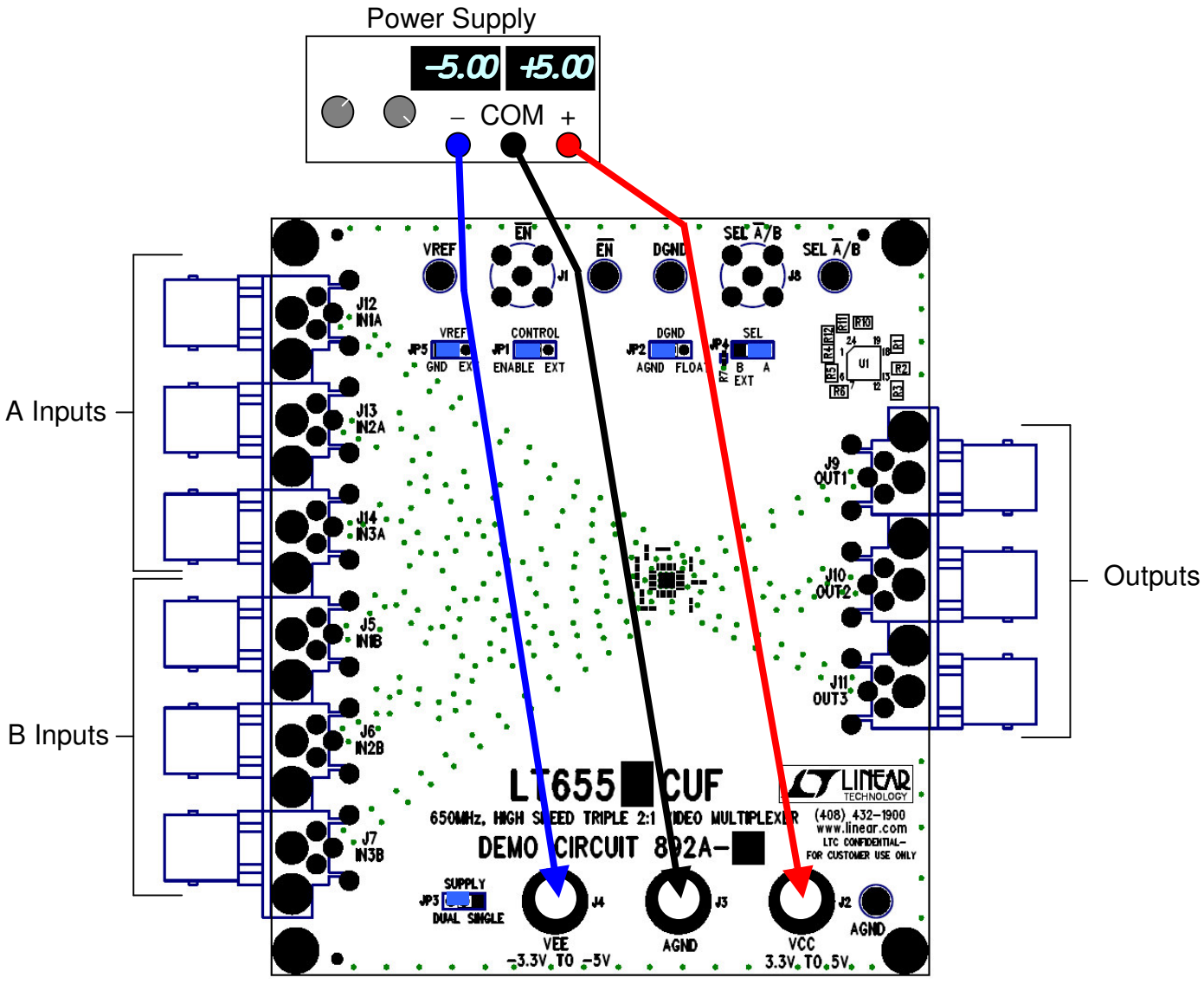

Figure 1. Recommended Demo Circuit Setup

OPERATING PRINCIPLES

DC892 provides three identical channels of 2-way selectable wideband signal amplification suitable for driving HDTV or high-resolution RGB video display cables. Each amplifier section of the LT6555 or LT6556 includes a dual-input selection circuit (MUX) and an internally fixed gain. The LT6555 provides a gain of two for driving terminated video cables and the LT6556 has unity gain for use with hi-impedance loads. Series back-termination resistors are provided at the outputs, so the overall result is unity gain transmission of a selected video signal to a 75Ω load for the LT6555 or to a hi-Z load for the LT6556 (the series termination will still prevent reflections and C-loading of the amplifiers in the LT6556 application). Each input is continually terminated to analog ground to properly load the input signal cables.

Refer to Figure 3 for the material list of the components used by DC892, and to Figure 4 for the electrical interconnection. Figure 3 shows the -A version, but the only difference in the –B is the U1 part number being LT6556CUF.

To minimize ingress of external digital ground noise, the DGND logic reference input is decoupled from analog ground within the LT6555 or LT6556. DC892 includes a jumper, JP2, which allows the DGND to be strapped to the local analog ground (AGND). This is used, for example, when the logic source is floating or none is used during the evaluation. DGND may be left uncommitted with JP2 in the FLOAT position.

Another jumper, JP1, allows the LT6555 or LT6556 to be forced to an ENABLE condition. If JP1 is left in the EXTernal position, then enabling is accomplished by pulling down the EN connection to a level near that of DGND via connection at E1 or J1. A pull-up resistor internal to the LT6555 or LT6556 will provide a default shutdown mode of operation if the control input is left open-circuit. NOTE: DO NOT open-circuit EN if V+ is more than 5.5V above DGND; refer to the LT6555 or LT6556 datasheets for application details in this situation.

JP3 is provided as a convenience to eliminate having to externally short V– to GND in the case of SINGLE supply operation. Leave JP3 in the DUAL position when using split supplies.

JP4 is provided to allow fixed selection of either the A or B inputs, or if in the B position, the optional introduction of an external SEL A/B control signal at J8 or E4.

JP5 provides a means of grounding the VREF input of the LT6555 or LT6556 in the GND position. An external VREF voltage can be provided via E5 with JP5 in the EXTernal position.

QUICK START PROCEDURE

Demonstration circuit 892 is easy to set up to evaluate the performance of the LT6556 and LT6555 in QFN. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

NOTE. Due to the Ultra High Frequencies (UHF) involved, RF measurement practices are required to accurately evaluate the performance of the LT6555.

1. Place jumpers in the following positions:

JP1	ENABLE
JP2	AGND
JP3	DUAL
JP4	A
JP5	GND

2. Prior to connecting the power supply, preset the output voltages to ±5V, or to the desired level, if different.
3. With power off, connect the power supplies to VCC, VEE, and GND using banana-plug cables.
4. If using a Network Analyzer, perform the THRU transmission cal with all cabling, adapters, impedance converters, etc. in place as the reference 0dB path.
5. Energize the power supply.
6. Connect the Network Analyzer (if used) to the appropriate channels to measure frequency response and crosstalk as desired.

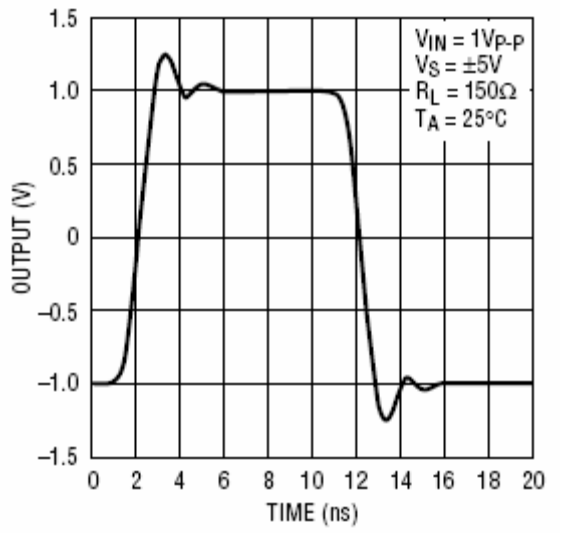

Figure 2. Typical Time-Domain Transmission Response (LT6555)

Item	*Qty*	*Reference*	*Part Description*	*Manufacture / Part #*
1	4	C1,C3,C5,C10	CAP., X7R, 4700PF, 25V, 10%, 0402	AVX, 04023C472KAT1A
2	3	C2,C7,C8	CAP., X5R, 0.22UF, 10V, 10%, 0402	TDK, C1005X5R1A224K
3	2	C4,C9	CAP., X7R, 10UF, 16V, 20%, 1206	TDK, C3216X7R1C106M
4	0	C6	CAP., 0402	OPT
5	5	E1,E2,E3,E4,E5	TP, TURRET, .094"	MILL-MAX, 2501-2
6	5	JP1,JP2,JP3,JP4,JP5	JMP, 3PIN 1 ROW .079CC	COMM-CON, 2802S-03-G2
7	5	SHUNTS FOR JP1-JP5 (1&2)	SHUNT, .079" CENTER	COMM-CON CCIJ2MM-138G
8	2	J1,J8	CONN, BNC, 5 PINS	CONNEX, 112404
9	3	J2,J3,J4	JACK, BANANA,KEY-575	KEYSTONE, 575-4
10	9	J5-J7, J9-J14	CONN, BNC, RIGHT ANGLE	CANARE, BCJ-BPLH
11	9	SCREW FOR J5-J7, J9-J14	SCREW, PC MOUNT	CANARE, M2.6
12	9	R1-R6,R10-R12	RES., CHIP, 75 OHMS, 1/16W, 5% 0402	VISHAY CRCW040275R0FKTD
15	1	R7	RES., CHIP, 20K OHMS, 1/16W, 5% 0402	VISHAY CRCW040220K0JNED
16	**0**	**R8,R9**	**RES., CHIP, 0402**	**TBD**
17	1	U1	IC., LT6555CUF, QFN24UF	LINEAR, LT6555CUF
18	4	FOR 4 MTG	STAND-OFF NYLON 0.25" (SNAP ON)	KEYSTONE, 8831
19	2	STENCILS FOR BOTH SIDES		STENCIL DC892A

Figure 3. DC892 Bill of Materials (-A version)

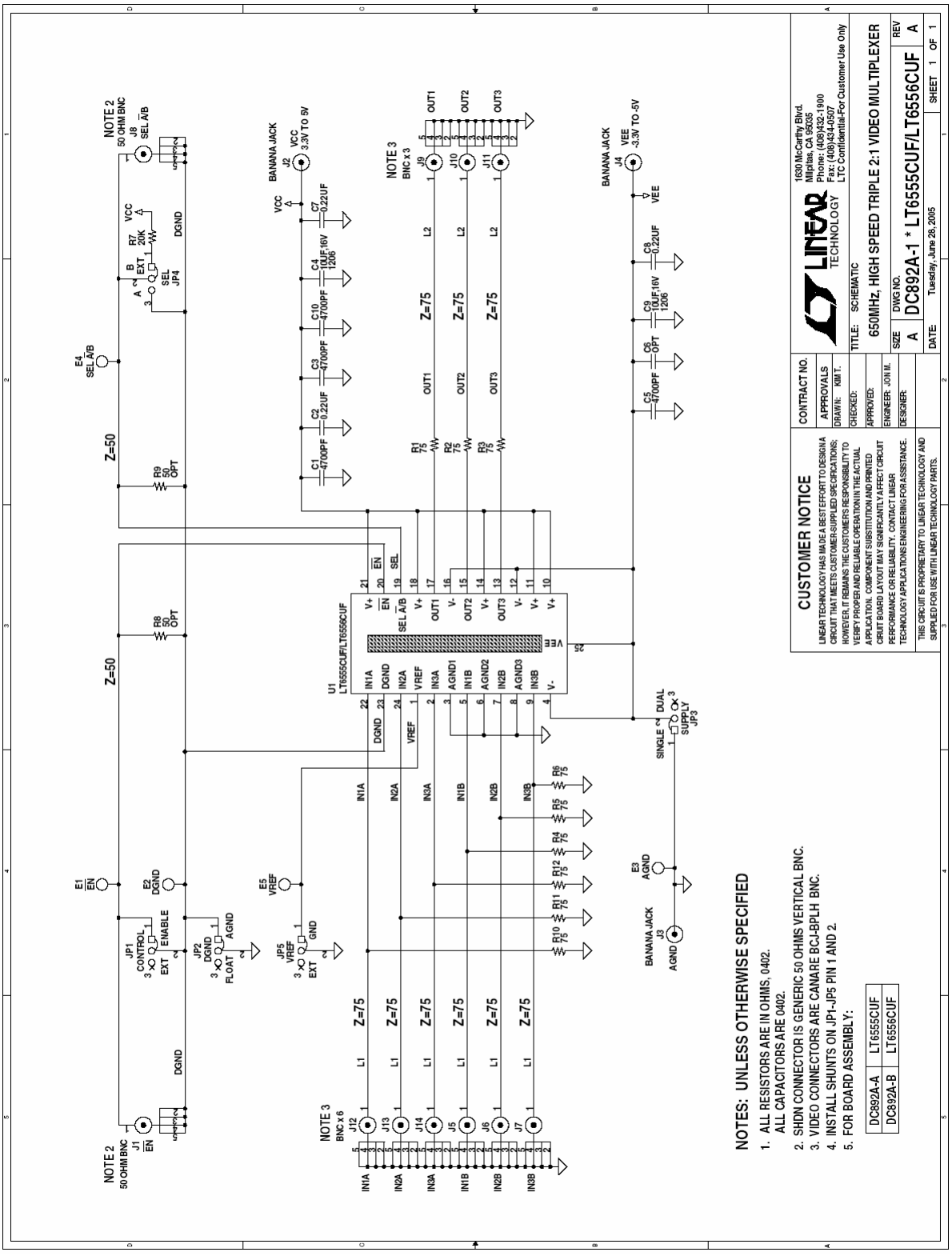

Figure 4. DC892 Electrical Schematic Diagram