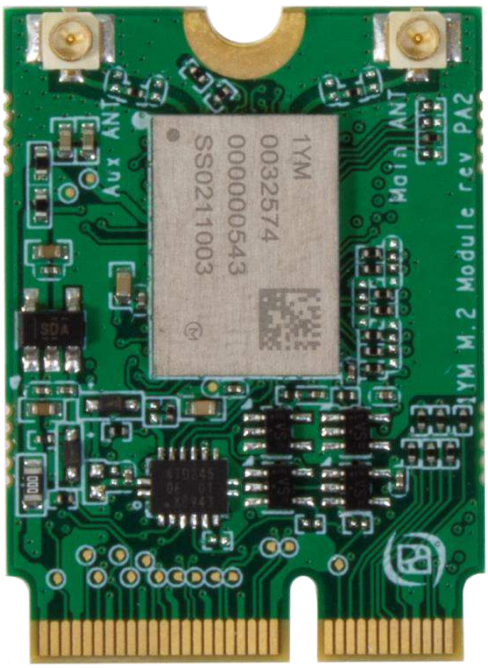
1YM M.2 Module Datasheet (EAR00370 / EAR00439 / EAR00440 / EAR00441)

- Wi-Fi 5, 802.11 a/b/g/n/ac 2x2 MU-MIMO
- Bluetooth 5.2 BR/EDR/LE
- PCIe or SDIO interface
- Chipset: NXP 88W8997



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Embedded Artists AB
Rundelsgatan 14
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Table of Contents

1 Document Information

This document applies to the following products.

Product Name	*Type Number*	*Murata Module*	*Chipset*	*Product Status*
1YM M.2 Module, rev A	EAR00370 / EAR00439 / EAR00440 / EAR00441	LBEE5XV1YM-574	88W8997	Initial Production

This table below lists the product differences. All products are not stocked. Consult Embedded Artists for availability and lead time.

Type Number	*Product Name*	*Host Interface for Wi-Fi functionality*	*Packaging*
EAR00370	1YM-PCIe M.2 Module	PCIe	Individual packing for evaluation, including 2 trace antennas.
EAR00440	1YM-PCIe M.2 Module	PCIe	Tray, no antenna included.
EAR00439	1YM-SDIO M.2 Module	SDIO	Individual packing for evaluation, including 2 trace antennas.
EAR00441	1YM-SDIO M.2 Module	SDIO	Tray, no antenna included.

1.1 Revision History

Revision	*Date*	*Description*
PA1	2020-08-28	First version.
PA2	2021-10-05	Updated document format.
PA3	2022-05-04	Updated information about used antenna for reference certification.
PA4	2023-01-16	Corrected max transmit power values. Added part number for bulk packing option.

2 Introduction

This document is a datasheet that specifies and describes the *1YM M.2 module* mainly from a hardware point of view.

The main component in the design is Murata's 1YM module (full part number: LBEE5XV1YM-574), which in turn is based on the NXP 88W8997 chipset. The 1YM module enables Wi-Fi, Bluetooth and Bluetooth Low Energy (LE) communication.

There are multiple application areas for the 1YM M.2 Module:

- Industrial and Buildings automation
- Asset management
- IoT applications
- Smart home: Voice assist device, smart printer, smart speaker, home automation gateway, and IP camera
- Retail/POS
- Healthcare and Medical devices
- Smart city

2.1 Benefits of Using an M.2 Module to get Wi-Fi/BT Connectivity

There are several benefits to use an *M.2 module* to add connectivity to an embedded design:

- Drop-in, certified solution!
- Modular and flexible approach to evaluate different Wi-Fi/BT solutions - with different trade-offs around performance, cost, power consumption, longevity, etc.
- Access to maintained software drivers (Linux) with responsive support from Murata.
- Supported by Embedded Artists' Developer's Kits for i.MX RT/6/7/8 development, including advanced debugging support on carrier boards
- One component to buy, instead of 30+
- No RF expertise is required
- Developed in close collaboration with Murata and NXP

2.2 More M.2 Related Information

For more information about the M.2 standard and Embedded Artists' adaptation, see: M.2 Primer

For more general information about the M.2 standard, see: https://en.wikipedia.org/wiki/M.2

The official M.2 specification (PCI Express M.2 Specification) is available from: www.pcisig.com

2.3 ESD Precaution and Handling

Please note that the M.2 module come without any case/box and all components are exposed for finger touches – and therefore extra attention must be paid to ESD (electrostatic discharge) precaution, for example use of static-free workstation and grounding strap. Only qualified personnel shall handle the product.

Make it a habit always to first touch the mounting hole (which is grounded) for a few seconds with both hands before touching any other parts of the boards. That way, you will have the same potential as the board and therefore minimize the risk for ESD.

In general touch as little as possible on the boards in order to minimize the risk of ESD damage. The only reasons to touch the board are when mounting/unmounting it on a carrier board.

Note that Embedded Artists does not replace modules that have been damaged by ESD.

2.4 Product Compliance

Visit Embedded Artists' website at http://www.embeddedartists.com/product_compliance for up to date information about product compliances such as CE, RoHS2, Conflict Minerals, REACH, etc.

3 Specification

This chapter lists some of the more important characteristics of the M.2 module, but it is not a full specification of performance and timing. The main component in the design is Murata's 1YM module (full part number: LBEE5XV1YM), which in turn is based around NXP's 88W8997 chipset.

For a full specification, see Murata's 1YM Module (LBEE5XV1YM-574) product page: https://www.murata.com/products/connectivitymodule/wi-fi-bluetooth/overview/lineup/type1ym and the 1YM datasheet: https://www.murata.com/products/productdata/8813652246558/type1ym.pdf

Module / Chipset	
Murata module	LBEE5XV1YM-574
Chipset	NXP 88W8997

Wi-Fi	
Standards	802.11 a/b/g/n/ac 2x2 MU-MIMO, Wi-Fi 5
Network	uAP and STA dual mode
Frequency	2.4GHz and 5 GHz band
Data rates	11, 54, 192.6, 400, 866 Mbps
Host interface	PCIe v3.0 Gen 1/Gen 2 rate (2.5/5 Gbps) (default) or SDIO 3.0, SDR104@208MHz / DDR50@50MHz

Bluetooth	
Standards	5.2 BR/EDR/LE, 3Mbps PHY
Power Class	Class 1/1.5
Host interface	4-wire UART@4MBaud
Audio interface	PCM for audio

Powering			
Supply voltage to M.2 module **Note: Do not exceed minimum or maximum voltage. Module will be permanently damaged above this limit!**	**Min** 0.0V minimum 3.0V operating and RF specification	**Typ** 3.3V	**Max** 3.6V **Note** that LBEE5XV1YM module specification has higher maximum voltage (5.5V), but other components on the M.2 module limit the maximum voltage.
Peak current	1.3A max		The power supply must be designed for this peak current, which typically happen during the startup calibration process.
Receive mode current (WLAN)	220 mA typical max		Note that current consumption varies widely between different operational modes.

Transmit mode current (WLAN)	540 mA typical max

Environmental Specification		
Operational Temperature	-30 to +85 degrees Celsius	Functionally ok, but specification is derated at temperature extremes
Storage Temperature	-30 to +85 degrees Celsius	
Relative Humidity (RH), operating and storage	10 - 90% non-condensing	

3.1 Power Up Sequence

The 3.3V supply voltage shall not rise (10 - 90%) faster than 40 microseconds and not slower than 100 milliseconds.

M.2 signal W_DISABLE1# (chipset signal PMIC_EN) must be held low for at least 100 milliseconds after supply voltage has reached specification level before pulled high.

3.2 External Sleep Clock

The sleep clock signals can be applied to a powered and unpowered M.2 module.

Clock Specification	
Frequency	32.768 kHz
Frequency accuracy	±250 ppm (including tolerance, aging, temperature, etc)
Duty cycle	20 - 80%
Clock jitter	1.5ns RMS typical
Voltage level	3.3V logic, according to M.2 standard

3.3 Mechanical Dimensions

The M.2 module is of type: 2230-S3-E according to the M.2 nomenclature. This means width 22 mm, length 30mm, top side component height 1.5 mm and key-E connector. The table below lists the different dimensions and weight.

M.2 Module Dimension	Value (±0.15 mm)	Unit
Width	22	mm
Height	30	mm
PCB thickness	0.8	mm
Maximum component height on top side	1.5	mm
Maximum component height on bottom side	0	mm
Ground hole diameter	3.5	mm
Plating around ground hole, diameter	5.5	mm
Module weight	1.5 ±0.5 gram	gram

The picture below gives dimensions for the grounded center (half) hole and the u.fl. antenna connectors.

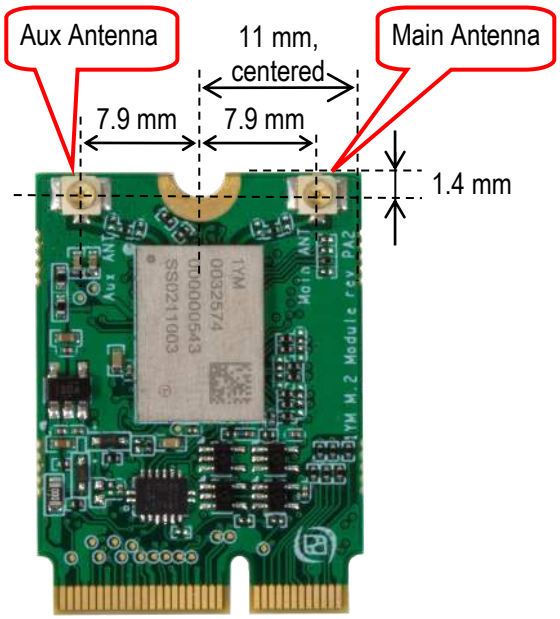

Figure 1 – M.2 Module Antenna Connector Measurements

3.4 M.2 Pinning

This section presents the pinning used for the M.2 module. It is essentially M.2 Key-E compliant with enhancements to support additional debug signals and 3.3V VDDIO override. The pin assignment for specific control and debug signals has been jointly defined by Embedded Artists, Murata, NXP and Infineon (former Cypress).

The picture below illustrates the edge pin numbering. It starts on the right edge and alternates between top and bottom side. The removed pads in the keying notch count (but are obviously non-existing).

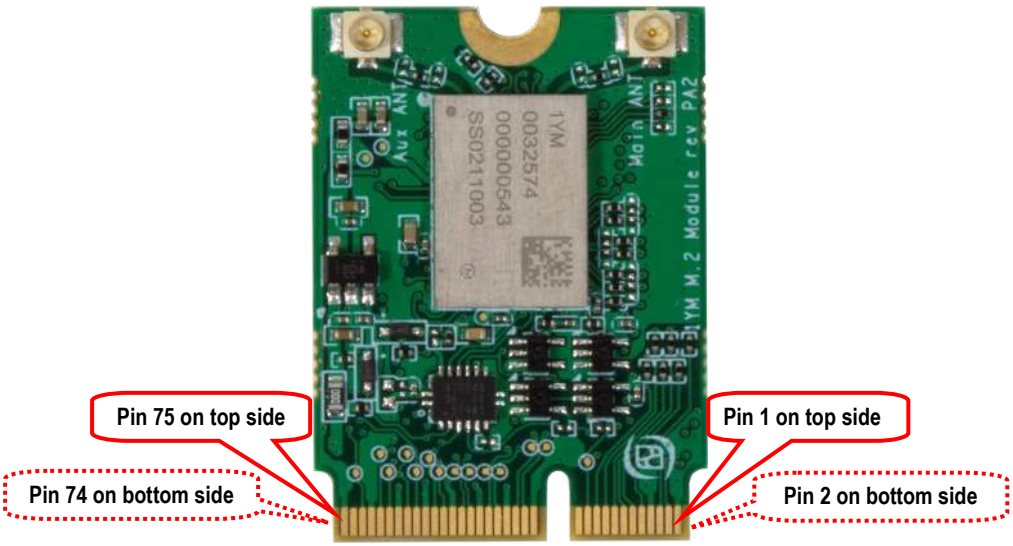

Figure 2 – M.2 Module Pin Numbering

The Wi-Fi interface uses the PCIe interface as default, but it is possible to configure the module to use the SDIO interface instead, see section 3.8 for details. The Bluetooth interface uses the UART interface for control and PCM interface for audio. The table below lists the pin usage for the 1YM M.2 modules. The column "When is signal needed" signals four different categories:

- Always: These signals shall always be connected.
- Wi-Fi PCIe: These signals shall always be connected then the PCIe interface is used for Wi-Fi
- Wi-Fi SDIO: These signals shall always be connected then the SDIO interface is used for Wi-Fi
- Bluetooth: These signals shall always be connected then the Bluetooth interface is used.
- Optional: These signals are optional to connect.

Pin #	Side of pcb	M.2 Name	Voltage Level and Signal Direction	When is signal needed	Note
1	Top	GND	GND	Always	Connect to ground
2	Bottom	3.3 V		Always	Power supply input. Connect to stable, low-noise 3.3V supply.
3	Top	USB_D+			Connected to 1YM module, signal USB_DP pin 14. Note that this interface is currently not supported in driver.
4	Bottom	3.3 V		Always	Power supply input. Connect to stable, low-noise 3.3V supply.
5	Top	USB_D-			Connected to 1YM module, signal USB_DN pin 13. Note that this interface is currently not supported in driver.

6	Bottom	LED_1#	1.8V OD output from M.2[1]		Connected to 1YM module, signal GPIO_2 pin 4.
7	Top	GND	GND	Always	Connect to ground.
8	Bottom	PCM_CLK	1.8V I/O[1]	Bluetooth audio	For Bluetooth audio interface: BT_PCM_CLK Connected to 1YM module, signal GPIO_6 pin 61.
9	Top	SDIO CLK	1.8V I/O[1]	Wi-Fi SDIO	For Wi-Fi SDIO interface: SDIO_CLK Connected to 1YM module, signal SDIO_CLK pin 20.
10	Bottom	PCM_SYNC	1.8V I/O[1]	Bluetooth audio	For Bluetooth audio interface: BT_PCM_SYNC Connected to 1YM module, signal GPIO_7 pin 81.
11	Top	SDIO CMD	1.8V I/O[1]	Wi-Fi SDIO	For Wi-Fi SDIO interface: SDIO_CMD Connected to 1YM module, signal SDIO_CMD pin 21. Note: 10-100K ohm pullup required and this interface is not enabled by default
12	Bottom	PCM_OUT	1.8V output from M.2[1]	Bluetooth audio	For Bluetooth audio interface: BT_PCM_OUT Connected to 1YM module, signal GPIO_5 pin 33.
13	Top	SDIO DATA0	1.8V I/O[1]	Wi-Fi SDIO	For Wi-Fi SDIO interface: SDIO_D0 Connected to 1YM module, signal SDIO_DATA0 pin 19. Note: 10-100K ohm pullup required and this interface is not enabled by default
14	Bottom	PCM_IN	1.8V input to M.2[1]	Bluetooth audio	For Bluetooth audio interface: BT_PCM_IN Connected to 1YM module, signal GPIO_4 pin 46.
15	Top	SDIO DATA1	1.8V I/O[1]	Wi-Fi SDIO	For Wi-Fi SDIO interface: SDIO_D1 Connected to 1YM module, signal SDIO_DATA1 pin 18. Note: 10-100K ohm pullup required and this interface is not enabled by default
16	Bottom	LED_2#	1.8V OD output from M.2[1]		Connected to 1YM module, signal GPIO_3 pin 3.
17	Top	SDIO DATA2	1.8V I/O[1]	Wi-Fi SDIO	For Wi-Fi SDIO interface: SDIO_D2 Connected to 1YM module, signal SDIO_DATA2 pin 24. Note: 10-100K ohm pullup required and this interface is not enabled by default
18	Bottom	GND		Always	Connect to ground.
19	Top	SDIO DATA3	1.8V I/O[1]	Wi-Fi SDIO	For Wi-Fi SDIO interface: SDIO_D3 Connected to 1YM module, signal SDIO_DATA3 pin 23. Note: 10-100K ohm pullup required and this interface is not enabled by default
20	Bottom	UART WAKE#	3.3V OD output from M.2	Bluetooth	For Bluetooth UART interface: BT_HOST_WAKE_L, also called BT_WAKE_OUT Connected to 1YM module, via buffer, signal GPIO_13 pin 64. Require an external 10K pull-up resistor to 3.3V.
21	Top	SDIO WAKE#	1.8V OD output from M.2[1]	Wi-Fi SDIO	For Wi-Fi SDIO interface: WL_HOST_WAKE_L, also called WL_WAKE_OUT Connected to 1YM module, via buffer, signal GPIO_19 pin 25. Note: require an external 10K pullup resistor to 1.8V.
22	Bottom	UART TXD	1.8V output from M.2[1]	Bluetooth	For Bluetooth UART interface: BT_UART_TXD Connected to 1YM module, signal GPIO_8 pin 63.
23	Top	SDIO RESET#			Not connected. The Wi-Fi interface is controlled by pin 56, W_DISABLE1#,

					which is a 3.3V logic level signal.
24	Key, non existing				
25	Key, non existing				
26	Key, non existing				
27	Key, non existing				
28	Key, non existing				
29	Key, non existing				
30	Key, non existing				
31	Key, non existing				
32	Bottom	UART_RXD	1.8V input to M.2[1]	Bluetooth	For Bluetooth UART interface: BT_UART_RXD Connected to 1YM module, signal GPIO_9 pin 62.
33	Top	GND		Always	Connect to ground.
34	Bottom	UART_RTS	1.8V output from M.2[1]	Bluetooth	For Bluetooth UART interface: BT_UART_RTS Connected to 1YM module, signal GPIO_11 pin 66.
35	Top	PERp0	PCIe input to M.2	Wi-Fi PCIe	PCIe data input (receive, positive signal) Connected to 1YM module, signal PCIE_RXP pin 39.
36	Bottom	UART_CTS	1.8V input to M.2[1]	Bluetooth	For Bluetooth UART interface: BT_UART_CTS Connected to 1YM module, signal GPIO_10 pin 65.
37	Top	PERn0	PCIe input to M.2	Wi-Fi PCIe	PCIe data input (receive, negative signal) Connected to 1YM module, signal PCIE_RXN pin 40.
38	Bottom	VENDOR DEFINED	1.8V I/O[1]	Optional	On rev PA2/A: Connected to 1YM module, signal GPIO_17 pin 5. On rev B: Not connected.
39	Top	GND		Always	Connect to ground.
40	Bottom	VENDOR DEFINED	1.8V I/O[1]	Wi-Fi SDIO (optional)	For Wi-Fi SDIO interface WL_DEV_WAKE_L, also called WL_WAKE_IN On rev PA2/A: Connected to 1YM module, signal GPIO_18 pin 73. On rev B: Connected to 1YM module, signal GPIO_15 pin 7.
41	Top	PETp0	PCIe output to M.2	Wi-Fi PCIe	PCIe data output (transmit, positive signal) Connected to 1YM module, signal PCIE_TXP pin 41.
42	Bottom	VENDOR DEFINED	1.8V input to M.2[1]	Bluetooth	For Bluetooth UART interface BT_DEV_WAKE_L, also called BT_WAKE_IN Connected to 1YM module, signal GPIO_12 pin 67.
43	Top	PETn0	PCIe output to M.2	Wi-Fi PCIe	PCIe data output (transmit, negative signal) Connected to 1YM module, signal PCIE_TXN pin 42.
44	Bottom	COEX3	1.8V I/O[1]	Optional	On rev PA2/A: Connected to 1YM module, signal GPIO_16 pin 6. On rev B: Not connected.
45	Top	GND		Always	Connect to ground.
46	Bottom	COEX_TXD	1.8V I/O[1]	Optional	On rev PA2/A: Connected to 1YM module, signal GPIO_14 pin 8. On rev B: Connected to 1YM module, signal GPIO_17 pin 5.
47	Top	REFCLKp0	PCIe clock input to M.2	Wi-Fi PCIe	PCIe clock input (receive, positive signal) Connected to 1YM module, signal PCIE_CLKP pin 43.
48	Bottom	COEX_RXD	1.8V I/O[1]	Optional	On rev PA2/A: Connected to 1YM module, signal GPIO_15 pin

					7. On rev B: Connected to 1YM module, signal GPIO_16 pin 6.
49	Top	REFCLKn0	PCIe clock input to M.2	Wi-Fi PCIe	PCIe clock input (receive, negative signal) Connected to 1YM module, signal PCIE_CLKN pin 44.
50	Bottom	SUSCLK	3.3V input to M.2	Always	External sleep clock input (32.768kHz) Connected to 1YM module, via a voltage translator, signal SLP_CLK pin 56.
51	Top	GND		Always	Connect to ground.
52	Bottom	PERST0#	3.3V input to M.2	Wi-Fi PCIe	PCIe PERST# signal, used to initialize the M.2 functions once power sources stabilize. Connected to 1YM module, via voltage translator, signal GPIO_21 pin 31.
53	Top	CLKREQ0#	3.3V OD output from M.2	Wi-Fi PCIe	PCIe clock request (low level request reference clock) Connected to 1YM module, signal PCIE_CLKREQ_N pin 82. **Note**: Requires external 10Kohm pull-up
54	Bottom	W_DISABLE2#			Not connected
55	Top	PEWAKE0#	3.3V OD output from M.2	Wi-Fi PCIe	PCIe PERST# signal, used to implement host wakeup functionality Connected to 1YM module, signal PCIE_WAKEUP_N pin 32. **Note**: Requires external 10Kohm pull-up
56	Bottom	W_DISABLE1#	3.3V input to M.2	Always	Connected to 1YM module, via buffer, signal PMIC_EN, pin 30. PMIC_EN High = Module enabled/internally powered, PMIC_EN Low = Module disabled/powered down This input has an on-board 100K ohm pull-up resistor.
57	Top	GND		Always	Connect to ground.
58	Bottom	I2C_SDA			Not connected.
59	Top	Reserved			Not connected.
60	Bottom	I2C_CLK			Not connected.
61	Top	Reserved			Not connected.
62	Bottom	ALERT#	1.8V I/O[1]	Optional	On rev PA2/A boards: Connected to 1YM module, signal GPIO_23 pin 79. On rev B boards: Not connected.
63	Top	GND		Always	Connect to ground.
64	Bottom	RESERVED		Optional	Optional supply voltage input for control and data signal voltage level. Apply a stable, low-noise, 3.3V 100mA supply to set 3.3V voltage level on all control signals (that normally are 1.8V).
65	Top	Reserved			Not connected.
66	Bottom	UIM_SWP			On rev PA2/A boards: Connected in parallel with M.2 pin 44. On rev B boards: Not connected.
67	Top	Reserved			Not connected.
68	Bottom	UIM_POWER_SNK	1.8V I/O[1]	Optional	On rev PA2/A boards: Connected to 1YM module, signal GPIO_1 pin 78. On rev B boards: Not connected.
69	Top	GND		Always	Connect to ground.
70	Bottom	UIM_POWER_SRC/GPIO_1	1.8V I/O[1]	Optional	On rev PA2/A boards: Connected to 1YM module, signal GPIO_0 pin 47. On rev B boards: Not connected.

71	Top	Reserved		Not connected.
72	Bottom	3.3 V	Always	Power supply input. Connect to stable, low-noise 3.3V supply.
73	Top	Reserved		Not connected.
74	Bottom	3.3 V	Always	Power supply input. Connect to stable, low-noise 3.3V supply.
75	Top	GND	Always	Connect to ground.

[1] Note: If applying 3.3V to pin 64, the signaling voltage is changed to 3.3V

3.5 VDDIO Override Feature

The M.2 standard specifies 1.8V logic level on several of the data and control signals. It is possible to override the voltage level for the 1.8V signals via pin 64. Apply a 3.3V / 100 mA supply to pin 64 in order to get 3.3V voltage level on all data and control signals.

Note: Changing VDDIO does not make sense when the Wi-Fi PCIe interface is used since the voltage levels of the PCIe interface are fixed and the PCIe related control signals are already defined for 3.3V operation (by the M.2 specification). The Bluetooth interface signals will however change from 1.8V to 3.3V logic levels.

Note: If SDIO is uses for the Wi-Fi interface, the SDIO control signals will have 3.3V signaling level. Also note that this limits the SDIO clock to 50 MHz, thereby limiting throughput. Running at 1.8V VIO will support up to 200 MHz SDIO clock (on rev A boards) which is ultimately needed for maximum 802.11ac throughput.

Note: On rev A boards, it is not enough to just apply 3.3V to pin 64. A small rework on the board is also needed. This rework is not needed on rev PA2 and rev B boards.

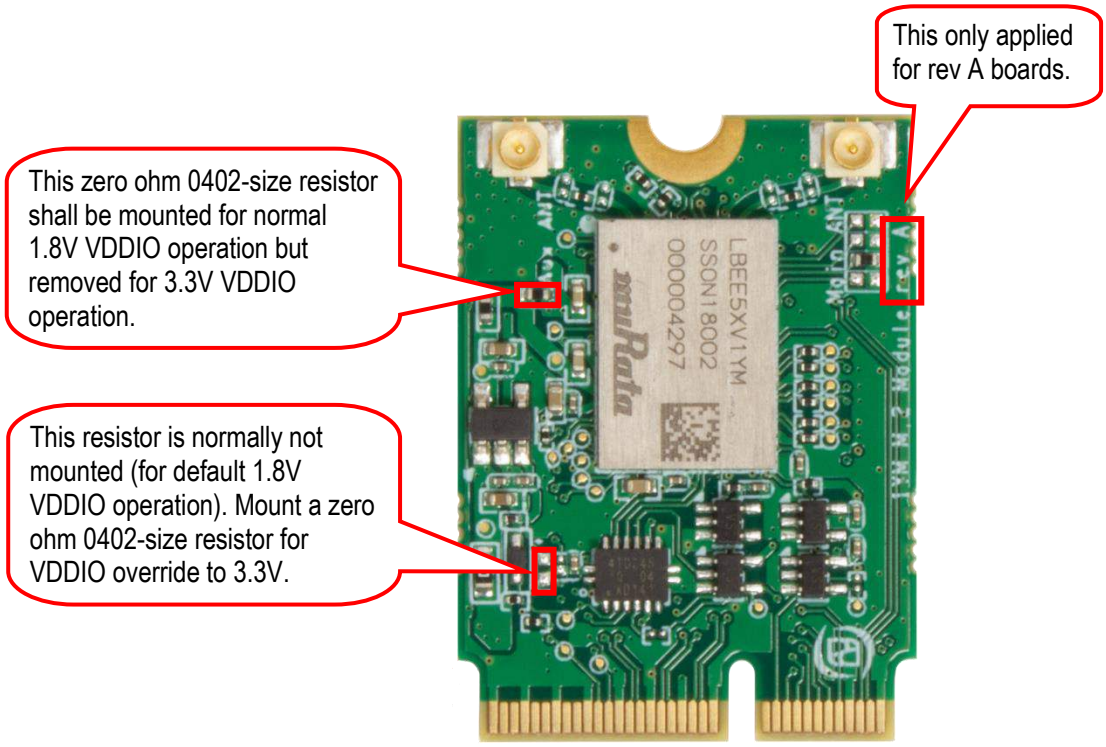

Figure 3 – Rework for 3.3V VDDIO Operation on rev A Boards

3.6 SDIO Interface

The SDIO interface conforms to the SDIO v3.0 specification, including the UHS-I modes, and is backward compatible with SDIO v2.0.

SDIO bus speed modes	Max SDIO clock frequency	Max bus speed	Signaling voltage according to M.2 specification	Supported in 3.3V VDDIO Override Mode
DS (Default speed)	25 MHz	12.5 MByte/s	1.8 V	Yes
HS (High speed)	50 MHz	25 MByte/s	1.8 V	Yes
SDR12	25 MHz	12.5 MByte/s	1.8 V	No
SDR25	50 MHz	25 MByte/s	1.8 V	No
SDR50	100 MHz	50 MByte/s	1.8 V	No
SDR104	208 MHz	104 MByte/s	1.8 V	No
DDR50	50 MHz	50 MByte/s	1.8 V	No

3.7 Test Points

There are some test points that can be of interest to probe for debugging purposes, as illustrated in the pictures below (note the different in board revisions).

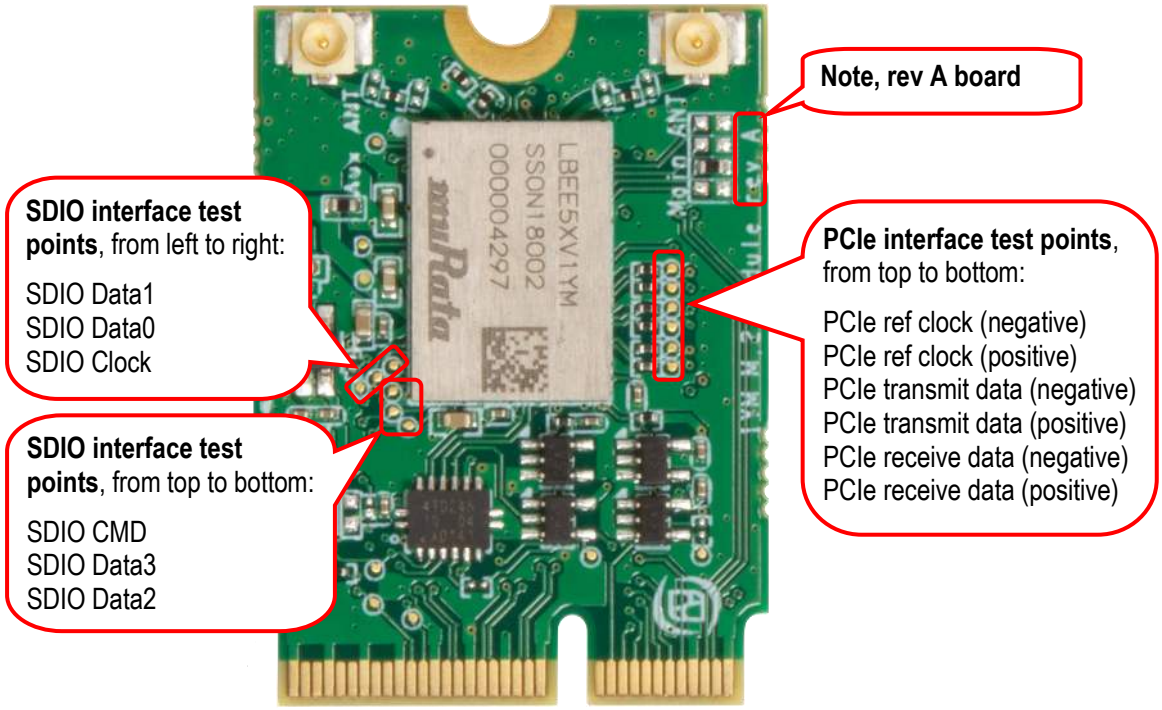

Figure 4 – 1YM M.2 Module PCIe and SDIO Test Points on rev A Boards

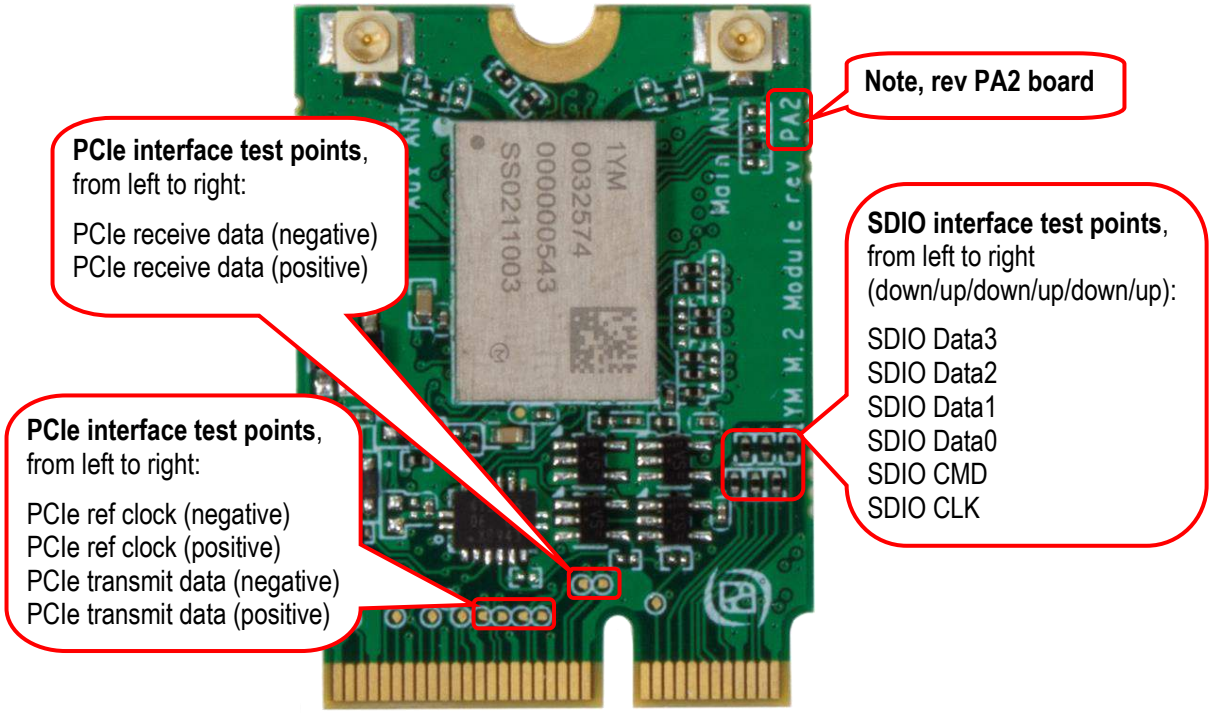

Figure 5 – 1YM M.2 Module PCIe and SDIO Test Points on rev PA2 Boards

3.8 Set SDIO Host Interface

The default interface for Wi-Fi is PCIe. It is possible to change this to the SDIO interface with a small rework, as described in the picture below.

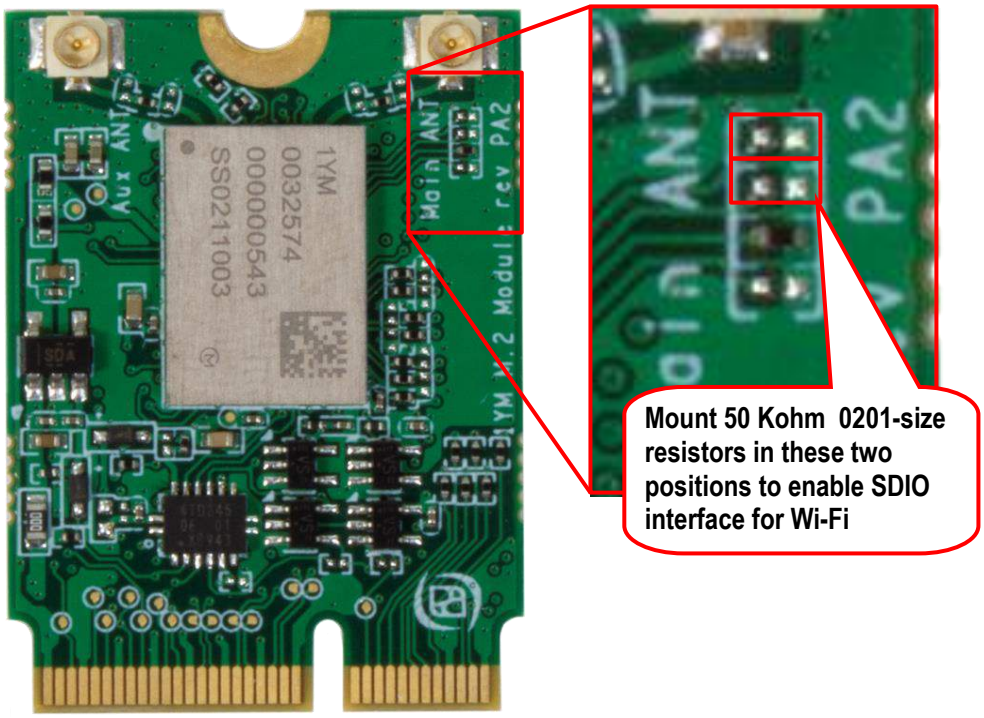

Figure 6 – 1YM M.2 Module Board Interface Configuration

Note: before deciding on using the SDIO interface, check availability of drivers for the host platform you are using

Note: To set the Wi-Fi interface to SDIO, use a rev B boards or later. On rev PA2/A boards, the SDIO interface was only experimental, and pinning was not 100% decided. With the current 1YM firmware, the SDIO interface wakeup functionality is only functional on rev B (or later) boards.

3.8.1 SDIO Clock Frequency Limit

Note: On rev PA2 boards the SDIO clock frequency must be limited to 100 MHz. On later revisions (rev A, or later) the SDIO clock frequency can be up to 200 MHz. The picture below illustrates where to locate the board revision information in the silk screen.

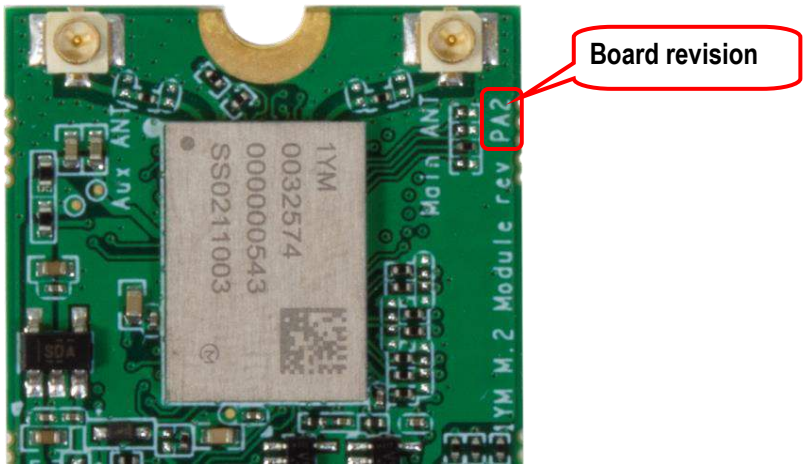

Figure 7 – 1YM M.2 Module Board Revision

3.9 Current Consumption Measurements

It is possible to measure the currents of the power supplies to the 1YM module, VBAT and VDDIO. VBAT is the 3.3V the is supplied to the M.2 interface and VDDIO is an on-board generated 1.8V. VDDIO is generated from the supplied 3.3V. If the supply voltage (3.3V) to the M.2 module is measured it will be both the VBAT and VDDIO currents that is measured. By measuring currents at the illustrated points below it is possible to measure VBAT and VDDIO. Note that VBAT is the total input current and includes the VDDIO current.

Note that zero ohm resistors are mounted by default. Select a series resistor with as low resistance as possible to keep the voltage drop to a minimum. Keep the drop below 100mV. VBAT can be slightly above 1 Amp in peak which means that maximum series resistance is 100 milliOhm for the VBAT resistor. For VDDIO the current is lower so a 1 ohm resistor can be a suitable value.

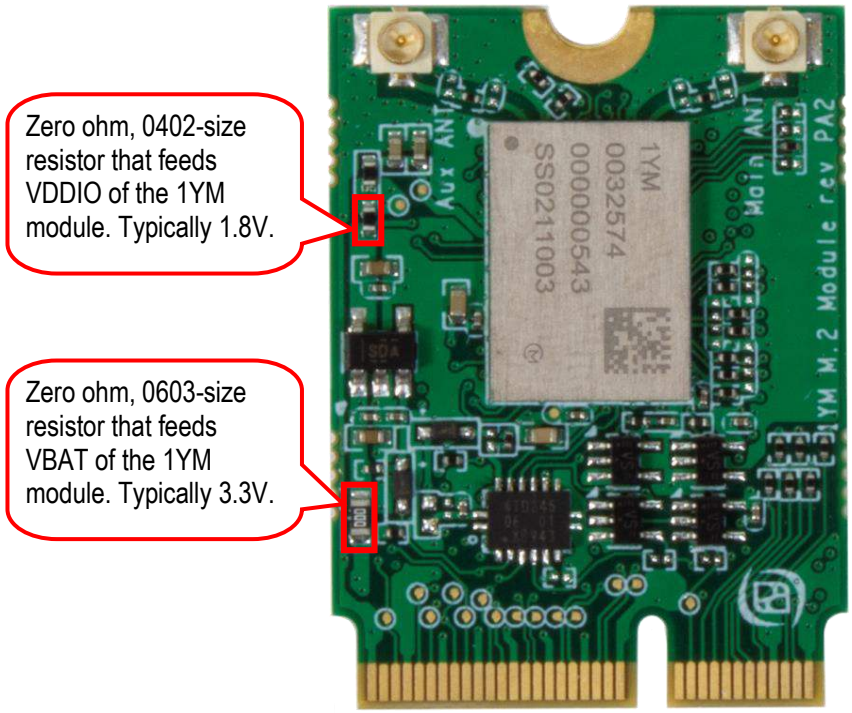

Figure 8 – Current Measurement

3.10 Differences between Revisions

To align the M.2 pinning with the coexistence interface, the M.2 pinning of four signals has been adjusted on rev B (and above), as listed in the table below. If the coexistence interface has not been used/enabled, the pinning update does not affect any operation.

M.2 pin	M.2 pin definition	Board rev PA2/A	Board rev B
21	SDIOWAKE#	GPIO19, pin 25	GPIO14, pin 8
38	VENDORDEFINED	GPIO17, pin 5	Not connected
40	VENDORDEFINED	GPIO18, pin 73	GPIO15, pin 7
44	COEX3	GPIO16, pin 6	Not connected
46	COEX_TXD	GPIO14, pin 8	GPIO17, pin 5
48	COEX_RXD	GPIO15, pin 7	GPIO16, pin 6

Also, on rev B boards it is easier to change the Wi-Fi host interface configuration. Instead of soldering resistors it is possible to just place a solder bump on one location to select the SDIO interface.

Note: To set the Wi-Fi interface to SDIO, use a rev B boards or later. On rev PA2/A boards, the SDIO interface was only experimental, and pinning was not 100% decided. With the current 1YM firmware, the SDIO interface wakeup functionality is only functional on rev B (or later) boards.

4 Antenna

The module does not have any on-board antennas because the module is too small to get spatial separation of two antennas. Two external antennas must be connected (to support MIMO).

Two different antenna types have been used for the reference certification of the 1YM module.

- Molex 1461870050 is a balanced, dipole-type, high efficiency antenna. It is ground plane independent, dual band antenna that supports the 2400-2500MHz and 5150-5850MHz frequency bands. The physical size is 40.95 x 9 x 0.7mm. The antenna cable comes in 6 standard length options: 50/100/150/200/250/300mm (50mm is used for the reference certification) and the connector is MHF-I, which is a U.FL compatible connector.

- Molex 1461530050 is also a balanced, dipole-type, high efficiency antenna. It is ground plane independent, dual band antenna that supports the 2400-2500MHz and 5150-5850MHz frequency bands. The physical size is 35 x 9 x 0.1mm. The antenna cable comes in 6 standard length options: 50/100/150/200/250/300mm (50mm is used for the reference certification) and the connector is MHF-I, which is a U.FL compatible connector.

Figure 9 – Reference Certified Antenna

Note that it is **not** the Molex 1461870050 antenna that is included when ordering the evaluation bundle of the 1YM M.2 board (bulk/tray orders of 1YM M.2 do not include antennas). Instead, it is the Molex 1461870100 antenna that is included. This antenna has 100mm cable. Murata permits using this antenna (Molex 1461870100) with a *Class I Permissive Change*.

Also note that it is not allowed to mix the two reference certified antennas. Both antennas must be of the same time in any given installation.

4.1 Antenna Connector

The M.2 standard specifies a 1.5 mm outer ring diameter male connector, which is compatible with the Murata MSC and IPEX MHF4 connector specifications. This connector is not used since our M.2 modules also targets industrial users, where the Hirose U.FL. connector standard is more commonly used. U.FL. is compatible with the IPEX MHF1 connector specification.

5 Software and Support

This chapter contains information about software and support.

5.1 Software Driver

The NXP 88W8997 chipset do not contain any persistent software. A firmware image must be downloaded by the host at start-up. This is the responsibility of the operating system driver.

There are three different cases, depending on which host processor is used:

1. **Embedded Artists' Computer-on-Modules, (u)COM, as host processor**
   Embedded Artists' Linux BSPs and SDKs for the different (u)COM board contains all drivers available and pre-configured. Everything has been tested and works out-of-the-box on the different iMX Developer's Kits.

iMX Developer's Kit	1YM M.2 (PCIe) support	1YM M.2 (SDIO) support
iMX8M Mini uCOM	Yes, from Linux BSP v5.4.47	Yes, from Linux BSP v5.4.47
iMX8M Nano uCOM	No	Yes, from Linux BSP v5.4.47
iMX8M COM	Yes, from Linux BSP v5.4.47	Yes, from Linux BSP v5.4.47
iMX7 Dual COM	Yes, from Linux BSP v5.4.47	Yes, from Linux BSP v5.4.47
iMX7 Dual uCOM	Yes, from Linux BSP v5.4.47	Yes, from Linux BSP v5.4.47
iMX7ULP uCOM	No	No
iMX 6 Quad COM	Yes, from Linux BSP v5.4.47	Yes, from Linux BSP v5.4.47
iMX 6 DualLite COM	Yes, from Linux BSP v5.4.47	Yes, from Linux BSP v5.4.47
iMX 6 SoloX COM	Yes, from Linux BSP v5.4.47	Yes, from Linux BSP v5.4.47
iMX 6 UltraLite/ULL COM	No	Yes, from Linux BSP v5.4.47
iMX RT1176 uCOM	No	No
iMX RT1166 uCOM	No	No
iMX RT1064 uCOM	No	No
iMX RT1062 OEM	No	No

2. **Other i.MX based, for example NXP's EVKs**
   Murata has created documentation how to compile the Linux kernel for the NXP EVKs https://wireless.murata.com/products/rf-modules-1/wi-fi-bluetooth-for-nxp-i-mx.html#Linux

3. **Non-i.MX host processor**
   There is no ready-to-go driver exist. Contact Murata to check driver availability on the hardware platform used.

5.2 Support

Embedded Artists supports customers that use our M.2 module in combination with Embedded Artists' Computer-on-Modules, (u)COM, based on NXP's i.MX RT/6/7/8/9 families.

For other platforms, support is provided by Murata via their Community Support Forum:
https://community.murata.com/s/topic/0TO5F0000002TLWWA2/connectivity-modules

6 Regulatory

The Murata 1YM module is reference certified. See the LBEE5XV1YM datasheet from Murata for details.

6.1 European Union Regulatory Compliance

EUROPEAN DECLARATION OF CONFORMITY (Simplified DoC per Article 10.9 of the Radio Equipment Directive 2014/53/EU)

This apparatus, namely 1YM M.2 module (pn EAR00370, EAR00439, EAR00440, EAR00441) conforms to the Radio Equipment Directive (RED) 2014/53/EU. The full EU Declaration of Conformity for this apparatus can be found at this location: https://www.embeddedartists.com/products/1ym-m-2-module/, see document *1YM M.2 module Declaration of Conformity*.

The following information is provided per Article 10.8 of the Radio Equipment Directive 2014/53/EU:

(a) Frequency bands in which the equipment operates.

(b) The maximum RF power transmitted.

PN	RF Technology	(a) Frequency Ranges (EU)	(b) Max Transmitted Power
EAR00370 / EAR00439 / EAR00440 / EAR00441	Bluetooth BR/EDR/LE	2400 MHz – 2484 MHz	6.0 dBm
EAR00370 / EAR00439 / EAR00440 / EAR00441	Wi-Fi IEEE 802.11b/g/n	2400 MHz – 2484 MHz	19.0 dBm
EAR00370 / EAR00439 / EAR00440 / EAR00441	Wi-Fi IEEE 802.11a/n/ac	5150 MHz – 5850 MHz	16.0 dBm

The 1YM M.2 module complies with the Directive 2011/65/EU (EU RoHS 2) and its amendment Directive (EU) 2015/863 (EU RoHS 3).

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