

Features

- Low On-Resistance
 - 45mΩ @ $V_{GS} = -10V$
 - 65mΩ @ $V_{GS} = -4.5V$
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **Lead Free By Design/RoHS Compliant (Note 2)**
- **"Green" Device (Note 4)**
- **Qualified to AEC-Q101 Standards for High Reliability**

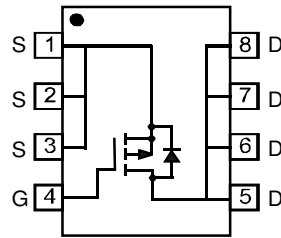
Mechanical Data

- Case: SOP-8L
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020D
- Terminals Connections: See Diagram
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208
- Marking Information: See Page 4
- Ordering Information: See Page 4
- Weight: 0.072g (approximate)



TOP VIEW

SOP-8L


 TOP VIEW
Internal Schematic

Maximum Ratings @ $T_A = 25^\circ C$ unless otherwise specified

| Characteristic | Symbol | Value | Units |
|-------------------------------|-----------|--------------|-------|
| Drain-Source Voltage | V_{DSS} | -30 | V |
| Gate-Source Voltage | V_{GSS} | ± 20 | V |
| Drain Current (Note 1) | I_D | -7.1 -6.0 | A |
| Pulsed Drain Current (Note 3) | I_{DM} | -20 | A |

Thermal Characteristics

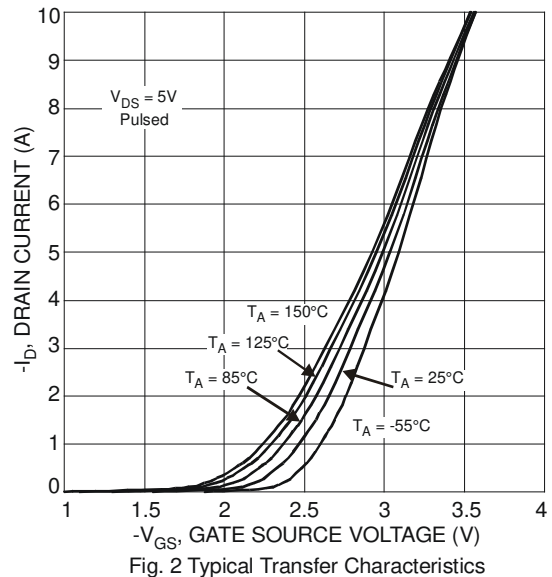
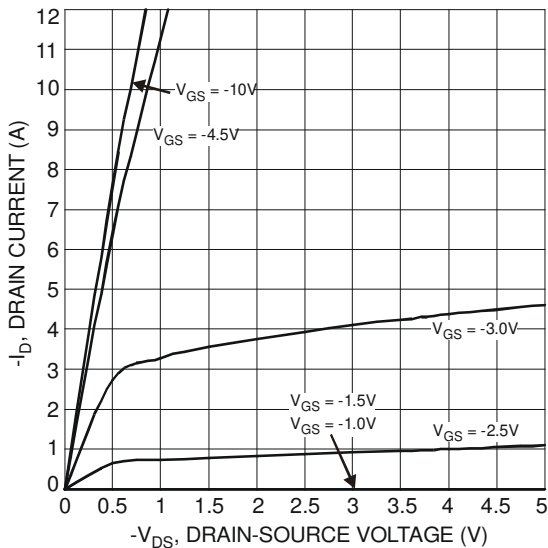
| Characteristic | Symbol | Value | Unit |
|--|-----------------|-------------|--------------|
| Total Power Dissipation (Note 1) | P_D | 2.5 | W |
| Thermal Resistance, Junction to Ambient (Note 1) | $R_{\theta JA}$ | 50 | $^\circ C/W$ |
| Operating and Storage Temperature Range | T_J, T_{STG} | -55 to +150 | $^\circ C$ |

- Notes:
1. Device mounted on 1" x 1" 2 oz. Copper pads on 2" x 2" FR-4 PCB.
 2. No purposefully added lead.
 3. Pulse width $\leq 10\mu S$, Duty Cycle $\leq 1\%$.
 4. Diodes Inc.'s "Green" policy can be found on our website at http://www.diodes.com/products/lead_free/index.php.

Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

| Characteristic | Symbol | Min | Typ | Max | Unit | Test Condition |
|-------------------------------------|--------------|------|------|------------------------|------------|--|
| OFF CHARACTERISTICS (Note 5) | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DSS} | -30 | — | — | V | $V_{GS} = 0V, I_D = -250\mu A$ |
| Zero Gate Voltage Drain Current | I_{DSS} | — | — | -1 | μA | $V_{DS} = -30V, V_{GS} = 0V$ |
| Gate-Source Leakage | I_{GSS} | — | — | ± 100 ± 800 | nA | $V_{GS} = \pm 20V, V_{DS} = 0V$ $V_{GS} = \pm 25V, V_{DS} = 0V$ |
| ON CHARACTERISTICS (Note 5) | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | -1 | 1.7 | -2.1 | V | $V_{DS} = V_{GS}, I_D = -250\mu A$ |
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | — | — | 45 65 | m Ω | $V_{GS} = -10V, I_D = -6.0A$ $V_{GS} = -4.5V, I_D = -5.0A$ |
| Forward Transconductance | g_{fs} | — | 8 | — | S | $V_{DS} = -10V, I_D = -5.3A$ |
| Diode Forward Voltage (Note 5) | V_{SD} | -0.5 | — | -1.2 | V | $V_{GS} = 0V, I_S = -1.7A$ |
| DYNAMIC CHARACTERISTICS | | | | | | |
| Input Capacitance | C_{iss} | — | 722 | — | pF | $V_{DS} = -25V, V_{GS} = 0V$ $f = 1.0MHz$ |
| Output Capacitance | C_{oss} | — | 114 | — | pF | |
| Reverse Transfer Capacitance | C_{rss} | — | 92 | — | pF | |
| Gate Resistance | R_G | — | 3.3 | — | Ω | $V_{DS} = 0V, V_{GS} = 0V$ $f = 1.0MHz$ |
| SWITCHING CHARACTERISTICS | | | | | | |
| Total Gate Charge | Q_G | — | 6.8 | — | nC | $V_{DS} = -15V, V_{GS} = -4.5V,$ $I_D = -6A$ |
| | Q_G | — | 13.7 | — | nC | |
| Gate-Source Charge | Q_{GS} | — | 1.6 | — | nC | $V_{DS} = -15V, V_{GS} = -10V,$ $I_D = -6A$ |
| Gate-Drain Charge | Q_{GD} | — | 4.18 | — | nC | |
| Turn-On Delay Time | $t_{d(on)}$ | — | 6.4 | — | ns | $V_{DS} = -15V, V_{GS} = -10V,$ $I_D = -1A, R_G = 6.0\Omega$ |
| Rise Time | t_r | — | 5.3 | — | | |
| Turn-Off Delay Time | $t_{d(off)}$ | — | 26.5 | — | | |
| Fall Time | t_f | — | 14.7 | — | | |

Notes: 5. Short duration pulse test used to minimize self-heating effect.



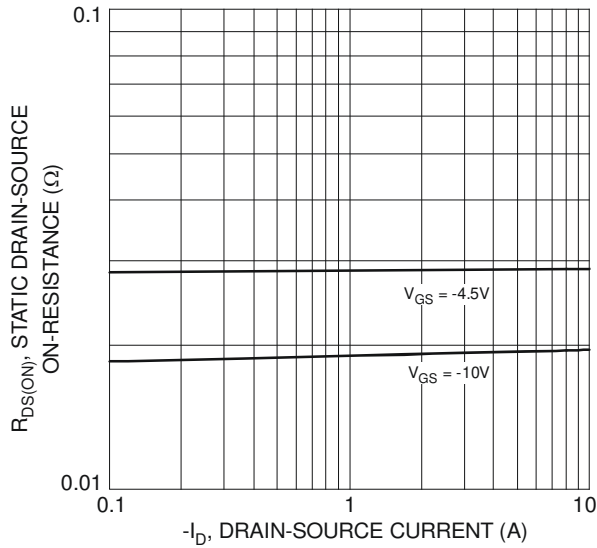


Fig. 3 On-Resistance vs. Drain Current & Gate Voltage

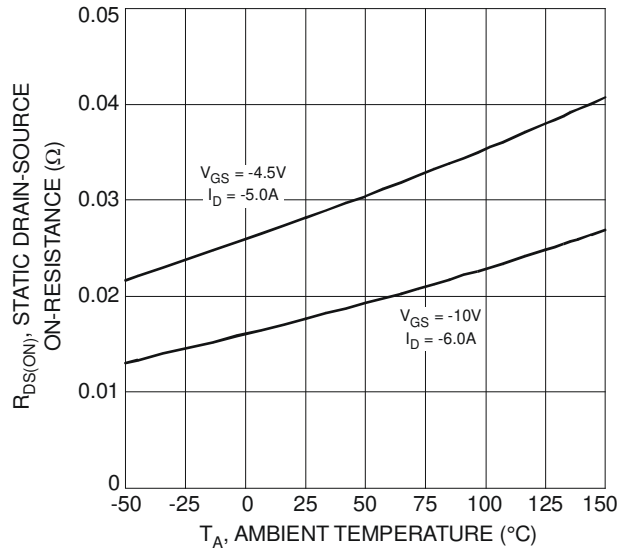


Fig. 4 Static Drain-Source On-Resistance vs. Ambient Temperature

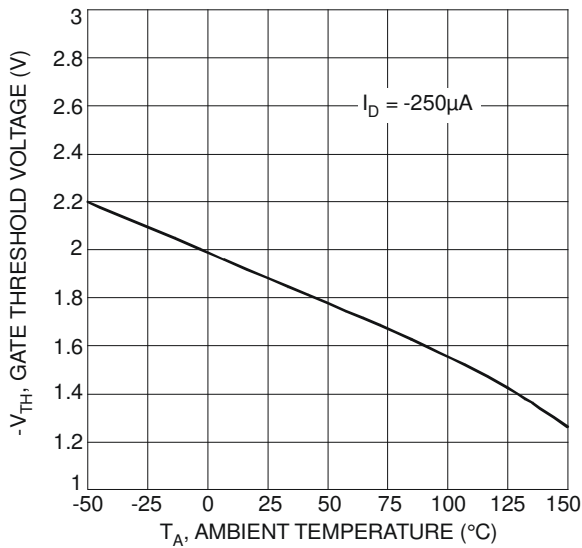


Fig. 5 Gate Threshold Variation vs. Ambient Temperature

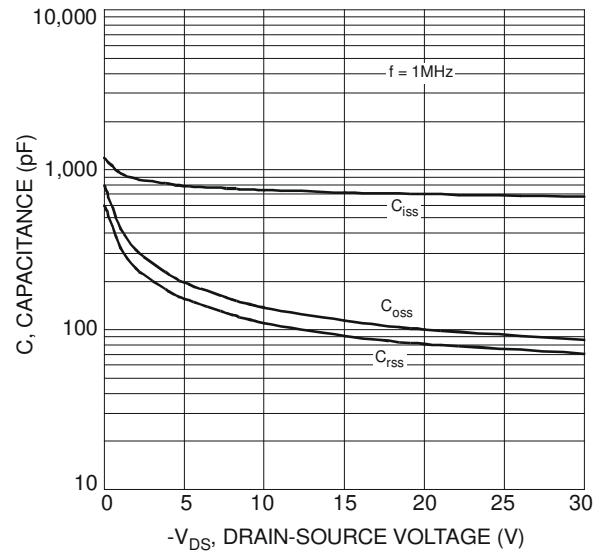


Fig. 6 Typical Total Capacitance

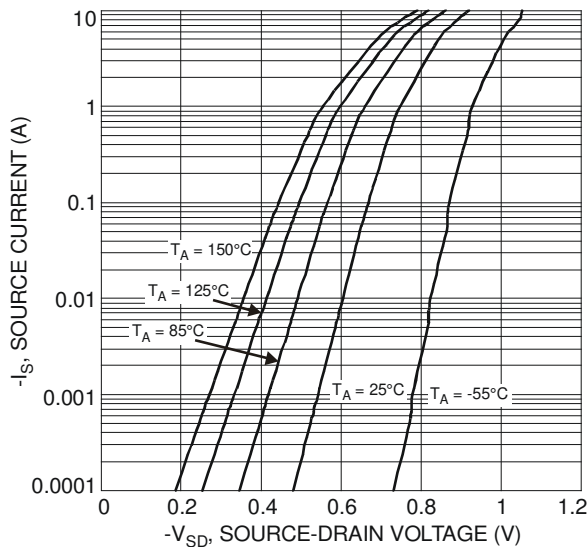


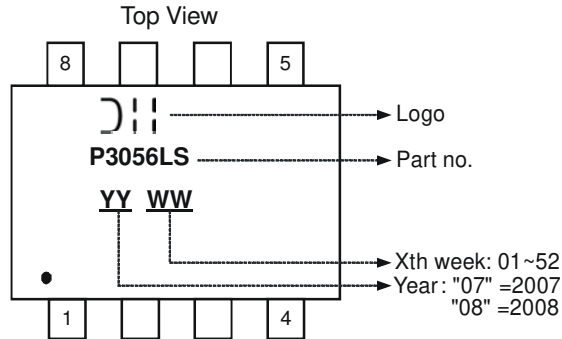
Fig. 7 Reverse Drain Current vs. Source-Drain Voltage

Ordering Information (Note 6)

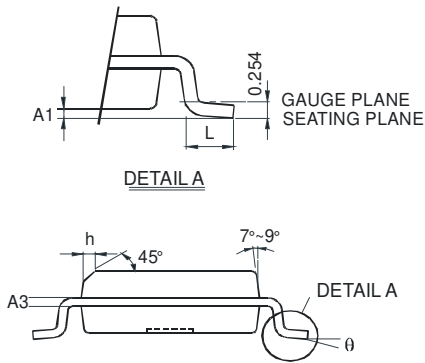
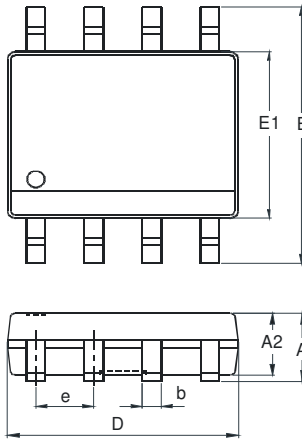
| Part Number | Case | Packaging |
|---------------|--------|------------------|
| DMP3056LSS-13 | SOP-8L | 2500/Tape & Reel |

Notes: 6. For packaging details, go to our website at <http://www.diodes.com/datasheets/ap02007.pdf>.

Marking Information

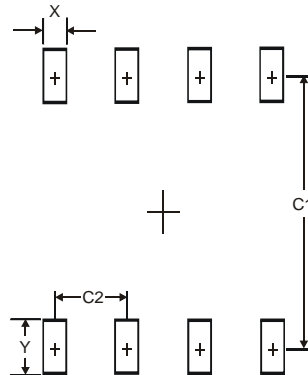


Package Outline Dimensions



| SOP-8L | | |
|----------------------|-----------|------|
| Dim | Min | Max |
| A | - | 1.75 |
| A1 | 0.08 | 0.25 |
| A2 | 1.30 | 1.50 |
| A3 | 0.20 Typ. | |
| b | 0.3 | 0.5 |
| D | 4.80 | 5.30 |
| E | 5.79 | 6.20 |
| E1 | 3.70 | 4.10 |
| e | 1.27 Typ. | |
| h | - | 0.35 |
| L | 0.38 | 1.27 |
| θ | 0° | 8° |
| All Dimensions in mm | | |

Suggested Pad Layout



| Dimensions | Value (in mm) |
|------------|---------------|
| X | 0.60 |
| Y | 1.55 |
| C1 | 5.4 |
| C2 | 1.27 |

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