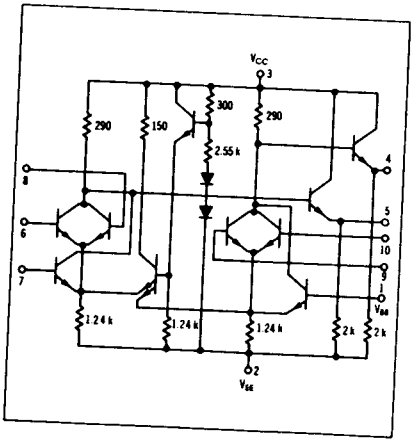
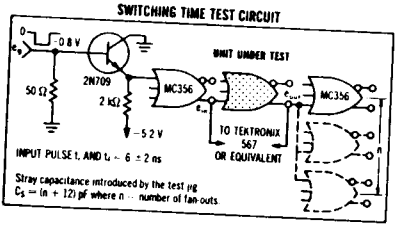
MC362A

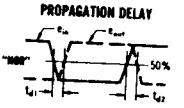
Dual 3-input gate that provides the positive logic "NOR" function, and features an internal bias driver. This gate is available without bias driver as MC362.



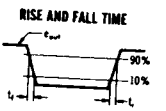
SWITCHING TIME TEST CIRCUIT



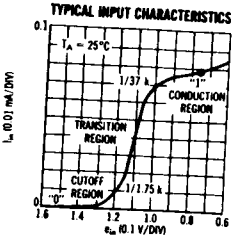
PROPAGATION DELAY



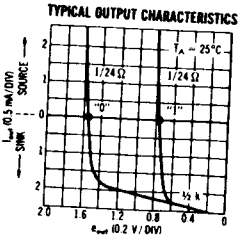
RISE AND FALL TIME



TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



ELECTRICAL CHARACTERISTICS

	Test Conditions $V_{dc} \pm 1\%$			
@ Test Temperature 0°C	—	−0.850	−1.350	−5.20
@ Test Temperature +25°C	−0.670	−0.795	−1.350	−5.20
@ Test Temperature +75°C	—	−0.725	−1.350	−5.20

Characteristic	V_{H} Pin No	$V_{l,max}$ Pin No	V_{l} Pin No	V_{EE} Pin No	dV_{in} Pin No	I_{l} Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	1,2,6,7,8,9,10	—	—	3	I_E (2)	—	17.7	—	17.0	—	16.4	mAdc
Input Current	1	—	—	2,6,7,8,9,10	—	—	3	I_{in} (1)	—	—	—	100	—	—	μAdc
	6	—	—	1,2,7,8,9,10	—	—	3	I_{in} (6)	—	—	—		—	—	
	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—		—	—	
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—		—	—	
	9	—	—	1,2,6,7,8,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	6	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	7	1,2,6,8,9,10	—	—	3	V_1 (5)							
	—	—	8	1,2,6,7,9,10	—	—	3	V_1 (5)							
	—	—	1	2,6,7,8,9,10	—	—	3	V_1 (4)							
	—	—	9	1,2,6,7,8,10	—	—	3	V_1 (4)							
	—	—	10	1,2,6,7,8,9	—	—	3	V_1 (4)							
"NOR" Logical "0" Output Voltage	—	6	—	1,2,7,8,9,10	—	—	3	V_0 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	7	—	1,2,6,8,9,10	—	—	3	V_0 (5)							
	—	8	—	1,2,6,7,9,10	—	—	3	V_0 (5)							
	—	1	—	2,6,7,8,9,10	—	—	3	V_0 (4)							
	—	9	—	1,2,6,7,8,10	—	—	3	V_0 (4)							
	—	10	—	1,2,6,7,8,9	—	—	3	V_0 (4)							
"NOR" Output Voltage Change	—	—	6	1,2,7,8,9,10	—	5①	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.065	Volts
	—	—	1	2,6,7,8,9,10	—	4①	3	ΔV_1 (4)	—	−0.055	—	−0.055	—	−0.065	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9,10	6②	—	3	V_3 (5)	—	−0.51	—	−0.55	—	−0.63	Vdc
	—	—	—	1,2,6,8,9,10	7②	—	3	V_3 (5)	—		—		—		
	—	—	—	1,2,6,7,9,10	8②	—	3	V_1 (5)	—		—		—		
	—	—	—	2,6,7,8,9,10	1②	—	3	V_3 (4)	—		—		—		
	—	—	—	1,2,6,7,8,10	9②	—	3	V_3 (4)	—		—		—		
	—	—	—	1,2,6,7,8,9	10②	—	3	V_3 (4)	—		—		—		
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	5	—	1,2,7,8,9,10	—	—	3	t_{dr} (5)	6.5	10.5	6.5	10.5	7.5	11.5	ns
	1	4	—	2,6,7,8,9,10	—	—	3	t_{dr} (4)	6.5	10.5	6.5	10.5	7.5	11.5	
	6	5	—	1,2,7,8,9,10	—	—	3	t_{df} (5)	8.5	11.5	8.5	11.5	10.0	15.0	
	1	4	—	2,6,7,8,9,10	—	—	3	t_{df} (4)	8.5	11.5	8.5	11.5	10.0	15.0	
Rise Time	6	5	—	1,2,7,8,9,10	—	—	3	t_r (5)	9.0	12.5	9.5	12.5	11.5	15.5	
	1	4	—	2,6,7,8,9,10	—	—	3	t_r (4)	9.0	12.5	9.5	12.5	11.5	15.5	
Fall Time	6	5	—	1,2,7,8,9,10	—	—	3	t_f (5)	8.5	14.0	9.0	14.0	11.5	17.0	
	1	4	—	2,6,7,8,9,10	—	—	3	t_f (4)	8.5	14.0	9.0	14.0	11.5	17.0	

Pins not listed are left open.
①Input voltage is adjusted to obtain dV "NOR" / $dV_{in} = 0$. ②Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)