User's Guide

ADC3664EVM

ABSTRACT

This user's guide describes the characteristics, operation, and use of the ADC3664 evaluation module (EVM). This user's guide discusses how to set up and configure the software and hardware, and reviews various aspects of the program operation. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the ADC3664EVM. In the following sections of this document, the ADC3664 evaluation board is referred to as the EVM and the ADC3664 device is referred to as the ADC device.

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Trademarks

1 Introduction

The ADC3664EVM is an evaluation board used to evaluate the ADC3664 analog-to-digital converter (ADC) from Texas Instruments. The ADC3664EVM is a dual-channel, 14-bit ADC that can operate up to 125 Mega-samples per second (MSPS). The ADC3664 uses a serial LVDS (SLVDS) interface to output the digital data. The SLVDS interface supports output rates to ~1 Gbps. The ADC3664 can be operated in 'oversampling + decimating' mode using the internal decimation filter in order to improve the dynamic range and relax external anti-aliasing filter.

The ADC3664EVM is equipped with the following features:

- Transformer and FDA coupled analog inputs
- Transformer coupled or single-ended clock inputs
- INA226 current shunt monitors for evaluating power consumption
- Power over mini-USB
- FMC connector

By default, the EVM is configured to receive external inputs for the sampling clock and analog input via AC-coupled, transformer (balun) inputs. These transformers perform single-ended to differential conversion, and provide a low noise/distortion passive input.

To exercise the full performance capabilities of this high performance SAR ADC, it is recommended to evaluate the ADC in the default configuration, and then evaluate in other configurations (like utilizing the FDA input), as required.

2 Equipment

This hardware setup procedure is written with the intent to use external clocking (sample clock and DCLKIN) and transformer coupled analog inputs. Using onboard FDA driven analog inputs is an option, and instructions are provided toward the end of this document to make the required hardware/software modifications.

2.1 ADC3664EVM Functionality

The ADC3664EVM receives power from the USB 2.0, +5 V rail, and is then converted to +3.3 VDC and +1.8 VDC. The ADC receives +1.8 VDC from the TPS62231 DC-DC converter. The power consumption of the 1.8 V rail can be monitored (using the INA226) in the ADC35xxEVM GUI. USB-to-SPI communication is established using the FTDI (FT4234H). The ADC clocks are supplied externally, and have limited functionality for the onboard CDCE6214 (Decimation modes only). The ADC3664 analog input can be AC coupled through the Balun (ADT1-6T+) input, or DC (or AC) coupled with the onboard FDA (THS4541). The analog input is 3.2 Vpp, and is driven a -1 dBFS (~2.8 Vpp) in all examples in this user's guide.

The ADC3664 has a +1.6 V voltage reference (VREF), and can be supplied internally or externally. By default, the EVM is configured to supply an external voltage reference using the REF3318 (divided down to +1.6V) and the OPA837 high speed amplifier to drive the voltage reference. At any time, the VREF can be changed to internal reference by SPI write.

The ADC3664 family uses an unbuffered analog input, so a glitch filter is required to attenuate the ADC sampling glitch from when the sampling capacitors switch (sample/hold). The glitch filter acts as a low pass filter with an corner frequency (Fc) at 30 MHz (accepts DC to 30 MHz). The Fc of the glitch filter can be modified by changing filter components.

The ADC3664EVM LVDS output data is routed to an FMC connector, and then connected to the LVDS Interposer card. This interposer card then maps to the TSW1400EVM's HSMC connector in order to capture the ADC36XXEVM SLVDS clock and data signals.

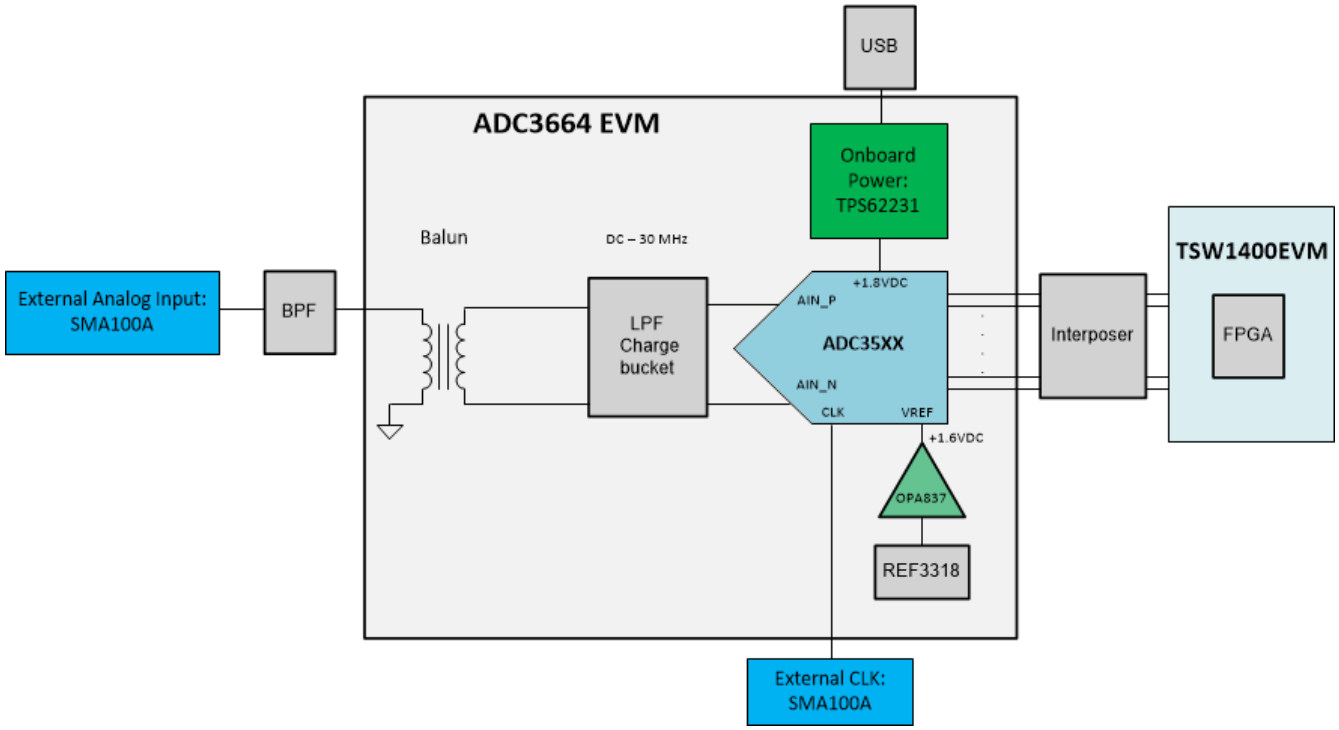

Figure 2-1. ADC3664EVM Block Diagram: Balun Input

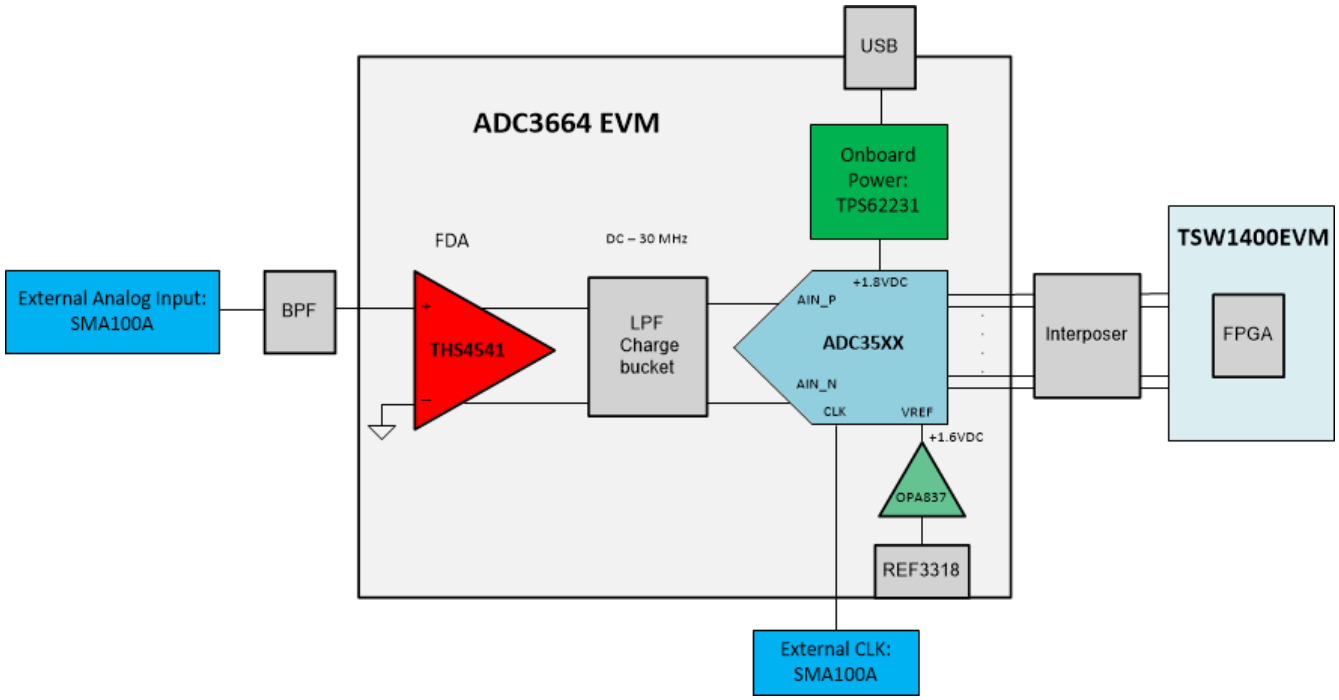

Figure 2-2. ADC36xxEVM Block Diagram: FDA Input

2.2 Evaluation Board Feature Identification Summary

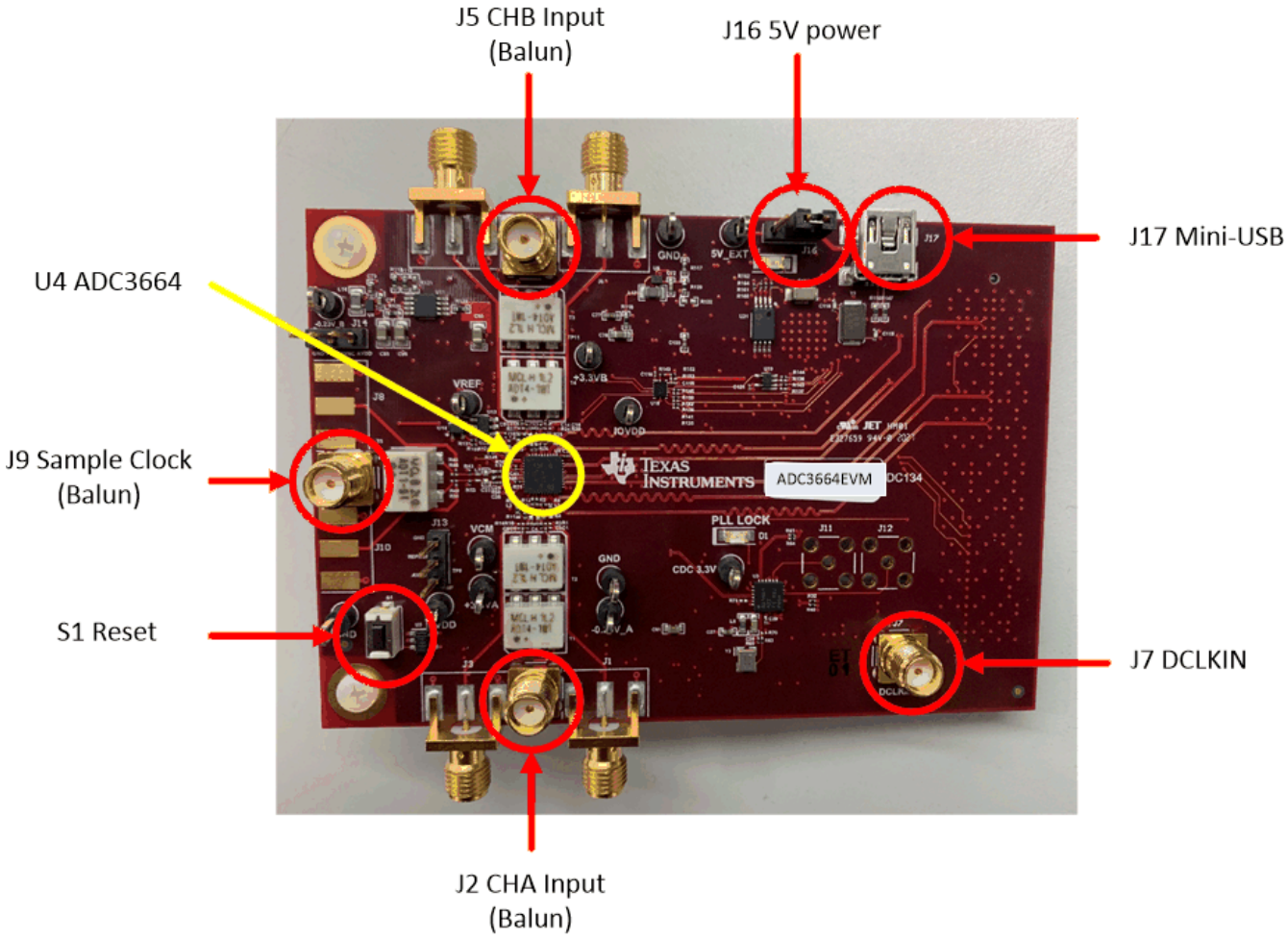

Figure 2-3. ADC3664EVM Feature Identification

Ensure that jumper J16 is shunted in the 2-3 position. This allows 5 V to be supplied to the ADC3664EVM through the mini-USB connector.

If an external 5-V supply is desired, J16 must be shunted in the 1-2 position, and the external 5 V can be connected to the test point labeled "+5 EXT". The USB data connection will still be connected for SPI communications.

J13 is tied to the REFBUF pin. It can be left floating, or can be tied to 1.8 V (shunt pins 2-3) for normal operation.

J14 is tied to the PDN/SYNC pin. It can be left floating for tied to ground (shunt pins 1-2) for normal operation. To power down the ADC, tied to 1.8 V (shunt pins 2-3). The ADC may also be powered down via SPI.

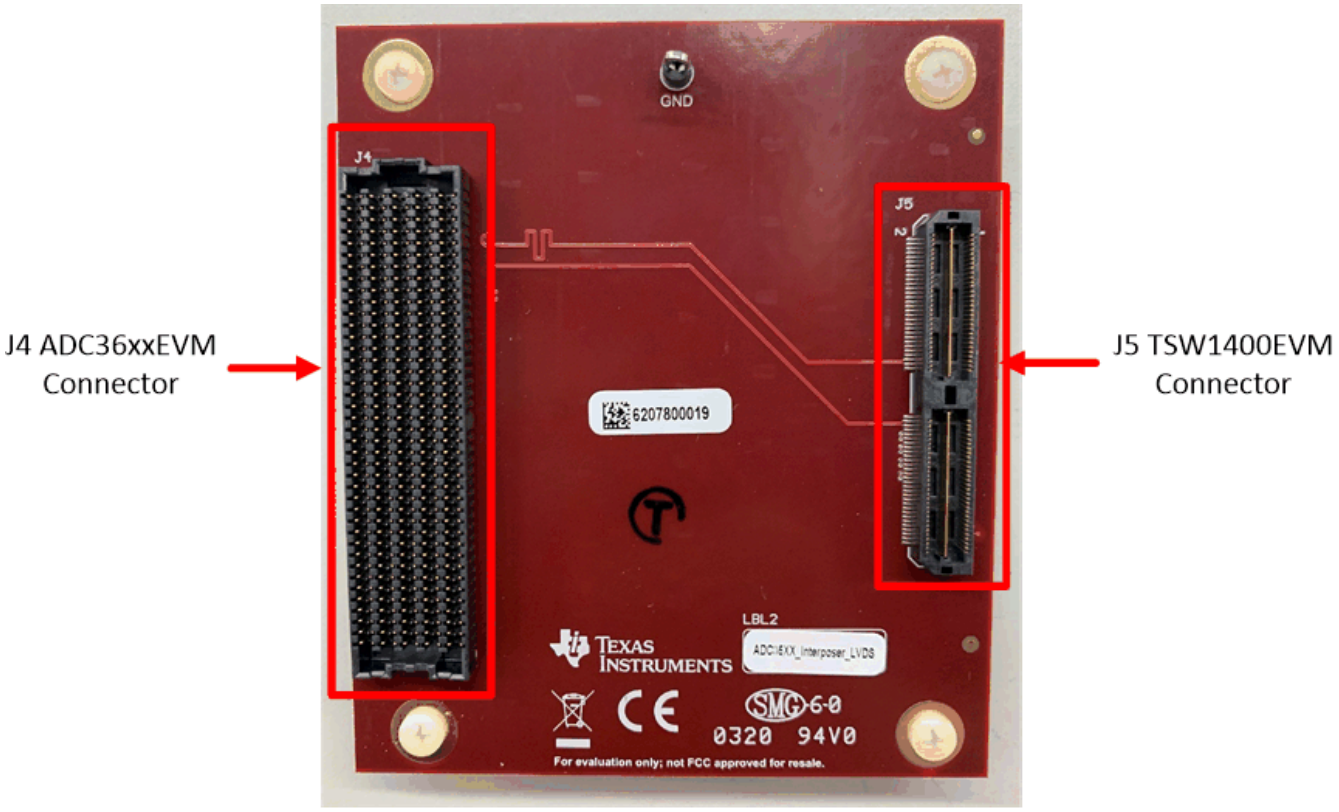

Figure 2-4. LVDS Interposer

2.3 Required Equipment

- The following equipment is included in the EVM evaluation kit:
  - ADC3664 Evaluation board (EVM)
  - LVDS FPGA Interposer Card
  - Mini-USB cable

The following equipment is **not** included in the EVM evaluation kit, but is required for evaluation of this EVM:

- TSW1400EVM data capture board and related items
- HSDC Pro software
- PC running Microsoft® Windows® 7, or 10
- One low-noise signal generators for the analog input (If using external clock option, additional signal generator is required).
- Two low-noise signal generators for the sample clock and DCLKIN. (These two signal generators must share the same reference frequency).

TI recommends the following generators:

- Rohde & Schwarz SMA100A
- Rohde & Schwarz SMA100B

A bandpass filter is required for the analog input signal due to most signal generators addition of phase noise or spurious components. A bandpass filter should also be used for the sample clock input. The DCLKIN input does not require a bandpass filter. If bandpass filters are not used, then the true performance of the ADC may not be seen clearly, and will be limited by the performance of the signal generators being used.

The following recommended bandpass filter will have:

- Bandpass filter, greater than or equal to 60-dB harmonic attenuation, less than or equal to 5% bandwidth, greater than 18-dBm power, less than 5-dB insertion loss
- Signal-path cables, SMA

3 Setup Procedure

This Setup Procedure will detail how to setup the ADC3664EVM hardware and software GUI required for evaluation using external sample and DCLKIN clocks.

3.1 Install High-Speed Data Converter (HSDC) Pro Software

Download the most recent version of the HSDC Pro software. Launch the executable, and accept the default installation options.

Download and install the HSDC Pro Patch. This patch copies all the INI files required to the HSDC pro directory.

3.2 Install ADC35XXEVM GUI 1.0 Software

Download the ADC35XXEVM GUI 1.0 software from the EVM tool folder at ADC3664EVM.

Extract and run the executable file, and accept the default installation options.

3.3 Connect the ADC3664 EVM and TSW1400EVM

Connect the ADC3664EVM FMC connector to J4 of the LVDS Interposer Card.

Connect J5 of the LVDS Interposer Card to J1 of the TSW1400EVM.

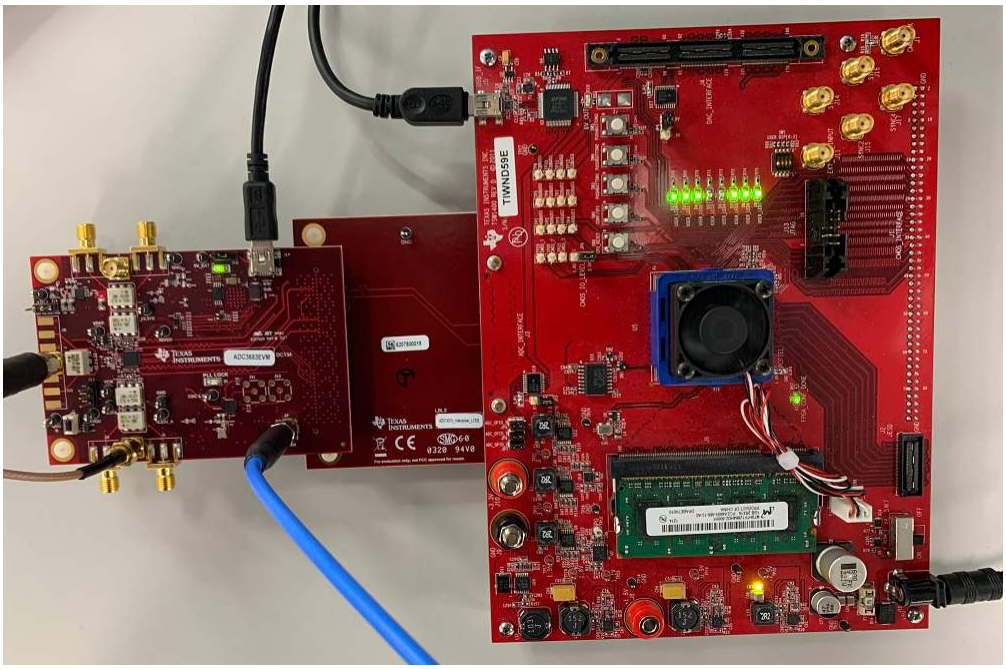

Figure 3-1. ADC3664EVM Complete Setup (external clocks)

3.4 Connect the Power Supply and Mini-USB Connections

Use the following steps to connect the power supply and mini-USB connections:

1. Connect the power cable to the TSW1400EVM at 5 V (minimum 3 A) power supply. Place the power switch (SW7) to the "On" position.
2. Connect the mini-USB cable to the TSW1400EVM (J2).
3. Connect the mini-USB cable to the ADC3664EVM (J16).

3.5 Connect the Clocks and Analog Input

Use the following steps to connect the external ADC clocks and analog input. The clock rates shown below are for the power on/default settings (bypass mode/non-decimation), but the physical connections and signal power levels will remain the same for all ADC modes.

1. For the sample clock (ADC3664EVM), set a signal generator to 125 MHz at a power level of +10 dBm. Connect to the SMA connector J4. A bandpass filter for the sample clock is recommended for best AC performance of the ADC3664EVM.
2. For the DCLKIN clock (ADC3664EVM), set a signal generator to 437.5 MHz at a power level of +10 dBm. A bandpass filter is not required for the DCLKIN clock.

   External ADC sampling clock source and DCLKIN source must be frequency locked. If this is not performed, the captured data will appear scrambled. If using the onboard clocking option, the sampling clock and DCLKIN are frequency locked.
3. For the analog input, set a signal generator to 10 MHz at a power level of ~ +15 dBm. A bandpass filter is required to reduce harmonic and phase noise effects of the signal generator.

4 Device Configuration

A hardware reset should be performed before programming the ADC by toggling the push button switch S1.

A software reset can be performed at any time to reset the ADC registers to their default state.

4.1 Bypass Mode

The steps in Section 4.1.1 show how to configure the ADC3664EVM in Bypass mode.

4.1.1 ADC35XX GUI: Bypass Mode Configuration

After power up, the ADC3664EVM is preconfigured for 14 bit, 2W Bypass Mode (No Decimation). There are other modes and sample rates that can be used in Bypass Mode, and Table 4-1 shows examples of required clocks for different serialization options (1W and 1/2W). To calculate the correct DCLKIN frequency for the desired sampling rate and mode, multiply the sampling rate by the DCLKIN multiplier (Serialization factor).

Table 4-1. 14-Bit, Bypass Sample Rate and DCLKIN Examples (ADC3664EVM)

Interface Mode	DCLKIN Multiplier (Serialization factor)	Example Sample Clock	Required DCLKIN Frequency
2 Wire	3.5	125 MSPS	437.5 MHz
1 Wire	7	65 MSPS	455 MHz
1/2 Wire	14	35 MSPS	490 MHz

For this 14 bit, 2-Wire example, ensure that the sampling clock (J9) and DCLKIN (J7) are connected before launching the ADC35XX EVM GUI. In this example, the sampling clock is 125 MHz, and the DCLKIN is 437.5 MHz.

External ADC sampling clock source and DCLKIN source must be frequency locked. If this is not performed, the captured data will appear scrambled. If using the onboard clocking option, the sampling clock and DCLKIN are frequency locked.

After launching the ADC35xx GUI, the below items should already be populated. If not, perform the following steps for 14 bit, 2W Bypass mode:

1. Under Resolution, select "14 bit".
2. Under Mode, select "2 Wire".
3. Under DDC, select "Bypass".
4. Enter "125M" for "Fs (MHz)".
5. Ensure that "CDC Enable" is red (disabled).
6. Click "Configure" button.

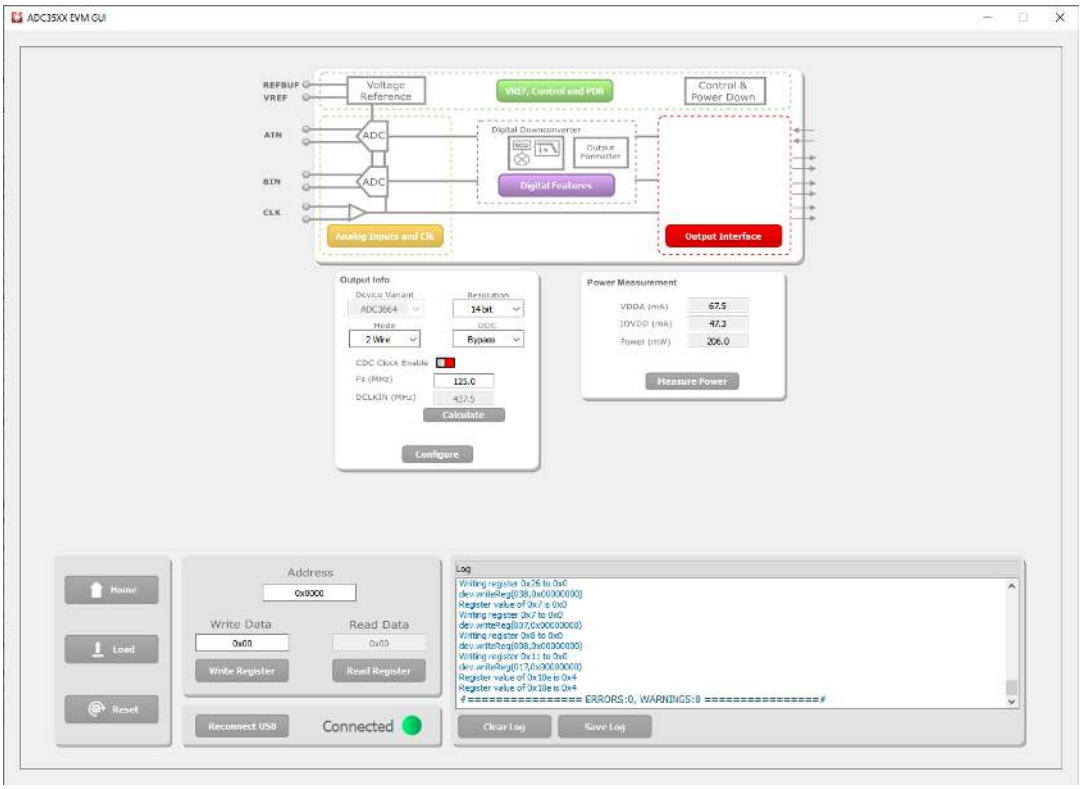

Figure 4-1. ADC35XXEVM GUI: ADC3664EVM Bypass Mode

4.1.2 HSDC Pro: Bypass Mode

After pressing "Configure" within the ADC35xx GUI perform the following steps to setup HSDC pro:

1. Launch HSDC Pro
2. Select the TSW1400 and click OK.

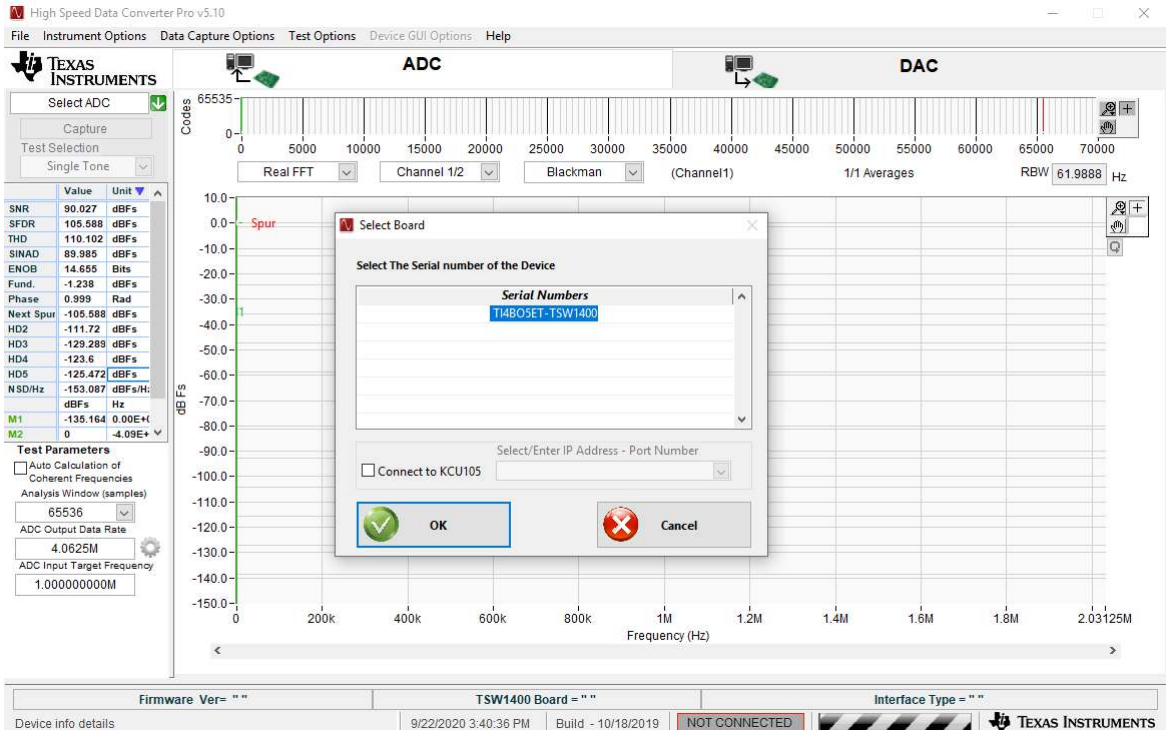

Figure 4-2. HSDC Pro: Connect to TSW1400

3. Click OK for the no firmware loaded prompt.
4. Select “ADC3664_2W_14 bit" to load firmware, and click Yes.

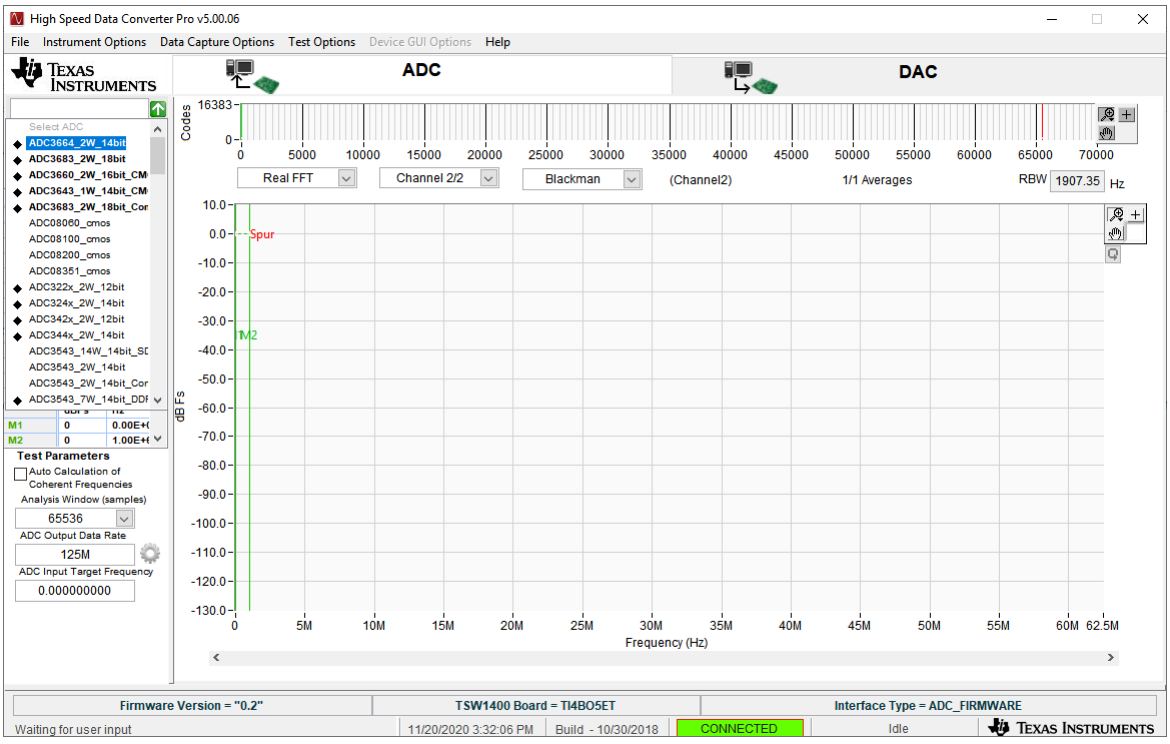

Figure 4-3. HSDC Pro: ADC3664_2W_14bit Ini File

5. Enter "125M" within the box that says “ADC Output Data Rate”.
6. Press Capture.

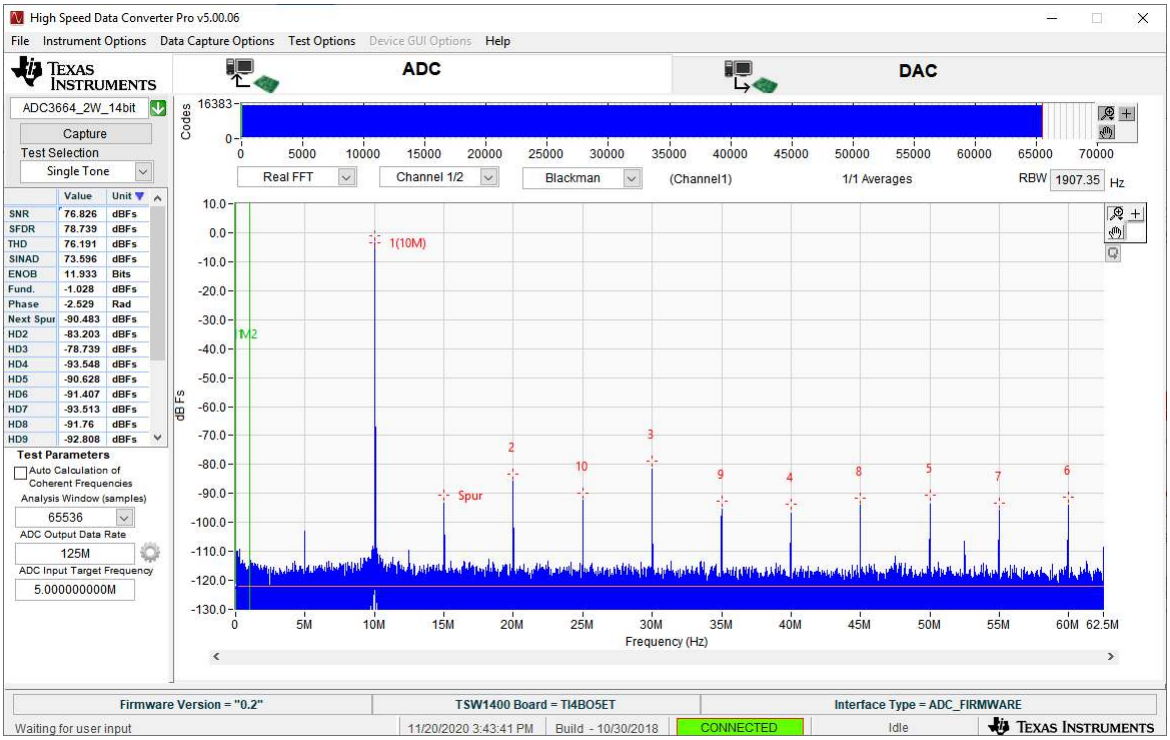

Figure 4-4. ADC3664EVM Bypass (10 MHz balun input)

7. The analog input signal power may need to be adjusted to reach -1 dBFS.

4.2 Real Decimation Mode

The software configuration steps shown in Section 4.2.1 will program the ADC3664EVM in 8x Real Decimation mode.

4.2.1 ADC35XX GUI: Real Decimation Mode Configuration

Table 4-2. 14-Bit, Real Decimation, Sample Rate and DCLKIN Examples

Interface Mode	DCLKIN Multiplier (Serialization Factor)	Example Sample Clock	Real Decimation Factor	Required DCLKIN Frequency
2 Wire	3.5	125 MSPS	2	218.75 MHz
1 Wire	7	65 MSPS	8	56.875 MHz
1/2 Wire	14	35 MSPS	32	15.3125 MHz

For this 14 bit, 2-Wire 8x Real Decimation example, apply a 125 MHz signal to J9 (sample clock) and a 54.6875 MHz signal to J7 (DCLKIN).

> External ADC sampling clock source and DCLKIN source must be frequency locked. If this is not performed, the captured data will appear scrambled. If using the onboard clocking option, the sampling clock and DCLKIN are frequency locked.

Apply a 5 MHz signal to J2 (ensure bandpass filter is used to reduce harmonics and noise of signal generator).

After launching the ADC35xx GUI perform the following steps:

1. Under Resolution, select "14 bit".
2. Under Mode, select "2 Wire".
3. Under DDC, select "Real".
4. For Decimation Factor, select "8".
5. To calculate the DCLKIN frequency, enter "125" in the Fs(MHz) field, and click calculate. This is informational only.
6. Ensure that "CDC Enable" is red (disabled).
7. Click "Configure"

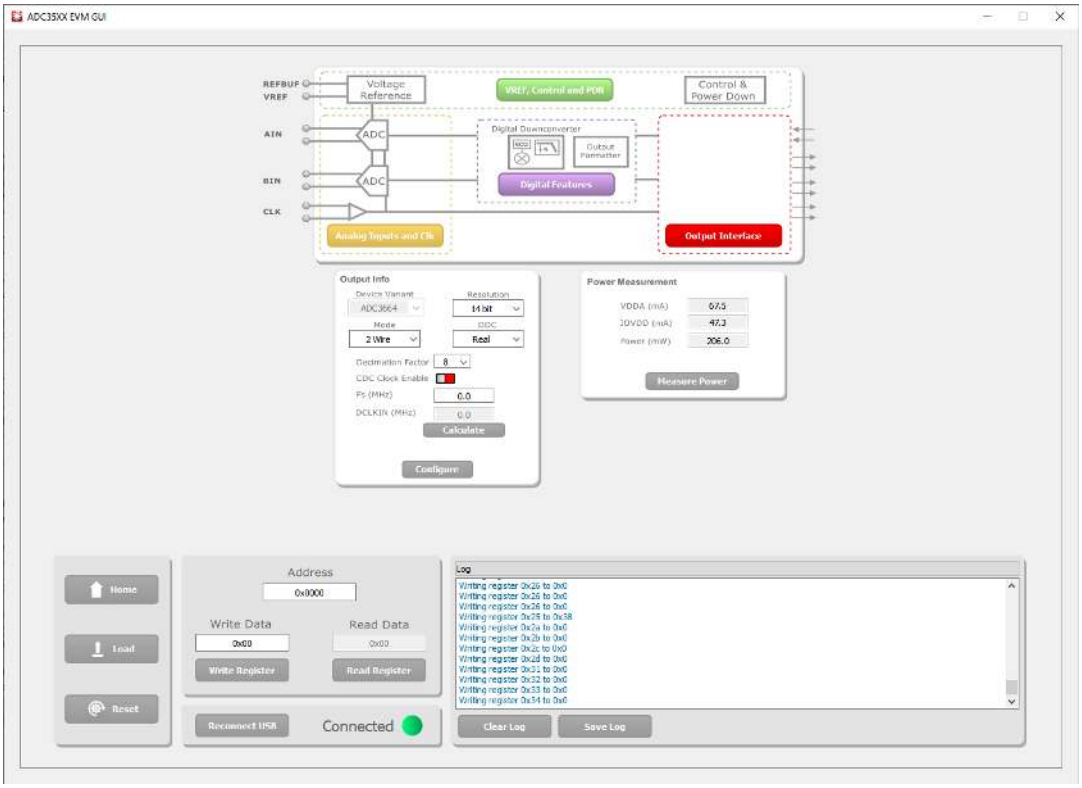

Figure 4-5. ADC35XXEVM GUI: ADC3664EVM 8x Real Decimation

4.2.2 HSDC Pro: Real Decimation Mode

After pressing "Configure" within the ADC35xx GUI perform the following steps to setup HSDC pro:

1. Launch HSDC Pro.
2. Select the TSW1400 and click OK.
3. Click OK for the no firmware loaded prompt.
4. Select “ADC3664_2W_14bit” to load firmware, and click Yes.

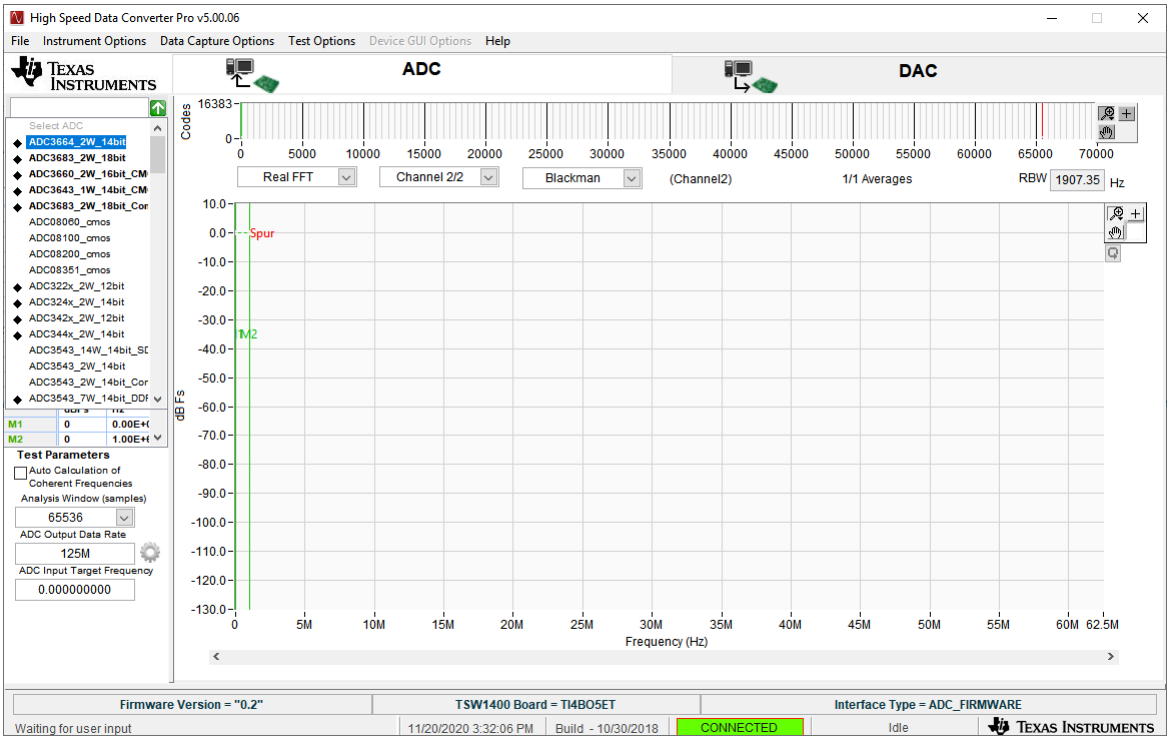

Figure 4-6. HSDC Pro: ADC3664EVM Real Decimation Ini File

5. Click on the cog next to “ADC Output Data Rate”.

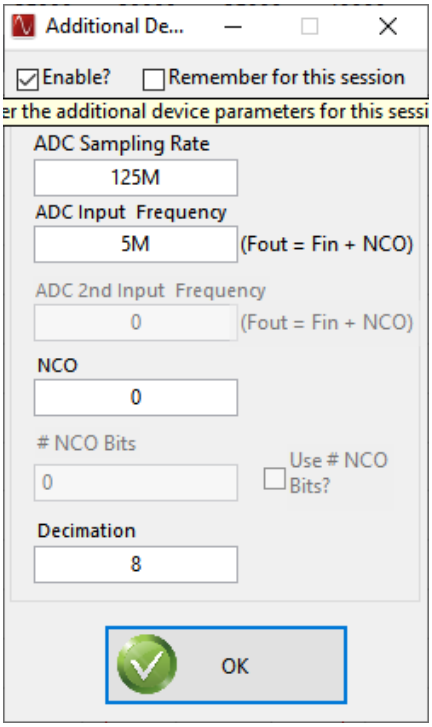

Figure 4-7. Real Decimation Mode HSDC Pro Parameters

6. In the new dialogue box, enter "125M" in “ADC Sampling Rate”.
7. Enter "5M" in “ADC Input Frequency”.
8. Enter "8" in “Decimation”.
9. Click Ok.
10. Click the "Capture" button.

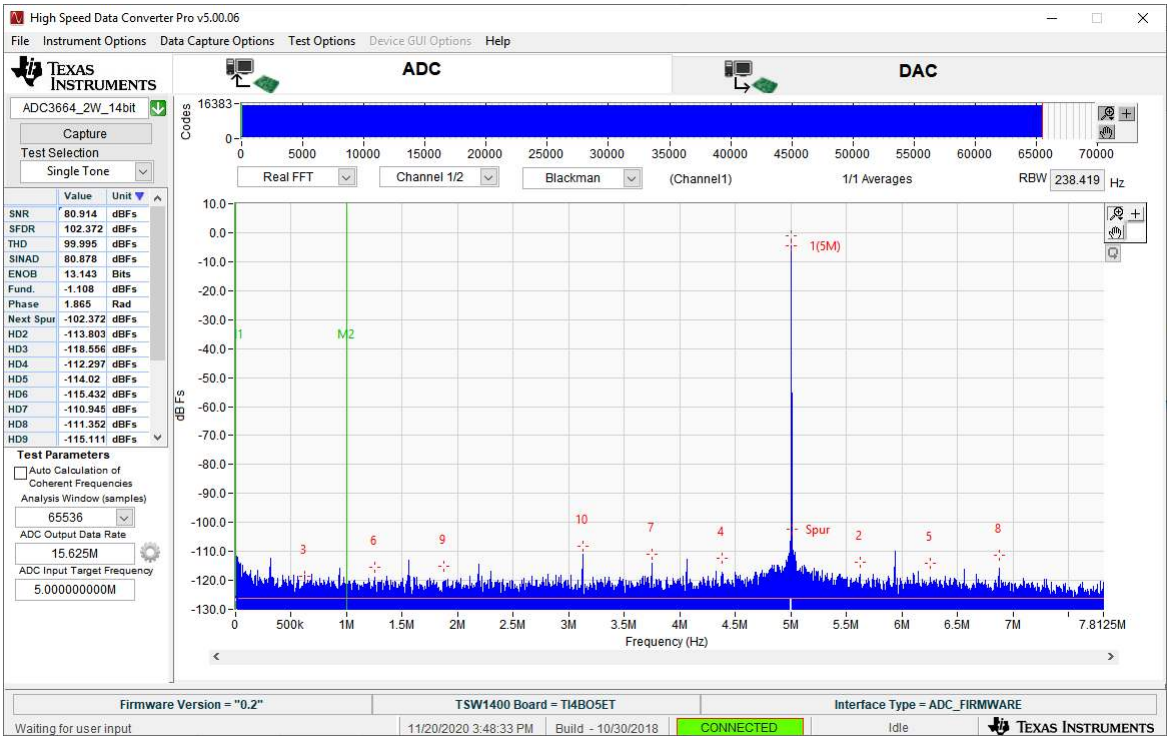

Figure 4-8. HSDC Pro: ADC3664EVM 8x Real Decimation

4.3 Complex Decimation Mode

The software configuration steps shown in Section 4.3.1 will program the ADC3664EVM (external clocks) in Complex Decimation mode (32x) with a 5 MHz analog input and 4.9 MHz NCO.

4.3.1 ADC35XX GUI: Complex Decimation Configuration

Table 4-3. 14-Bit, Complex Decimation, Sample Rate and DCLKIN Examples

Interface Mode	DCLKIN Multiplier (Serialization Factor)	Example Sample Clock	Complex Decimation Factor	Required DCLKIN Frequency
2 Wire	3.5	125 MSPS	2	437.5 MHz
1 Wire	7	65 MSPS	8	113.75 MHz
1/2 Wire	14	35 MSPS	32	30.625 MHz

For this 32x Complex Decimation example, apply a 125 MHz signal to J9 (sample clock) and a 27.34375 MHZ signal to J7 (DCLKIN).

> External ADC sampling clock source and DCLKIN source must be frequency locked. If this is not performed, the captured data will appear scrambled. If using the onboard clocking option, the sampling clock and DCLKIN are frequency locked.

Apply a 5 MHz signal to J2 (ensure bandpass filter is used to reduce harmonics and noise of signal generator). An NCO of 4.9 MHz will be used to shift the 5 MHz input signal to -100 kHz.

After launching the ADC35xxEVM GUI perform the following steps:

1. Under "Resolution", select "14 bit".
2. Under "DDC", Select "Complex".
3. For "Decimation Factor", select "32".
4. Ensure that CDC is disabled (red).
5. For "Fs (MHz)", select 125M.
6. To calculate the DCLKIN frequency, enter "125" in the Fs (MHz) field, and click calculate. This is informational only.
7. Under "FNCO A (MHz)" and "FNCO B (MHz)", enter "4.9" in the field. This field will then calculate to the nearest valid NCO value, and will auto-calculate the correct register values in the field next to it.
8. Click "Configure".

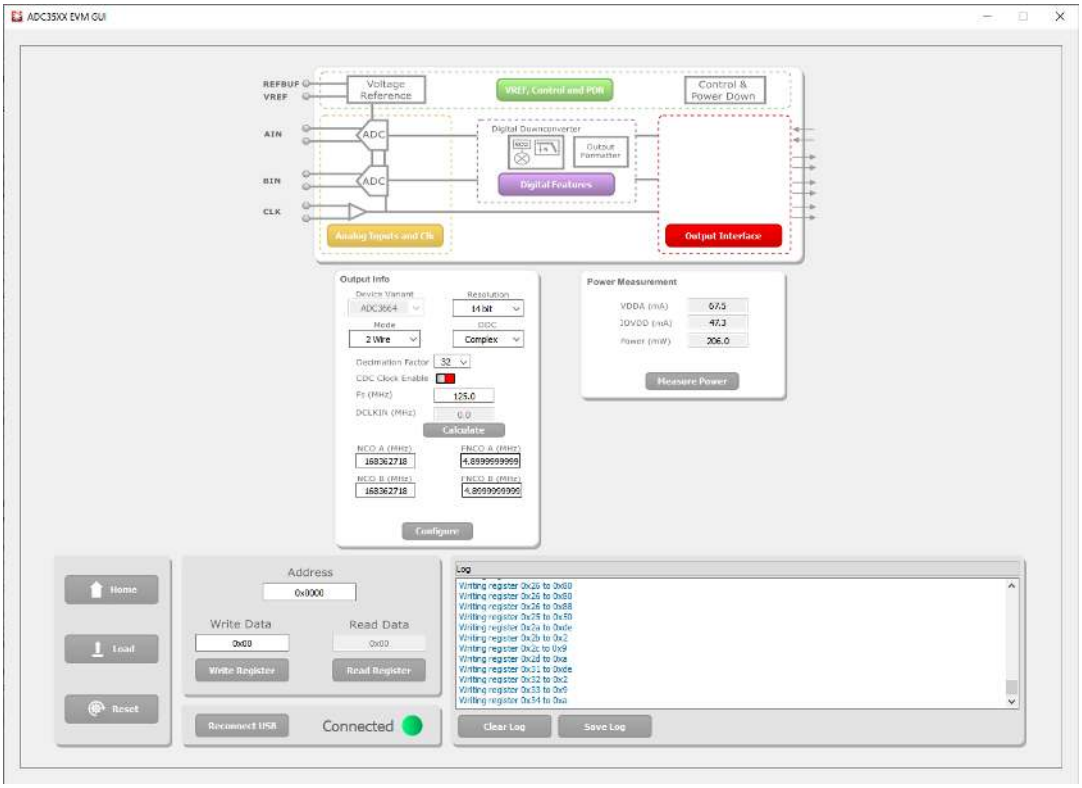

Figure 4-9. ADC35XXEVM GUI: ADC3664EVM 32x Complex Decimation

4.3.2 HSDC PRO: Complex Decimation Mode

After pressing "Configure" within the ADC35xx GUI perform the following steps to setup HSDC pro:

1. Launch HSDC Pro.
2. Select the TSW1400 and click "OK".
3. Click OK for the "no firmware loaded" prompt.
4. Select “ADC3664_2W_14bit_Complex” to load firmware, and click Yes.

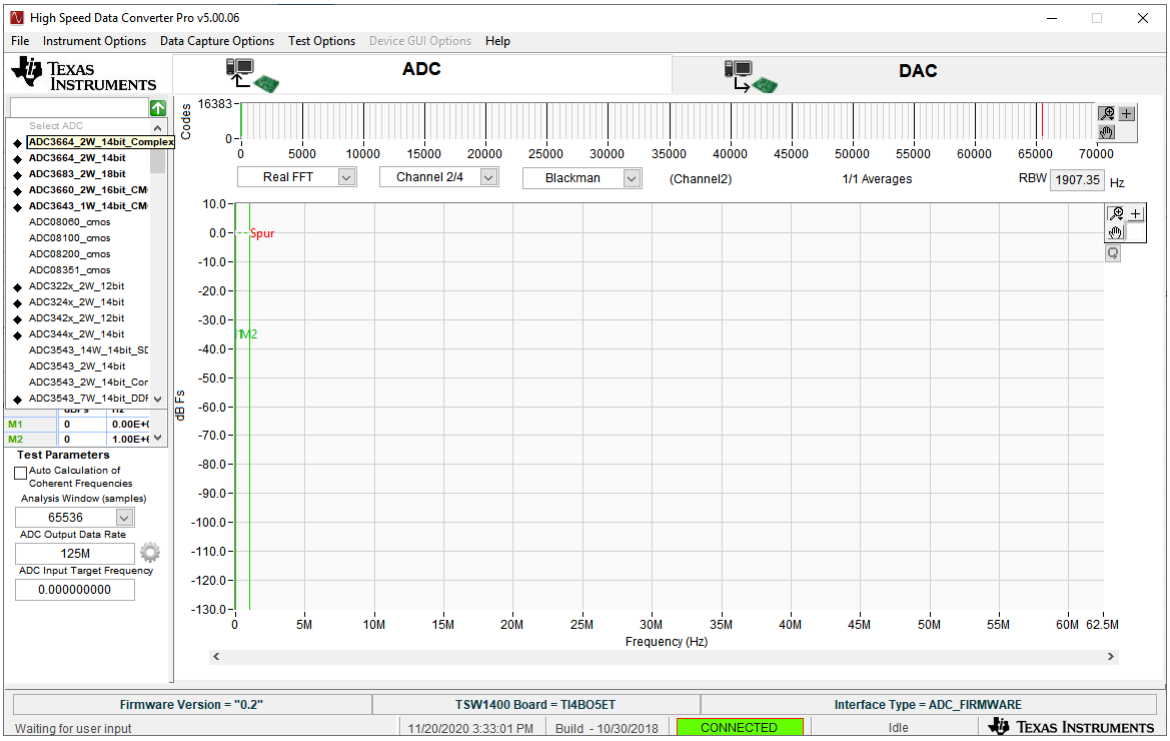

Figure 4-10. HSDC Pro: ADC3664EVM 2Wire Complex Ini File

5. Click on the cog next to “ADC Output Data Rate”.
6. In the new dialogue box, check the "Enable?" box.
7. Under “ADC Sampling Rate”, enter "125M".
8. Under “ADC Input Frequency”, enter "5M".
9. Under "NCO", enter "4.9M".
10. Under “Decimation”, enter "32".
11. Click "OK".

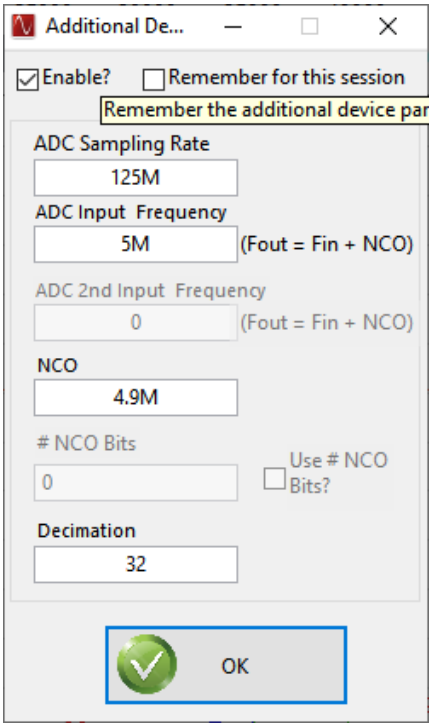

Figure 4-11. HSDC Pro Cog: Complex Decimation

12. Select "Complex FFT".
13. Press "Capture".

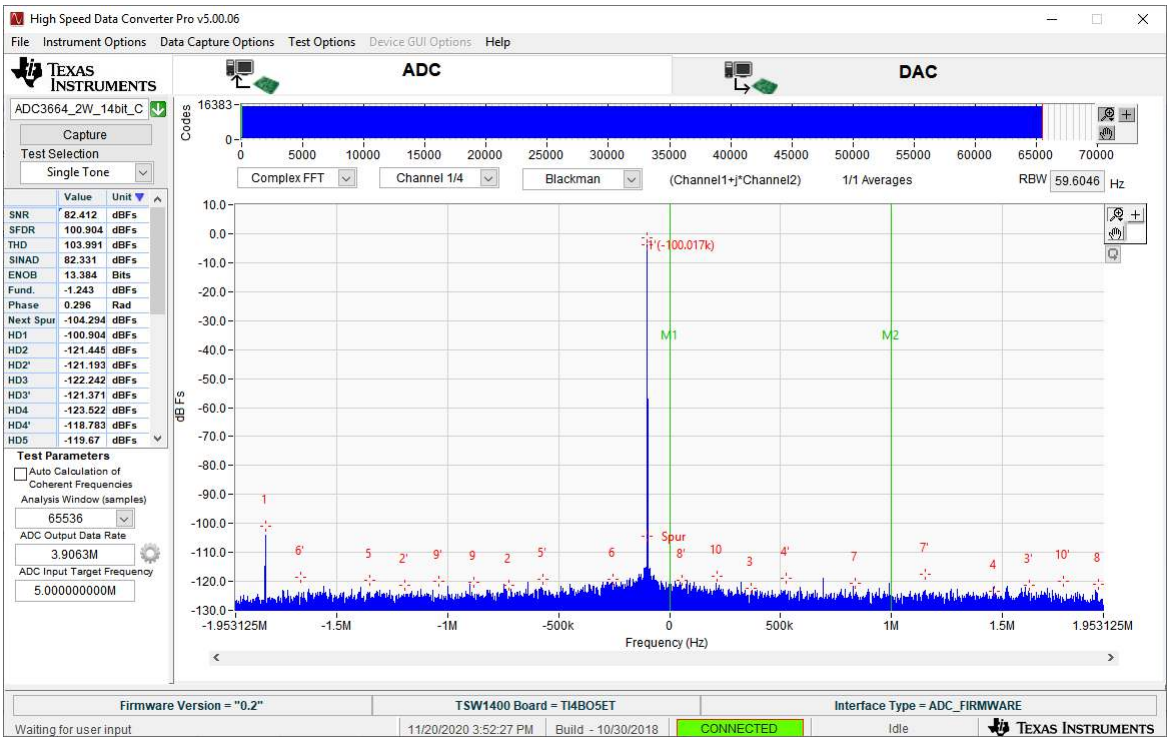

Figure 4-12. HSDC Pro: ADC3664EVM 32x Complex Decimation 5 MHz Input, 4.9 MHz NCO

5 Onboard FDA Configuration

By default, the analog input is configured to use the balun input (AD1T-6T+) for both analog input channels, but can be modified to utilize the onboard FDA (THS4541).

In terms of performance as compared with the balun input, SNR and SFDR are similar up to ~ 15 MHz input frequency. If using input frequencies above 15 MHz, it is recommended to use the balun input.

A benefit of using the FDA is that the required signal strength needs to achieve the full scale input is several dB less when compared to the balun input (losses in 50 ohm termination for balun input).

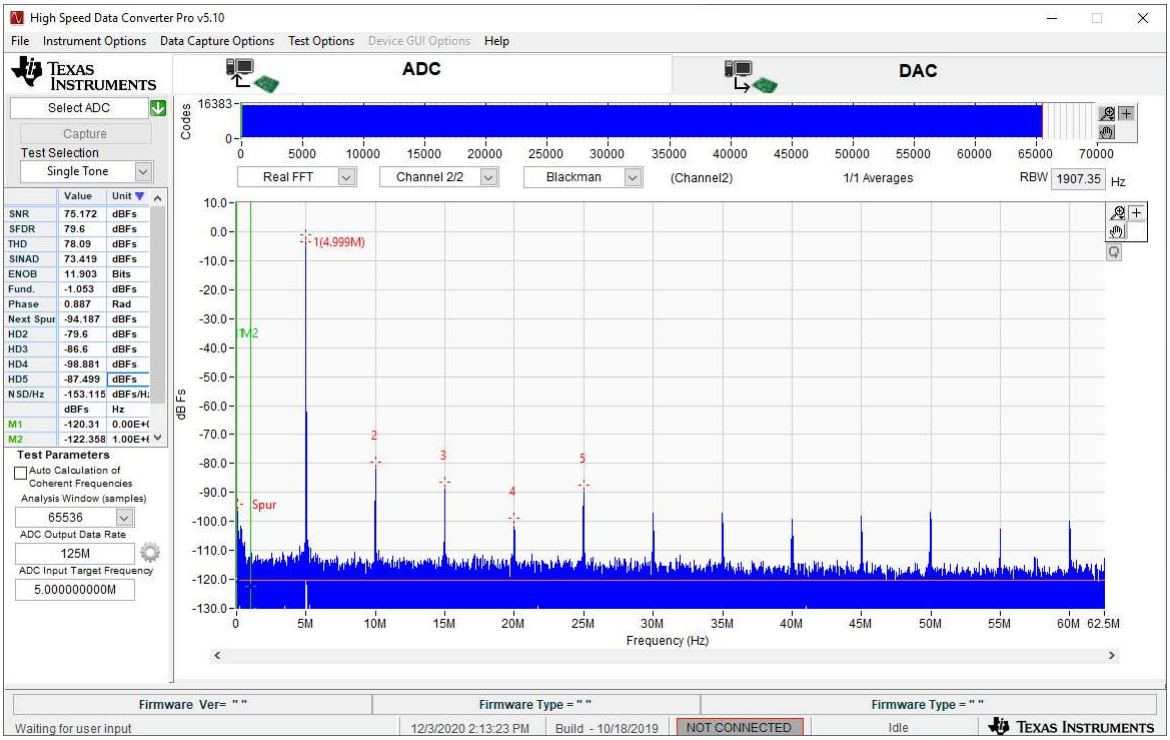

Figure 5-1. ADC3664EVM: FDA Input

This procedure shows how to configure the FDA single-ended to differential conversion for CHA. The same procedure can be performed for CHB (with the respective component designators).

The edge launched SMA connector J1 receives the single-ended analog input signal. R1 can be replaced with a capacitor for AC coupling to FDA.

Modify the following components to complete the path to FDA (located on top of EVM).

1. Install: R1, R2, R14 (o Ω)
2. Remove (DNI): C3, C6, R7, R8

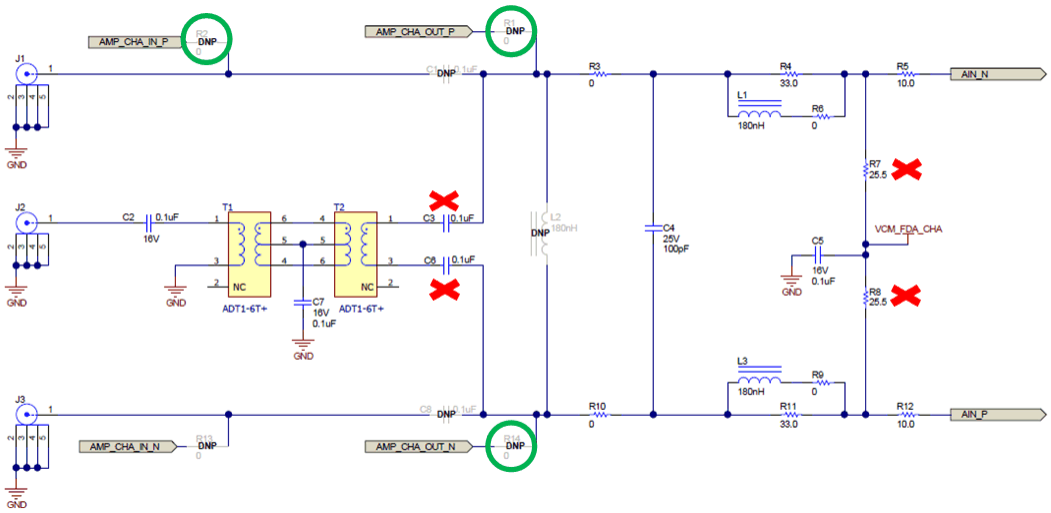

Figure 5-2. CHA FDA Component Modification

The FDA is setup with a gain of 2.5, and can be adjusted (R78, R84, R86 and R94) as the application requires. There is a 20 MHz LPF on the output of the FDA, and these components (C52, L11,L12 and C53) can be adjusted as the application requires. The termination resistors (R80, R81, R89 and R90) can be adjusted according to the source impedance.

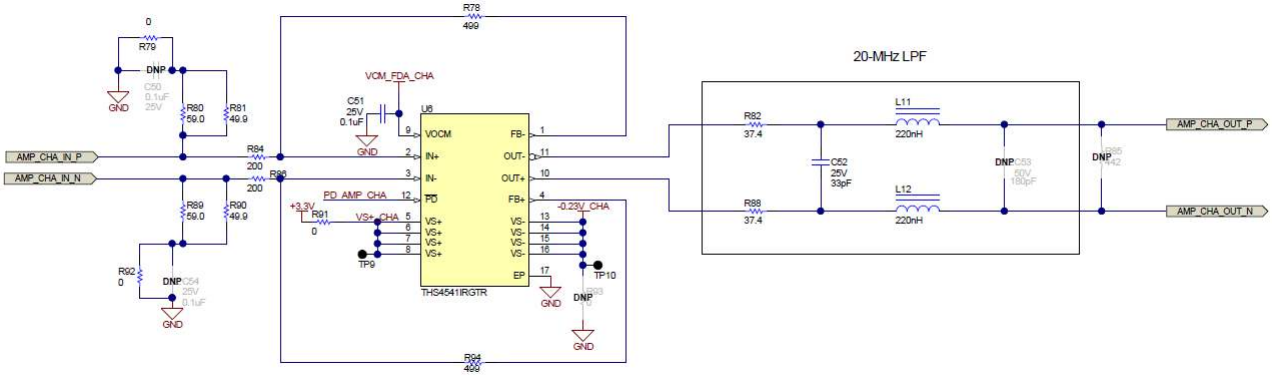

Figure 5-3. FDA Schematic

For further information on the THS4541 FDA, see the *THS4541 Negative Rail Input, Rail-to-Rail Output, Precision, 850-MHz Fully Differential Amplifier data sheet*.

6 ADC3664EVM Power Monitor

The ADC3664EVM is equipped with on-board current shunt monitors that are able to measure the current consumption on the +1.8VDC rails (AVDD and IOVDD). The user has the ability to read the ADC3664EVM's power consumption on the front page of the ADC35XX GUI. Click the "Measure Power" button to refresh the current values. This feature is useful for determining what mode/sampling speed offers the best power consumption for your application needs.

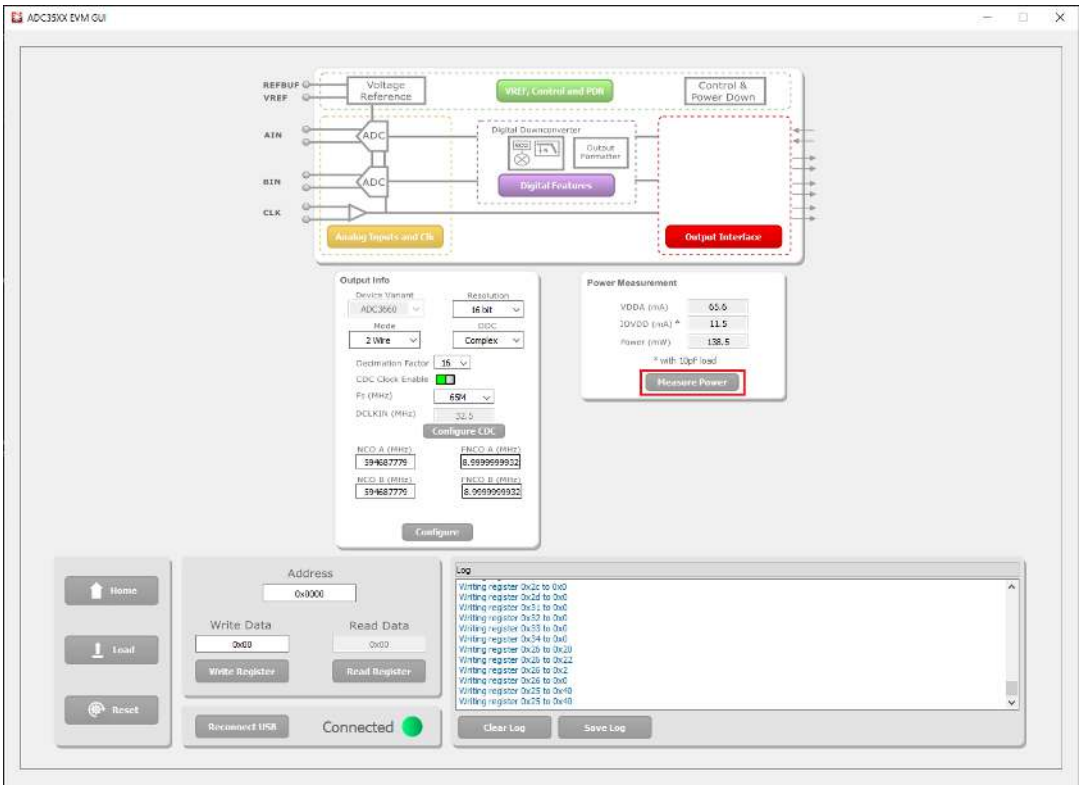

Figure 6-1. ADC3664EVM Power Meter

7 Test Pattern

It is often useful to utilize test patterns to help verify the correct receipt of digital data at the microcontroller or FPGA. A ramp pattern can be enabled by following these steps:

1. Click the yellow button "Analog Inputs and Clk".
2. Next to "Test Pattern CHA", click the drop down menu, and select "RAMP CUSTOM". This can be done for "Test Pattern CHB" as well.
3. In the field next to "Custom Pattern", enter the number "16".
4. The digital ramp pattern is now enabled on the ADC. The output of the ADC is now a 14 bit, incrementing ramp pattern.

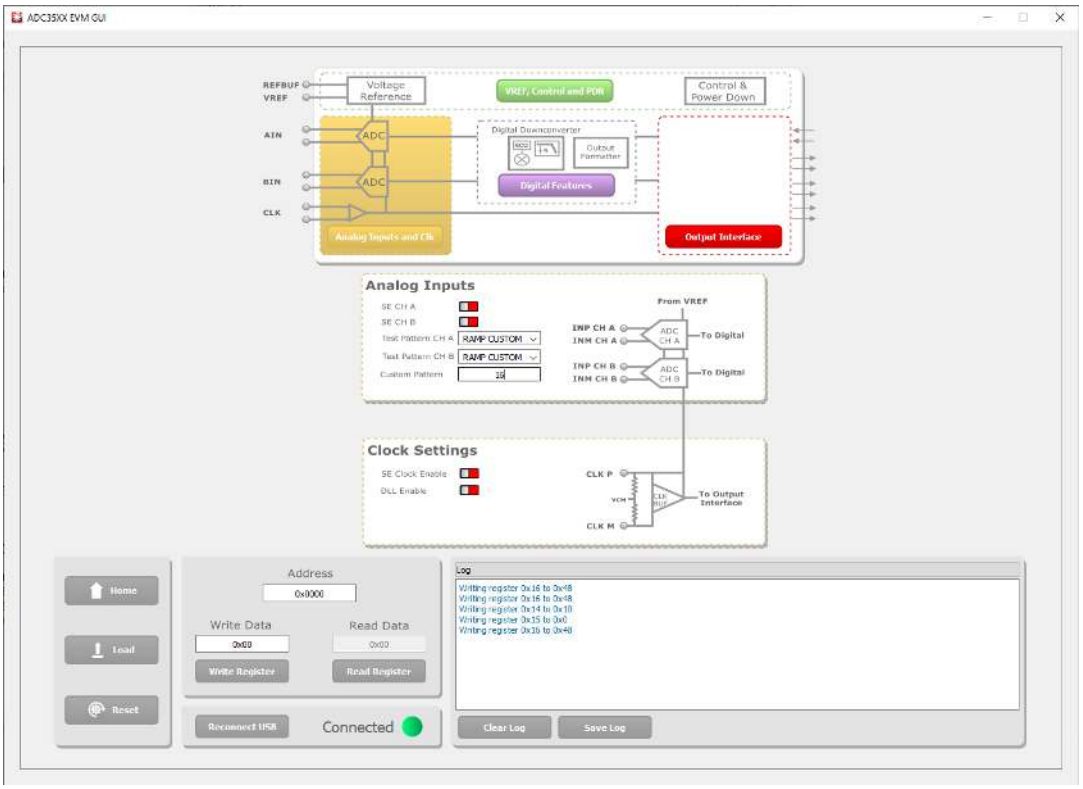

Figure 7-1. ADC35XXEVM GUI 1.0 Ramp Pattern

5. In HSDC Pro, the ramp pattern can now be seen when data is captured. These same steps apply to any data output mode (Bypass, Real Decimation and Complex Decimation).

Figure 7-2. HSDC Pro Digital Ramp Pattern

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