

BOOSTXL-TPS652170 EVM User's Guide

The BOOSTXL-TPS652170 is a BoosterPack evaluation module (EVM) for programming samples of the TPS652170 power management IC (PMIC) with user-defined values for output voltage, sequence timing, and other critical parameters. Modifying these parameters using the BOOSTXL-TPS652170 allows for rapid prototyping and quick time to market when using the TPS652170 PMIC to provide power to a variety of processors and FPGAs.

This document provides a description of how to setup the EVM and re-program the EEPROM memory of the TPS652170 devices using the BOOSTXL-TPS652170 BoosterPack, an MSP430F5529 LaunchPad, and the IPG-UI software. The steps in this document describe the procedure for programming samples of the TPS652170 installed in the socket of the BOOSTXL-TPS652170 printed circuit board (PCB).

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	Electrical Connections of Headers BOOSTXL-TPS652170 Test Point List BOOSTXL-TPS652170 Jumper List Bill of Materials

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1 Introduction

The BOOSTXL-TPS652170 allows designers to program samples of the TPS652170 and verify the values in the EEPROM match the power-up and power-down sequence requirements of the targeted processor that will be powered by the PMIC in the final application. The BOOSTXL-TPS652170 BoosterPack EVM is simple to test, requiring only an MSP430F5529 LaunchPad and USB A-to-micro B cable. With no load or a light load on the BoosterPack EVM, the power provided by the LaunchPad is sufficient to power the TPS652170 device, re-program the EEPROM, and perform all of the measurements described in this document. The 5 V provided by the VBUS wire of the USB cable is the only power input to the LaunchPad.

The TPS652170 device consists of three step-down converters (DCDC1, DCDC2, DCDC3), one WLED boost converter (DCDC4), two general-purpose LDO regulators (LDO1, LDO2), and two load switches that can be purposed as LDO regulators (LS1/LDO3, LS2/LDO4). The output voltage of all the DC/DC converters and the LDO regulators is programmable. Configuring the load switches as additional LDO regulators is programmable. The sequence order of all DC/DC converters, the LDOs, and the load switches can also be programmed and assigned to integer values relative to each other. The sequence timing and supervisor thresholds are global parameters that can be programmed. The integrated battery charger of the TPS652170 can also be programmed but the BAT, BAT_SENSE, and TS pins are not routed out to test points on the BOOSTXL-TPS65218.

Modifying some or all of these register map values and re-programming the EEPROM of the TPS652170 device with the IPG-UI software creates new reset values for the PMIC, which allows the PMIC to poweron and power-off with the required timing for a variety of processors or FPGAs.

Figure 1 shows the top-side of the BOOSTXL-TPS652170 PCB, on which a socket is placed to install TPS652170 samples and re-program the samples. The samples can then be removed from the socket and soldered down on a TPS65217xEVM or prototype PCB to evaluate the power delivery capabilities of the TPS652170 newly programmed for a specific processor or FPGA. If the output voltages or sequencing are not ideal for the processor or FPGA on the first attempt, the process can be repeated until the ideal programming of the TPS652170 device is determined.





Figure 1. BOOSTXL-TPS652170 Printed Circuit Board (Top View)

This procedure requires:

- 1. An MSP430F5529 LaunchPad development kit, MSP-EXP430F5529LP
- 2. A USB A to micro B cable (included with the LaunchPad development kit)
- 3. A BOOSTXL-TPS652170 BoosterPack plug-in module
- 4. TPS652170 devices (TPS652170RSL)
- 5. An internet connection

Specific instructions on how to program the TPS652170 using the BOOSTXL-TPS652170 with the IPG-UI software are provided in Appendix A, while the EVM documentation related to the design of the BOOSTXL-TPS652170 hardware is provided in Appendix B.

NOTE: All re-programmed EEPROM settings must be validated during prototyping phase to ensure desired functionality because parts cannot be returned in case of incorrect programming. Any issues should be reported to the e2e forum.

1.1 Related Documentation

Texas Instruments, TPS65217x Single-Chip PMIC for Battery-Powered Systems Data Sheet

Texas Instruments, IPG-UI User's Guide

Texas Instruments, TPS65217CEVM User's Guide

Texas Instruments, MSP430F5529 LaunchPad Development Kit (MSP-EXP430F5529LP) User's Guide

1.2 Required Hardware

1.2.1 MSP430F5529 LaunchPad

The MSP430F5529 LaunchPad will serve as a communication interface between the IPG-UI software and the TPS652170 device. The firmware on the MSP430F5529 needs to be updated before it can communicate with the TPS652170. Figure 2 shows the BOOSTXL-TP652170 connected on top of the MSP430F5529 LaunchPad with a micro-USB cable inserted in the LaunchPad.

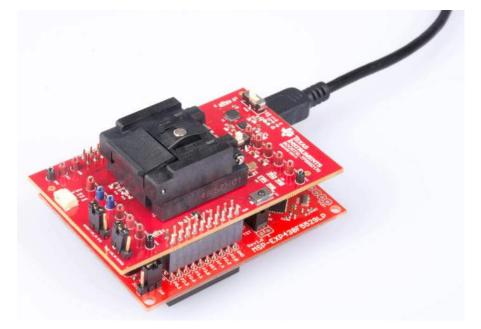


Figure 2. BOOSTXL-TPS652170 and MSP430F5529 LaunchPad Connected

NOTE: Do not plug the BOOSTXL-TPS652170 BoosterPack into the MSP430F5529 LaunchPad before the firmware is updated, as described in Section 2.5.

2 Getting Started

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Figure 3 shows the high-level block diagram of the BOOSTXL-TPS652170 as it is wired to the MSP430F5529 LaunchPad through the two 20-pin headers connecting the two PCBs. It also shows the LaunchPad connected to a computer through a USB cable, which is required for programming the TPS652170 device.



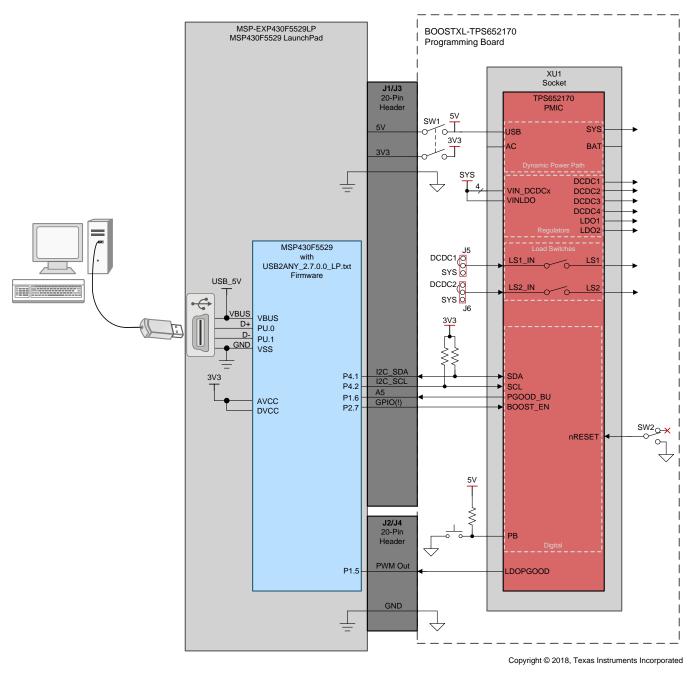


Figure 3. BOOSTXL-TPS652170 BoosterPack and MSP430F5529 LaunchPad Block Diagram

2.1 Connecting Headers

This section describes the headers on the BOOSTXL-TPS652170 used to connect the BoosterPack EVM to the MSP430F5529 LaunchPad. There are two sets of headers numbered J1-J4, each set having two rows of 10 pins, for a total of 40 pins. The outside headers, closest to the board edge, are J1 (left) and J2 (right). The inside headers, closest to the socket on BOOSTXL-TPS652170 and closest to the MSP430F5529 device on the LaunchPad, are J3 (left) and J4 (right). When connected correctly, all 40 pins of the headers make a physical connection from board to board and the headers numbers line up (in other words, J1 connects to J1, J2 connects to J2, and so forth.). However, all 40 pins do not make an electrical connection from the LaunchPad to the BOOSTXL-TPS652170 design.



Getting Started

 Table 1 lists all of the electrical connections made when the headers of the BOOSTXL-TPS652170 and

 MSP430F5529 LaunchPad are connected correctly.

BOOSTXL-TPS	S652170	Connecting He	aders	MSP430F5529 LaunchPad				
Device Pin	Net Name	Pin Number	Header Number	Pin Number	Header Pin Info	Net and/or Device Pin Name		
18 (VIO) ⁽¹⁾	3V3LP	1	J1	1	+3V3	+3V3		
9	PWR_EN	2	J1	2	Analog In (A5)	P6.5		
N/A ⁽²⁾	BOOST_EN	8	J1	8	GPIO(!)	P2.7		
28	SCL	9	J1	9	I2C SCL	P4.2		
27	SDA	10	J1	10	I2C SDA	P4.1		
PAD	GND	20	J2	20	GND	GND		
12 ⁽³⁾	USBLP	21	J3	21	+5 V	+5 V		
PAD	GND	22	J3	22	GND	GND		
46	LDOPGOOD	39	J4	39	PWM Out	P2.4		

Table 1. Electrical Connections of Headers

⁽¹⁾ The net named 3V3LP is re-named 3V3SW after the current-limiting switch controlled by S1 and provides a pull-up reference voltage for SCL, SDA, INT, nWAKEUP, and LED D7 driven by the PGOOD pin of the TPS652170 device.

⁽²⁾ The BOOST_EN signal is for the TPS61093 and does not connect to the TPS652170. Enabling the boost provides 8 V to the PWR_EN pin, which is sufficiently high to allow re-programming of the EEPROM.

⁽³⁾ The net named USBLP is re-named USBSW after the current-limiting switch controlled by S1 and provides power (5 V) to the USB pin of the TPS652170 device directly from VBUS of the USB cable. USBSW is the only supply available and generates SYS, which provides power to all VIN_DCDCx pins, VINLDO, and LSx_IN.

2.2 Test Points

Table 2 lists the test points located on the BOOSTXL-TPS652170. The test points are required to measure the output voltage and sequence timing of the power rails generated by the TPS652170 device.

PCB Reference Designator	Net Name	Туре
TP1, TP2, TP3, TP4	GND, PAD (thermal pad)	Ground
TP5	PWR_EN	Digital input
TP6	LS2_OUT	Power output
TP7	LS1_OUT	Power output
TP8	VLDO2	Power output
TP9	SYS	Power output
TP10	VLDO2	Power output
TP11	VDCDC3	Power output (feedback input)
TP12	AC	Power input
TP13	USB	Power input
TP14	VDCDC1	Power output (feedback input)
TP15	VDCDC2	Power output (feedback input)
TP16	SCL	Digital input
TP17	SDA	Digital input/output

Table 2. BOOSTXL-TPS652170 Test Point List

2.3 Jumpers

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Table 3 lists and describes the jumper headers located on the BOOSTXL-TPS652170 for connecting or disconnecting nets of the PCB.

Table 3. BOOSTXL-TPS652170 Jumper List

PCB Reference Designator	Pin	Net Name	Default Shunt Connection	Description		
	1	DCDC1	-	Connect to pin 2 when LS1 is re- programmed as a load switch		
J5	2	LS1_IN	Installed	L S1 configurad as L DO2		
	3	SYS		LS1 configured as LDO3		
	1	SYS	Installed	LS2 configured on LDO4		
J6	2	LS2_IN		LS2 configured as LDO4		
	3	DCDC2	-	Connect to pin 2 when LS2 is reprogrammed as a load switch		

2.4 Software

The software to be used with the BOOSTXL-TPS652170 EVM is the IPG-UI. Download the following files to ensure that all of the required software is available on the computer used for testing:

- 1. The latest revision of the IPG-UI EVM GUI.
- 2. The latest revision of the TPS652170 IPG-UI device file (TPS652170-1.x.json) and script file (TPS652170-programming.js) from here.
- 3. The latest MSP430F5529 LaunchPad USB2ANY firmware (USB2ANY_2.7.0.0_LP.txt) from here.
- 4. The MSP430_USB_Firmware_Upgrade_Example-1.3.1.1-Setup.exe from the MSP430_USB_Developers_Package 5_20_06_02.

A detailed set of instructions for using the software, with examples, is provided in Appendix A.

2.5 Update MSP430F5529 Firmware

Update the MSP430F5529 LaunchPad development to the USB2ANY_2.7.0.0_LP.txt file before putting the BOOSTXL-TPS652170 on the LaunchPad development kit.

- 1. Press the S5 button while connecting the Micro USB cable.
- 2. Run the Firmware Upgrade Example.
- 3. Choose "Select Firmware".
- 4. Choose "Browse" and select the USB2ANY_2.7.0.0_LP.txt file downloaded previously.
- 5. Choose "Upgrade Firmware".
- 6. When complete, disconnect the USB cable.

3 EVM Operation

3.1 Power-On Procedure

Figure 4 shows the BOOSTXL-TPS652170 board with socket XU1 open and a TPS652170 samples installed correctly. After the socket is closed, the SW1 *PWR* switch can be moved from the *OFF* position to the *ON* position.

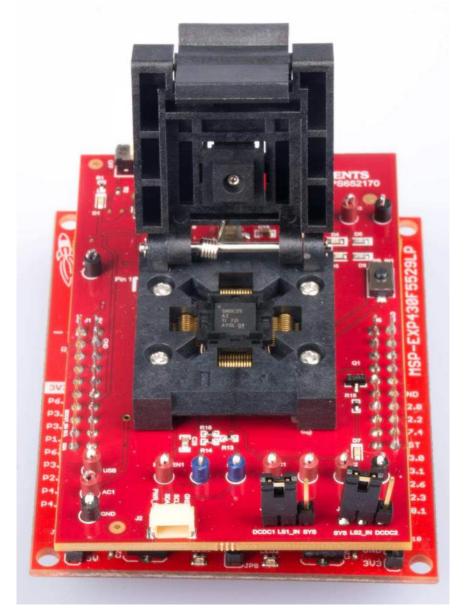


Figure 4. BOOSTXL-TPS652170 with Socket Open

In order for the configurable load switches/LDO regulators (LS1/LDO3, LS2/LDO4) to receive power from the correct source, shunts must be installed in the correct position on both 3-pin headers (J5 and J6) as described in Table 3.



Software Instructions

A.1 IPG-UI Software Installation

The following instructions explain how to install the IPG-UI software on a computer. If this software is already installed, this section may be skipped.

To install the IPG-UI software, first download the IPG-UI software installation package from www.ti.com. Then unzip and install the IPG-UI software tool onto the computer.

A.2 IPG-UI Setup for BOOSTXL-TPS652170

The following instructions explain how to run, setup, and operate the IPG-UI software on a computer and connect it to the BOOSTXL-TPS652170.

• Run the IPG-UI software by using the Windows *Start Menu* and navigating to the Texas Instruments folder, or by double-clicking the desktop icon, as shown in Figure 5.



Figure 5. Run the IPG-UI Software

- Wait for the program to load.
- Plug in the micro-USB cable to the USB port of the MSP430F5529 LaunchPad and connect the other end of the USB cable to an open USB2/3 port on the computer.
- Verify that the software is connected to the USB2ANY (MSP430F5529 LaunchPad) as shown in Figure 6.

🖬 IPGUI					1		×
		USB2ANY hardwe	are connected				
http://localhost.8100	Disconnect	Select USB2ANY Device USB2ANY/OneD	emo device F265806F0E002200 •	Hardware Connected .	49 TEXAS I	NSTRUM	ENTS

Figure 6. Successful Connection Between Computer and USB2ANY (MSP430F5529 LaunchPad)

• Click the drop-down menu in the *Create New Project* section and select *TPS652170-1.x* as shown in Figure 7.



Create New	Project			
Select Device		Select Device	• 3	Create Project from
Blank-I2C-7bit-1.0 V	3	Create Project		C:\Users\\\D UI\Devices\TPS65217
Blank-12C-7bit-1.0 TPS65020-1.0 TPS65023-1.0 TPS65055-1.0 TPS650860-1.1 TPS65090-1.0 TPS65217-1.2 TPS65217-1.3	or nation from File		or	
TPS652170-1.0 TPS65218-1.1 TPS65291-spi-1.1 TPS65910-1.0 TPS65911-1.1 TPS65912-1.1		Disconnect	Select USB2ANY Device	USB2ANY/OneDemo de

Figure 7. Creating New IPG-UI Project for the TPS652170

- Click the Create Project button.
 - **NOTE:** After a project is initially created, it is available in the *Create Projects from Recent Devices* menu. When a project is saved, it is available in the *Open Recent Projects* menu.
- The TPS652170 Introduction tab is now displayed, as shown in Figure 8. Click the Get Started button or the Register Map tab to begin communicating with TPS652170 device.



IPGUI - TPS652170	
File 🔻 GUI Settings	▼ Report ▼ About €
🗋 New Project 🛛 🕞 Ope	an Project 🐵 Save Project 🕲 Save As Project
Introduction	Introduction Download Datasheet
Register Map	
Single Register	TPS652170 is the programmable version of the TPS65217x test programming and this GUI shows additional registers that can be programmed or are required for re-programming the EEPROM of the device. The TPS65217x device is a single-chip Power Management IC specifically
Register Controls	designed to support applications in portable and 5V non-portable applications. It provides a linear battery charger for single-cell Li-lon and Li- Polymer batteries, dual-input power path, three step-down converters, four LDOs, and a high-efficiency boost converter to power two strings of
Device Controls	up to 10 LEDs each. The system can be supplied by any combination of USB port, 5V AC adapter, or Li-Ion battery. The device is characterized across a -40C to 105C temperature range which makes it suitable for industrial applications. Three high-efficiency 2.25 MHz step-down converters can provide the core voltage, memory, and I/O voltage for a system.
Adapter Controls	converters can provide the core voltage, memory, and i/O voltage for a system.
Macros	Get Started
Transaction History 🔺	Hardware Connected Changes Written

Figure 8. TPS652170 Project Introduction Tab in IPG-UI

• Click the *Read All* button and verify that data has changed in the **CHIPID** register from 0x00 to 0x02. Verify that no red notifications appear in the upper left corner of the IPG-UI window. Blue notifications are informational only and do not indicate an error has occurred. Figure 9.



IPGUI - TPS652170															
File 🔻 GUI Settings 🔻	Report 👻														
🗅 New Project 🛛 🕞 Open	Project 🖺 Save Project	🖺 Save	As	Pr	oje	ct									
Introduction	Read ALL Write A	LL Updat		lac		Mar				ĩo	Autoread	0# -			
Register Map	Configuration Regis		stR		-		lua		0.28		Lutoreau	Un ,			
Single Register	I2C Address 0x24 V	Read G					Gr		0	0-	Jaco Dec Car	100000	1		
Register Controls	IZC Address 0x24	Read G	out		VV		ts	oup		Un	der By ad	aress	<u>.</u>	Auto	Pead
Device Controls	Register Name	Address	7	6	5			2	1	0	Value	w	R	10	s
Adapter Controls	★ CHIPID	0x00	0	0	0	0	0	0	1	0	02		R		
Viacros	★ PPATH	0x01	0	0	1	1	1	1	1	1	3F	w	R		
	★ INT	0x02	0	0	0	0	0	0	0	0	00	w	R		
	★ CHGCONFIG0	0x03	0	0	0	0	0	0	0	1	01		R		
	* CHGCONFIG1	0x04	1	0	1	0	0	0	0	1	A1	w	R		
	★ CHGCONFIG2	0x05	1	0	1	0	0	1	0	1	A5	w	R		
	★ CHGCONFIG3	0x06	1	1	1	1	0	1	1	0	F6	w	R		
	* WLEDCTRL1	0x07	0	0	0	0	0	0	0	1	01	w	R		
	* WLEDCTRL2	0x08	0	0	0	0	0	0	0	0	00	w	R		
	# MUXCTRL	0x09	0	0	0	0	0	0	0	0	00	w	R		
	* STATUS	0x0A	1	0	0	0	0	1	0	0	84	w	R		

Figure 9. Successful Write Access to TPS652170 Notification

If all register data remains 0x00 and a red notification appears (as in Figure 10), it indicates the computer can talk to the USB2ANY (MSP430F5529 LaunchPad) but cannot communicate with the TPS652170 device. The primary cause of this issue may be that the power switch for the BOOSTXL-TPS652170 is in the *OFF* position, the socket does not have a sample installed, or the USB cable is not plugged into the MSP430F5529 LaunchPad or the computer. In case of either issue, the test setup of the EVM must be debugged before continuing.



Read ALL Write A	LL Updat	te N	۸od	eN	Aanu	ıal	,	•	Autoread	Off ▼				Cannot read property 'registers' of undefined
Configuration Regis	ters Te Read G	0.000	Regi		rs rite (Grou	P	Or	der By ac	ldress	•			USB2ANY Failure: -49 ERR_J2C_WRITE_TIMEOUT
Register Name	Address	7	6	5	Bits		1	0	Value	w	R	AutoF 10	Read s	
	0x00	0	0	0	0	0 0	0	0	00		R			
🚖 PPATH	0x01	0	0	0	0	0	0	0	00	w	R			
★ INT	0x02	0	0	0	0	0 0	0	0	00	w	R			

Figure 10. Failed GUI Communication to TPS652170 Notification

NOTE: At the time of writing this document, the IPG-UI software version is 2.5.0.5 and the TPS652170 file version is 1.0.

A.3 Testing TPS652170 DCDC1 Voltage Change with IPG-UI

This section provides an example of how to use the IPG-UI software to read registers and modify the voltage of a single DC/DC converter of the TPS652170 device.

• Start by navigating to the *Device Controls* tab of the IPG-UI and verify that the Auto Password feature is Enabled, as shown in Figure 11.

Introduction	PASSWORD PROGRAM
Register Map	
Single Register	Auto Password
Register Controls	When enabled writes to the password protected registers will first have a pre-write to the password register performed to unlock the register for write
Device Controls	access

Figure 11. Auto Password Write Enabled

• Navigate back to the *Register Map* tab, click on the row for the **DEFDCDC1** register (0x0E), and read the value of this register by clicking the button labeled *R* in this row of the register map table, as shown in Figure 12.

★ DEFDCDC1	0x0E	0	0	0	1	0	0	1	0	12	W	R	DCDC	21	RW
* DEFDCDC2	0x0F	0	0	0	0	1	0	0	0	08	w	R		1.350 V	-
★ DEFDCDC3	0x10	0	0	0	0	0	0	1	0	02	w	R	This g	group represents the DCDC1 output vo	tage.

Figure 12. DEFDCDC1 Register, Default Value

• Click on the row for the **DEFSLEW** register (0x11) and change the value of bit 6 in the from 0b to 1b by clicking the bit's cell in the table or clicking the radio button labeled *Disabled* on the right-hand side of the window. Write the new value of this register by clicking the button labeled *W* in this row of the register map table, as shown in Figure 13.



Testing TPS652170 DCDC1 Voltage Change with IPG-UI

r DEFSLEW	0x11	0	1	0	0	0 1	1	0	46 1	V R		GODSBL R W
E DEFLDO1	0x12	0	0	0	0	1 0	0	1	09	V R	0	 Enabled Disabled. DCDCX output voltage changes
EFLD02	0x13	0	0	1	1	1 0	0	0	38 V	V R		whenever set-point is updated in DEFDCDCX register without having to write to the GO bit
R DEFLS1	0x14	0	0	1	0	0 1	1	0	26 V	R		This group represents the GO bit disable
DEFLS2	0x15	0	0	1	1	1 1	1	1	3F V	R		PFM_EN1
	0x16	n	1	1	1	1 1	1	1	7F V	V R		 DCDC converter operates in PWM/PFM mode depending on load
R ENABLE	UXTO											
r ENABLE Data: 31 Seq: 141 🔺	-	9								Hardware C	onnected	Changes not Written • 49 Texas Instrume
	-		1	0	0	0 1	1	0	46		onnected •	GODSBL RW
Data: 31 Seq: 141 🔺		0	97	999	99 - 1	0 1	1		46 V 09 V	/ R		GODSBL R W © Enabled © Disabled. DCDCX output voltage changes
Data: 31 Seq: 141 🔺	0x11	0	0	0	0		0	1		/ R / R	0	GODSBL RW
Data: 31 Seq: 141 A DEFSLEW DEFLD01	0x11 0x12	0	0	0	0	1 0	0	1	09	/ R / R / R		GODSBL R W C Enabled Disabled. DCDCX output voltage changes whenever set-point is updated in DEFDCDCX
Data: 31 Seq: 141 DEFSLEW DEFLD01 DEFLD02	0x11 0x12 0x13	0	0	0 1 1	0 1 0	1 0 1 0	0	1 0 0	09 V 38 V	/ R / R / R	0	GODSBL R W Enabled Disabled. DCDCX output voltage changes whenever set-point is updated in DEFDCDCX register without having to write to the GO bit

Figure 13. Disable GO Bit in SLEW Register

• Click on the row for the **DEFDCDC1** register (0x0E) again, and this time move the slider on the righthand side of the window to change the output voltage of DCDC1 to a new value. Write the new value of this register by clicking the button labeled *W* in this row of the register map table, as shown in Figure 14. The value in the **PASSWORD** register (0x10) will also change because the IPG-UI is automatically writing the correct password to this register in advance so that the DCDC1 register will accept the new data.

2C Address 0x24 🔻	Read Gr	oup		Wri	te (Gro	up	C)rder	By address ▼		DEFDCDC1 This register contains the DCDC1 control settings
PASSWORD	0x0B	0	1	1	1	0	0	1	1 [3 W R		XADJ1 R W
🛊 PGOOD	0x0C	0	1	1	1	1	1	1	1	FR		Output voltage is adjusted through register
🛊 DEFPG	0x0D	0	0	0	0	1	1	0	0	C W R		setting O Output voltage is externally adjusted
DEFDCDC1	0x0E	0	0	0	1	0	1	0	1	5 W R	6	This group represents the DCDC1 voltage adjustmer option
DEFDCDC2	0x0F	0	0	0	0	1	0	0	0	8 W R		DCDC1 R W
DEFDCDC3	0x10	0	0	0	0	0	0	1	0	2 W R		
# DEFSLEW	0x11	0	0	0	0	0	1	1	0 [6 W R		- 1.425 V -
★ DEFLD01	0x12	0	0	0	0	1	0	0	1	9 W R		This group represents the DCDC1 output voltage

Figure 14. Modifying DEFDCDC1 Register Value

• Verify the new voltage setting by measuring the DCDC1 test point (TP14) on the BOOSTXL-



TPS652170 board with a multi-meter.

A.4 Re-Programming the EEPROM of the TPS652170 Device

This section provides an example of how to re-write the EEPROM of the TPS652170 device using the IPG-UI and visually verify that the new values have been correctly programmed into the non-volatile EEPROM memory of the device. The most commonly programmed values, DC/DC converter output voltage and sequencing order, will be modified in this example.

- **NOTE:** All of the bits that are backed by EEPROM and are programmable are highlighted in red in the Register Map section of the IPG-UI software for the TPS652170 device. Bits that are grayed out are Reserved and are Read-Only. The bits with no color-coding are Read-Write capable and can be edited in real-time, but this memory is volatile and the values will not be stored when the TPS652170 device is power-cycled.
- Figure 15 and Figure 16 show all of the available EEPROM-backed registers of the TPS652170 that may be programmed.



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Introduction	Read ALL Write ALL	Undata	v.	أما						A.,	torood Of				
Register Map					10000		11			Au					
Single Register	Configuration Registe		_	-							-				
Register Controls	I2C Address 0x24 V	Read Grou	P	V	Vinte			P	O	rdei	r By addre	ss 🔻		AutoE	Dood
Device Controls	Register Name	Address	7	6	5			2	1	0	Value	w	R	10	s
Adapter Controls	* CHIPID	0x00	0	0	0	0	0	0	1	0	02		R		
Macros	★ PPATH	0x01	0	ode Manual Autoread Off agisters Write Group Order By address Bits AutoRead 6 5 4 3 2 1 0 Value W R 10 s											
	★ INT	0x02	0	0	0	0	0	0	ö	0	00	w	R		
	CHGCONFIG0	0x03	0	0	0	0	0	0	0	1	01		R		
	CHGCONFIG1	0x04	1	0	1	1	0	0	0	1	B1	w	R		
	* CHGCONFIG2	0x05	1	0	0	0	0	0	0	0	80	w	R		
	★ CHGCONFIG3	0x06	1	0	1	1	0	0	1	0	B2	w	R		
	* WLEDCTRL1	0x07	0	0	0	0	0	0	0	1	01	W	R		
	* WLEDCTRL2	0x08	0	0	0	0	0	0	0	0	00	W	R		
	# MUXCTRL	0x09	0	0	0	0	0	0	0	0	00	w	R		
	★ STATUS	0x0A	0	0	0	Ő	0	1	Ö	0	04	W	R		
	+ PASSWORD	0x0B	0	0	0	0	0	0	0	0	00	w	R		

Figure 15. EEPROM-Backed Registers of the TPS652170 (1 of 2)

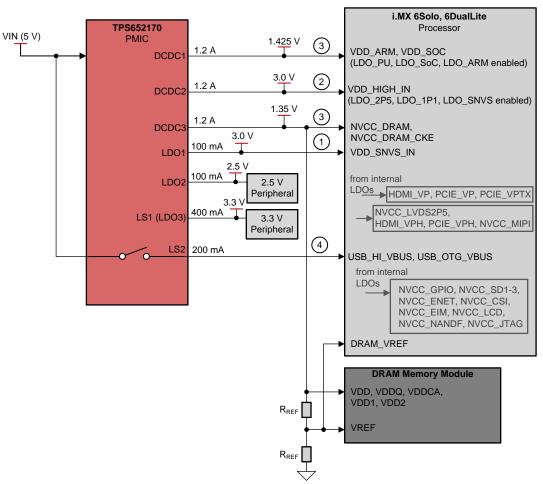
Re-Programming the EEPROM of the TPS652170 Device

★ PGOOD	0x0C	0	3	1	1	1	1	3	1	7F	R
★ DEFPG	0x0D	0	0	0	0	1	1	0	0	0C W	R
★ DEFDCDC1	0x0E	0	0	0	1	0	0	1	0	12 W	R
★ DEFDCDC2	0x0F	0	0	0	0	1	0	0	0	08 W	R
★ DEFDCDC3	0x10	0	0	0	0	1	0	0	0	08 W	R
★ DEFSLEW	0x11	0	0	0	0	0	1	1	0	06 W	R
★ DEFLDO1	0x12	0	0	0	Ö	1	0	0	1	09 W	R
★ DEFLDO2	0x13	0	0	1	1	1	0	0	0	38 W	R
★ DEFLS1	0x14	0	0	1	0	0	1	1	0	26 W	R
★ DEFLS2	0x15	0	0	1	1	1	1	1	1	3F W	R
★ ENABLE	0x16	0	1	1	1	1	1	1	1	7F W	R
★ DEFUVLO	0x18	0	0	0	0	0	0	0	0	00 W	R
★ SEQ1	0x19	0	0	0	1	0	1	0	1	15 W	R
★ SEQ2	0x1A	0	1	0	1	1	1	1	1	5F W	R
★ SEQ3	0x1B	0	0	1	1	0	0	1	0	32 W	R
★ SEQ4	0x1C	0	1	0	0	0	0	0	0	40 W	R
★ SEQ5	0x1D	0	0	1	0	0	0	0	0	20 W	R
* SEQ6	0x1E	0	0	0	0	0	0	0	0	00 W	R

Figure 16. EEPROM-Backed Registers of the TPS652170 (2 of 2)

• For this example, the TPS652170 will be re-programmed from its original settings to provide power to the processor shown in Figure 17.





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(1) The power-on sequence order is listed for each rail, numbered 1-4.

Figure 17. TPS652170 Re-Programming Example Block Diagram

 The voltage setpoint of DCDC1 has already been modified, so only the remaining DC/DC converters and LDO1 regulator voltages need to be modified at this time. Figure 18 shows the new output voltage setpoint configured in the DEFDCDC2, DEFDCDC3, DEFLDO1, DEFLDO1, DEFLS1, and DEFLS2 registers (0x0F, 0x10, 0x12, 0x13, 0x14, and 0x15) as well as the correct PASSWORD register (0x10) value written automatically by the IPG-UI.

* PASSWORD	0x0B	0 1	1	1 0	0	1	0 72	w	R		
* DEFDCDC2	0x0F	0 0	1	1 0	1	0	1 35	w	R	D	DCDC2 R W
★ DEFDCDC3	0x10	0 0	0	1 0	0	1	0 12	w	R		3.000 V F
* DEFSLEW	0x11	0 1	0	0 0	1	1	0 46	W	R		This group represents the DCDC2 output voltage
* PASSWORD	0x0B	0 1	1 (01	1	0	1 6D	w	R		
★ DEFDCDC1	0x0E	0 0	0	1 0	1	0	1 15	w	R		DCDC3
★ DEFDCDC2	0x0F	0 0	1	1 0	1	0	1 35	W	R		- 1.350 V +
★ DEFDCDC3	0x10	0 0	0	1 0	0	1	0 12	w	R		This group represents the DCDC3 output voltage
* PASSWORD	0x0B	0 1	1	01	1	1	1 6F	w	R		
* DEFLD01	0x12	0 0	0 0	1	1	0	1 0D	w	R		LD01 R W
★ DEFLD02	0x13	0 0	1 1	1 1	0	0	0 38	w	R		- 3.00 V +
★ DEFLS1	0x14	0 0	1 (0 0	1	1	0 26	w	R		This group represents the LDO1 output voltage settings
* PASSWORD	0x0B	0 1	1	0 1	1	1	0 6E	W	R		
★ DEFLDO2	0x13	0 0	1	0 1	1	0	0 2C	w	R		LDO2 R W
★ DEFLS1	0x14	0 0	1	0 0	1	1	0 26	w	R		- 2.500 V +
★ DEFLS2	0x15	0 0	1	1 1	1	1	1 3F	w	R		This group represents the LD02 output voltage
★ PASSWORD	0x0B	0 1	1	0 1	0	0	1 69	W	R		

Figure 18. Modifying DCDC2-3, LDOx, and LSx Register Values

- **NOTE:** Extreme changes in output voltage settings for DCDC1-3 and LDO1-4 may not settle to the desired voltage before the TPS652170 supervisor circuitry recognizes the voltage as an undervoltage fault condition and performs a system reset. This will reset the DCDC1-3 and LDO1-4 registers to the value currently stored in EEPROM and is desirable in the end application, but it will prevent successful re-programming with new output voltage settings. If this issue is observed while modifying registers prior to re-programming the EEPROM, then a value of 0x00 must be written to the **ENABLE** register (0x16) before re-starting this procedure.
- To match the example, the order in which the DC/DC converters and LDO turn on and turn off is must be changed. This order, or sequencing, is changed by modifying the SEQ1, SEQ2, and SEQ3 registers (0x19, 0x1A, and 0x1B), as shown in Figure 19. The SEQ4 register (0x1C) controls the sequence order of LS2/LDO4 but this register does not need to be changed for this example.



Re-Programming the EEPROM of the TPS652170 Device

Configuration Regi	isters Te	st R	egis	ster	s						
2C Address 0x24	Read Gr	oup		Wri	ite (Grou	ф	0	rder By address		SEQ1
* DEFUVLO	0x18	0	0	0	0	0	0	0	0 00 W	R	This register contains sequencer settings
★ SEQ1	0x19	0	0	1	1	0	0	1	0 32 W	R	DC1_SEQ R V
🗙 SEQ2	0x1A	0	0	1	1	1	1	1	1 3F 🛛 🖤	R	This group represents the DCDC1 sequencer strobe
★ SEQ3	0x1B	0	0	0	0	0	0	0	0 00 W	R	setting
★ SEQ4	0x1C	0	1	0	0	0	0	0	0 40 W	R	DC2_SEQ
* SEQ5	0x1D	0	0	1	0	0	0	0	0 20 W	R	enable at STROBE2
* SEQ6	0x1E	0	0	0	0	0	0	0	0 00 W	R	This group represents the DCDC2 sequencer strobe setting
SEQ2			22				1000	EQ			SEQ4
This register contains s	equencer set	tings	3	R	M	,1			egister contains sec	iencer settings	This register contains sequencer settings
enable at STROBE3			-						is not controlled by s		enable at STROBE4
This group represents setting	the DCDC3 se	quei	ncer	str	obe			'his ettii		LD02 sequencer strob	This group represents the LDO4 sequencer strobe setting
LD01_SEQ			1	R	V	/	L	DO:	3_SEQ	R	w
enable at STROBE15		1					16	Rail	is not controlled by s	quencer V	

Figure 19. Modifying Sequence (SEQ3-4, SEQ6) Registers

To re-program the EEPROM of the TPS652170 device and make these changes permanent, a special bit named EE_PROG_BIT must be set to 1b in the TEST_EEP_ADDR register (0x2C). This register and other special registers can be found in the *Test Registers* tab of the GUI. Figure 20 shows how to enter programming mode manually and Figure 21 shows how to use the IPG-UI to automatically reprogram the EEPROM memory of the TPS652170 device. When the programming mode is entered manually, the EE_PROG_BIT must be reset to 0b to exit programming mode.



I2C Address 0x24 ▼	Read Grou	p	V	Vrite	e G	rou	p	0	rde	r By addre	ss 🔻				TEST_EEP_ADDR
					В	its					2		Auto	Read	This register contains EEP
Register Name	Address	7	б	5	4	3	2	1	0	Value	W	R	10	S	EE_PROG_BIT
TEST_EEP_ADDR	0x2C	0	0	0	1	0	0	0	0	10	w	R		9	Enabled
★ EE_LS1_ADDR	0x49	0	0	0	1	1	0	0	0	18	w	R		0	Enabling this bit allows the EEPROM memory
★ EE_LS2_ADDR	0x4A	0	0	0	1	1	0	0	0	18	W	R			
★ EE_CHARGER1	0x4B	0	0	1	1	0	0	ö	1	31	w	R		0	

Figure 20. Manually Writing EE_PROG_BIT to Re-Program EEPROM

💋 IPGUI - TPS652170		<u>14.4</u> 7		×
File 🔻 GUI Settings 🔻	Report -		About	6
🗋 New Project 🛛 🗁 Open F	Project 🖺 Save Project 🖺 Save As Project			
Introduction	PASSWORD PROGRAM	EEPROM Programming started		*
Register Map				
Single Register	Re-program EEPROM	EEPROM Programming finished		*
Register Controls	Start This control will program the EEPROM with a custom sequence. Make sure that you have provided 8V to the P	OWER_EN pin		
Device Controls				1

Figure 21. Automatically Writing EE_PROG_BIT to Re-Program EEPROM

Now the BOOSTXL-TPS652170 board can be reset by moving SW1 (labeled *PWR*) to the *OFF* position and then moving it back to the *ON* position. Click *Read All* on the IPG-UI to verify that all of the registers programmed into the EEPROM has been re-programmed correctly. Figure 22 and Figure 23 show all of the registers that have been re-programmed in this example, as well as the volatile bits that have changed after power cycling the TPS652170 device.



Configuration Registe	Test	Reg	jist	ers										
2C Address 0x24 🔻	Read Grou	p	v	Vrite	e G	rou	P	Or	der	Byaddres	ss 🔻			
					Bi	its							AutoF	Read
Register Name	Address	7	б	5	4	3	2	1	0	Value	W	R	10	s
★ CHIPID	0x00	0	0	0	0	0	0	1	0	02		R		6
* PPATH	0x01	0	0	1	1	1	1	0	1	3D	w	R		0
★ INT	0x02	0	0	0	0	0	0	0	0	00	W	R		0
* CHGCONFIG0	0x03	0	0	0	0	0	0	0	1	01		R		8
* CHGCONFIG1	0x04	1	0	1	1	0	0	0	1	B1	W	R		0
CHGCONFIG2	0x05	1	0	0	0	0	0	0	0	80	w	R		C
* CHGCONFIG3	0x06	1	0	1	1	0	0	1	0	B2	W	R		C
* WLEDCTRL1	0x07	0	0	0	0	0	0	0	1	01	w	R		5
WLEDCTRL2	0x08	0	0	0	0	0	0	0	0	00	w	R		6
MUXCTRL	0x09	0	0	0	0	0	0	0	0	00	W	R		6
🖈 STATUS	0x0A	0	0	0	0	0	1	0	0	04	W	R		G
* PASSWORD	0x0B	0	0	0	0	0	0	0	0	00	W	R		2

Figure 22. Registers After Successful Re-Programming (1 of 2)



★ PGOOD	0x0C	0	0	1	1	1	1	1	0	3E	R	
★ DEFPG	0x0D	0	0	0	0	1	1	0	0	0C W	R	
* DEFDCDC1	0x0E	0	0	0	1	0	1	0	0	[14] W	R	C
* DEFDCDC2	0x0F	0	0	1	1	0	1	0	0	34 W	R	6
* DEFDCDC3	0x10	0	0	0	1	0	0	1	0	12 W	R	6
* DEFSLEW	0x11	0	0	0	0	0	1	1	0	06 W	R	
★ DEFLDO1	0x12	0	0	0	0	1	1	0	1	0D W	R	6
★ DEFLDO2	0x13	0	0	1	0	1	1	0	0	2C W	R	2
★ DEFLS1	0x14	0	0	1	1	1	1	1	1	3F W	R	C
★ DEFLS2	0x15	0	Ö	0	1	1	1	1	1	1F W	R	0
🛊 ENABLE	0x16	0	0	1	1	1	1	1	0	3E W	R	Ę
# DEFUVLO	0x18	0	0	0	0	0	0	0	0	00 W	R	6
★ SEQ1	0x19	0	0	1	1	0	0	1	0	32 W	R	0
🛊 SEQ2	0x1A	0	0	1	1	1	1	1	1	3F W	R	6
🛊 SEQ3	0x1B	0	0	0	0	0	0	0	0	00 W	R	6
★ SEQ4	0x1C	0	1	0	0	0	0	0	0	40 W	R	6
★ SEQ5	0x1D	0	0	1	0	0	0	0	0	20 W	R	0
★ SEQ6	0x1E	0	0	0	0	0	0	0	0	00 W	R	0

Figure 23. Registers After Successful Re-Programming (2 of 2)

NOTE: If the voltage on the PWR_EN pin of the TPS652170 is less than to 7 V, this is too low for re-programming the EEPROM.



Re-Programming the EEPROM of the TPS652170 Device

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The EEPROM re-programming was successful because the IPG-UI remembers the previous value of bits before the *Read All* button is pressed and highlights changes in blue. There are some bits highlighted in blue in Figure 22 and Figure 23, but these differences do not indicate a failed EEPROM re-programming. The **PGOOD** and **ENABLE** registers (0x0C and 0x16) are both 0x3E now because LDO2 and LDO3 have been disabled from the sequencer. The least significant bit (LSB), bit 0, of the **DEFDCDC1** and **DEFDCDC2** registers (0x0E and 0x0F) is set to 0b now and the output of these DC/DC converters will be 25 mV lower than expected, but this volatile bit can be set to 1b again in real-time by I²C. and LDO1 have been enabled. Bit 6 of the **DEFSLEW** register (0x11) has reset to 0b because the **GODSBL** bit is not backed by EEPROM. None of the EEPROM-backed bits (highlighted in red) that were changed in the example re-programming have been highlighted in blue.

The successful re-programming of the EEPROM can also be verified on the BOOSTXL-TPS652170 hardware by measuring the output voltages of DCDC1, DCDC2, DCDC3, LDO1, LDO2, LS1 (LDO3) and LS2 with a multi-meter and by measuring the power-on sequence timing with an oscilloscope.

CAUTION

The BOOSTXL-TPS652170 board is intended for re-programming the EEPROM of the TPS652170 only. Significant loads should not be applied to the DC/DC converters, LDOs regulator, or load switches using the BOOSTXL-TPS652170 test points. The newly re-programmed TPS652170 device must be removed from the socket and soldered down onto a TPS65217xEVM board or another board designed to carry the current for maximum loads to evaluate the full performance of the TPS652170 device.



Appendix B SLVUBH6–November 2018

EVM Documentation

B.1 Layout

Figure 24 through Figure 31 show the board layout for the BOOSTXL-TPS652170

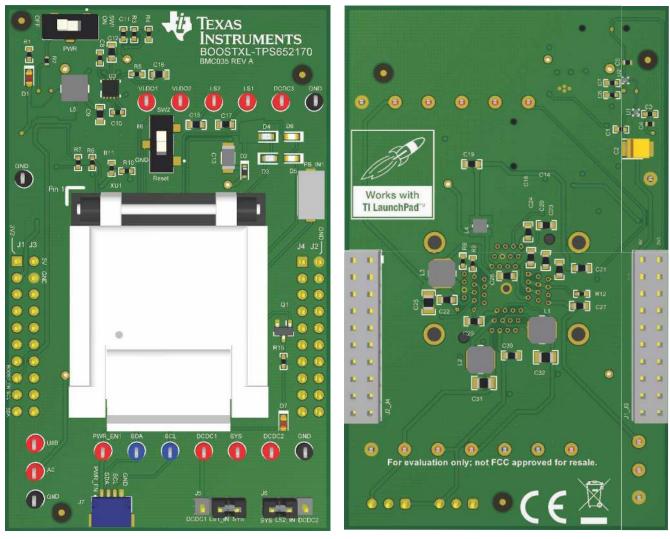


Figure 24. Component Placement—Top Assembly

Figure 25. Component Placement—Bottom Assembly



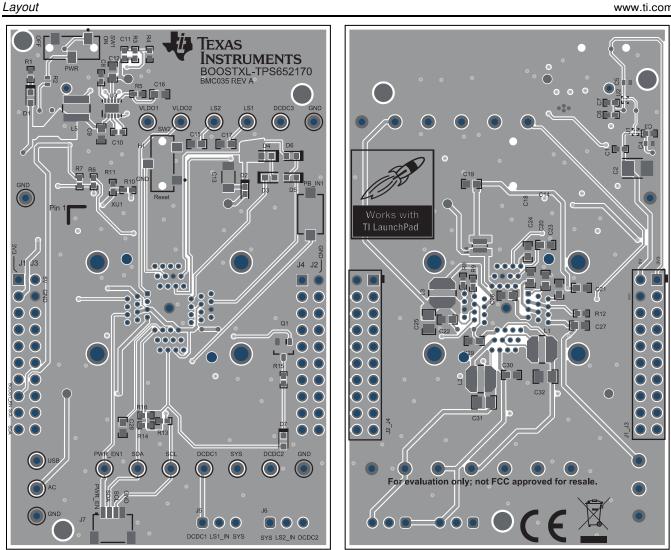


Figure 26. Layout—Top Composite

Figure 27. Layout—Bottom Composite





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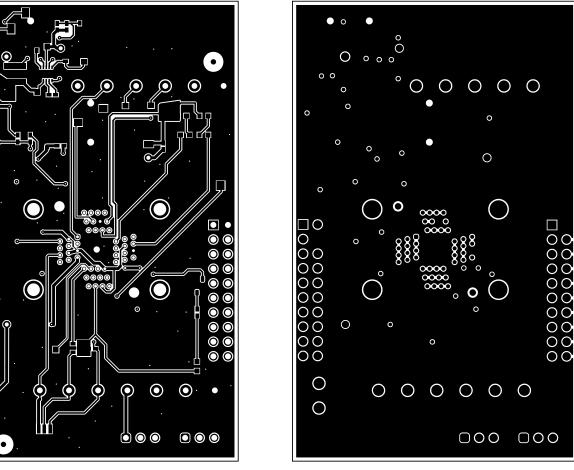


Figure 28. Top Layer

Figure 29. Inner Layer 1 (GND Plane)



Layout

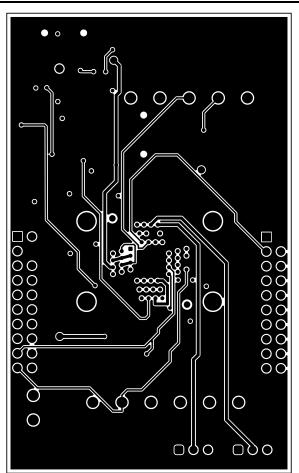


Figure 30. Inner Layer 2 (Signal)

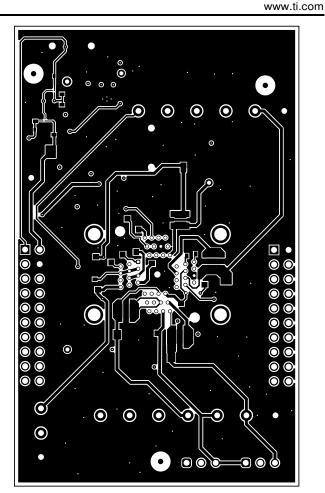
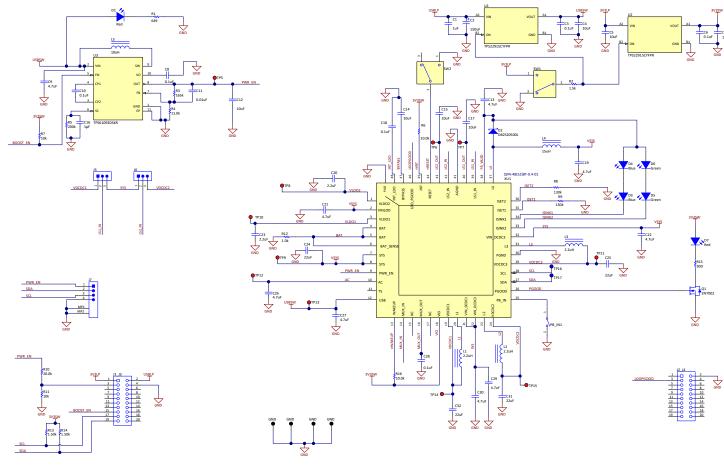


Figure 31. Bottom Layer (Top View)



B.2 Schematic

Figure 32 shows the schematic for BOOSTXL-TPS652170.



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Figure 32. BOOSTXL-TPS652170 Schematic



B.3 Bill of Materials

Table 4 provides the bill of materials (BOM) for the BOOSTXL-TPS652170.

Table 4. Bill of Materials

Designator	Quantity	Value	Description	PackageRefere nce	PartNumber	Manufacturer
C1, C7	2	1 uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X5R, 0402	0402	C1005X5R1E10 5K050BC	ТDК
C2	1	150 uF	CAP, TA, 150 uF, 6.3 V, +/- 20%, 0.07 ohm, SMD	3528-21	T520B157M006 ATE070	Kemet
C3, C6, C8, C10	4	0.1 uF	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X5R, 0402	0402	C1005X5R1A10 4K050BA	ТDК
C4, C5	2	10 uF	CAP, CERM, 10 uF, 10 V, +/- 20%, X5R, 0402	0402	CL05A106MP5N UNC	Samsung Electro- Mechanics
C9, C19, C21, C22, C26, C27, C29, C30	8	4.7 uF	CAP, CERM, 4.7 uF, 35 V, +/- 10%, X5R, 0603	0603	C1608X5R1V47 5K080AC	TDK
C11	1	0.01 uF	CAP, CERM, 0.01 uF, 50 V, +/- 5%, X7R, 0402	0402	C0402C103J5R ACTU	Kemet
C12, C14, C15, C17	4	10 uF	CAP, CERM, 10 uF, 16 V, +/- 20%, X5R, 0603	0603	GRM188R61C10 6MAALD	MuRata
C13	1	4.7 uF	CAP, CERM, 4.7 uF, 50 V, +/- 10%, X7R, 1206_190	1206_190	UMK316AB7475 KL-T	Taiyo Yuden
C16	1	1 uF	CAP, CERM, 1 μF, 16 V,+/- 10%, X7R, AEC- Q200 Grade 1, 0603	0603	CGA3E1X7R1C 105K080AC	TDK
C18, C28	2	0.1 uF	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0603	0603	C1608X7R1E10 4K080AA	TDK
C20, C23	2	2.2 uF	CAP, CERM, 2.2 uF, 16 V,+/- 10%, X7R, 0603	0603	EMK107BB7225 MA-T	Taiyo Yuden
C24	1	22 uF	CAP, CERM, 22 uF, 10 V, +/- 20%, X5R, 0603	0603	C1608X5R1A22 6M080AC	TDK
C25, C31, C32	3	22 uF	CAP, CERM, 22 uF, 10 V, +/- 20%, X5R, 0805	0805	CL21A226MPCL RNC	Samsung Electro- Mechanics
D1, D7	2	Red	LED, Red, SMD	LED, 1.6 x .8 x .8 mm	SML-311UTT86	Rohm
D2	1	15 V	Diode, Schottky, 15 V, 0.2 A, SOD-523	SOD-523	DB2S20500L	Panasonic
D3, D4	2	Blue	LED, Blue, SMD	1.6 x 0.8 mm	LTST- C193TBKT-5A	Lite-On
D5, D6	2	Green	LED, Green, SMD	1.6 x 0.8 mm	LNJ337W83RA	Panasonic
J1_J3, J2_J4	2		Receptacle, 2.54 mm, 10 x 2, Gold, TH	Receptacle, 2.54 mm, 10 x 2, TH	SSW-110-02-G- D	Samtec



Table 4. Bill of Materials	(continued)
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			. Dill of Materials	,	1	
Designator	Quantity	Value	Description	PackageRefere nce	PartNumber	Manufacturer
J5, J6	2		Header, 2.54 mm, 3 x 1, Gold, TH	Header, 2.54 mm, 3 x 1, TH	TSW-103-08-G- S	Samtec
J7	1		Header (Shrouded), 1 mm, 4x1, Tin, R/A, SMT	Header (Shrouded), 1 mm, 4 x 1, R/A, SMT	SM04B-SRSS- TB(LF)(SN)	JST Manufacturing
L1, L2, L3	3	2.2 uH	Inductor, Shielded, Ferrite, 2.2 uH, 1.44 A, 0.06 ohm, SMD	4.0 x 1.8 x 4.0 mm	VLCF4018T- 2R2N1R4-2	TDK
L4	1	15 uH	Inductor, Shielded, Ferrite, 15 uH, 0.4 A, 1.062 ohm, SMD	Inductor, 2 x 1.2 x 2 mm	VLS2012ET- 150M	TDK
L5	1	10 uH	Inductor, Shielded, Ferrite, 10 uH, 1.3 A, 0.17 ohm, SMD	SMD, 3.8 x 3.8 mm	IFSC1515AHER 100M01	Vishay-Dale
PB_IN1	1		Switch, Tactile, SPST, 12 V, SMD	SMD, 6 x 3.9 mm	434121025816	Wurth Elektronik
Q1	1	60 V	MOSFET, N-CH, 60 V, 115 A, SOT-23	SOT-23	2N7002	Fairchild Semiconductor
R1	1	649	RES, 649, 1%, 0.063 W, AEC- Q200 Grade 0, 0402	0402	CRCW0402649 RFKED	Vishay-Dale
R2	1	1.5 k	RES, 1.5 k, 5%, 0.063 W, AEC- Q200 Grade 0, 0402	0402	CRCW04021K50 JNED	Vishay-Dale
R3	1	165 k	RES, 165 k, 1%, 0.063 W, AEC- Q200 Grade 0, 0402	0402	CRCW0402165K FKED	Vishay-Dale
R4	1	11.0 k	RES, 11.0 k, 1%, 0.063 W, AEC- Q200 Grade 0, 0402	0402	CRCW040211K0 FKED	Vishay-Dale
R5	1	200 k	RES, 200 k, 1%, 0.063 W, AEC- Q200 Grade 0, 0402	0402	CRCW0402200K FKED	Vishay-Dale
R6, R16	2	10.0 k	RES, 10.0 k, 1%, 0.063 W, AEC- Q200 Grade 0, 0402	0402	CRCW040210K0 FKED	Vishay-Dale
R7, R11	2	10 k	RES, 10 k, 5%, 0.063 W, AEC- Q200 Grade 0, 0402	0402	CRCW040210K0 JNED	Vishay-Dale
R8, R9	2	130 k	RES, 130 k, 5%, 0.063 W, AEC- Q200 Grade 0, 0402	0402	CRCW0402130K JNED	Vishay-Dale
R10	1	20.0 k	RES, 20.0 k, 1%, 0.063 W, AEC- Q200 Grade 0, 0402	0402	CRCW040220K0 FKED	Vishay-Dale



Bill of Materials

Table 4. Bill of Materials (continued)

Designator	Quantity	Value	Description	PackageRefere nce	PartNumber	Manufacturer
R12	1	1.0 k	RES, 1.0 k, 5%, 0.063 W, AEC- Q200 Grade 0, 0402	0402	CRCW04021K00 JNED	Vishay-Dale
R13, R14	2	1.50 k	RES, 1.50 k, 1%, 0.063 W, AEC- Q200 Grade 0, 0402	0402	CRCW04021K50 FKED	Vishay-Dale
R15	1	300	RES, 300, 5%, 0.063 W, AEC- Q200 Grade 0, 0402	0402	CRCW0402300 RJNED	Vishay-Dale
SH-J1, SH-J2	2		Shunt, 2.54 mm, Gold, Black	Shunt, 2.54 mm, Black	60900213421	Wurth Elektronik
SW1	1		Switch, Slide, SPDT, 0.2 A, J Lead, SMD	SMD, 3-Leads, Body 8.5 x 3.5 mm, Pitch 2.5 mm	CL-SB-12A-01T	Copal Electronics
SW2	1		Switch, Slide, SPDT, 0.2 A, GULL, 12 V, SMD	SMD, 3-Leads, Body 8.5 x 3.5 mm, Pitch 2.5 mm	CL-SB-12B-01T	Copal Electronics
TP1, TP2, TP3, TP4	4		Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15	11		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP16, TP17	2		Test Point, Miniature, Blue, TH	Blue Miniature Testpoint	5117	Keystone
U1, U2	2		5.5 V, 2 A, 38 m Ω Load Switch With Quick Output Discharge, YFP0004AAAA (DSBGA-4)	YFP0004AAAA	TPS22915CYFP R	Texas Instruments
U3	1		Low Input, 20 V / 1.1 A Step-Up DC/DC Converter with Integrated Power Diode and Input/Output Isolation, DSK0010A (WSON-10)	DSK0010A	TPS61093DSKR	Texas Instruments
XU1	1		Socket, QFN-48, 0.4 mm Pitch	Socket, QFN-48, 0.4 mm Pitch	QFN-48(52)BT- 0.4-01	Enplas Tech Solutions
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A

STANDARD TERMS FOR EVALUATION MODULES

- 1. Delivery: TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
 - 1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software
 - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
- 2 Limited Warranty and Related Remedies/Disclaimers:
 - 2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
 - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.
 - 2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.
- 3 Regulatory Notices:
 - 3.1 United States
 - 3.1.1 Notice applicable to EVMs not FCC-Approved:

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- · Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

- 3.3 Japan
 - 3.3.1 Notice for EVMs delivered in Japan: Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に 輸入される評価用キット、ボードについては、次のところをご覧ください。 http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page
 - 3.3.2 Notice for Users of EVMs Considered "Radio Frequency Products" in Japan: EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

- 1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
- 2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
- 3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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- 2. 実験局の免許を取得後ご使用いただく。
- 3. 技術基準適合証明を取得後ご使用いただく。
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- 3.3.3 Notice for EVMs for Power Line Communication: Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page 電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page
- 3.4 European Union
 - 3.4.1 For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

- 4 EVM Use Restrictions and Warnings:
 - 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
 - 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
 - 4.3 Safety-Related Warnings and Restrictions:
 - 4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.
 - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
 - 4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.
- Accuracy of Information: To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. Disclaimers:

- 6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.
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- 8. Limitations on Damages and Liability:
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 - 8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.
- 9. Return Policy. Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.
- 10. Governing Law: These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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