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NTE4538B
Integrated Circuit
CMOS, Dual Precision Retriggerable/ Resettable Monostable Multivibrator

Description:

The NTE4538B is a dual, retriggerable, resettable, monostable multivibrator in a 16–Lead DIP type package. It may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X. Linear CMOS techniques allow more precise control of output pulse width.

Features:

- ±1.0% (Typ) Pulsewidth Variation from Part to Part
- ±0.5% (Typ) Pulsewidth Variation over Temperature Range
- New Formula: T = RC (T in Seconds, R in Ohms, C in Farads)
- Pulse Width Range – 10μs to ∞
- Symmetrical Output Sink an Source Capability
- Latched Trigger Inputs
- Separate Latched Reset Inputs
- Quiescent Current (Standby) = 5nA/Package (Typ) at 5Vdc
- 3Vdc to 18Vdc Operational Limits
- Triggerable from Positive or Negative Going Edge
- Capable of Driving Two Low–Power TTL Loads, One Low–Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- For Pulse Widths Less Than 10μs, the NTE4525B is Recommended

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (All Inputs), V_{in} . . . . . –0.5 to V_{DD} to +0.5V
DC Current Drain (Per Pin), I 10mA
Operating Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. This device contains circuitry to protect the input against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Electrical Characteristics: (Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage "0" Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current	I_{OH}									
(V_{OH} = 2.5Vdc) Source		5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
(V_{OH} = 4.6Vdc)			–0.64	–	–0.51	–0.88	–	–0.36	–	mAdc
(V_{OH} = 9.5Vdc)		10	–1.6	–	–1.3	–2.25	–	–0.9	–	mAdc
(V_{OH} = 13.5Vdc)		15	–4.2	–	–3.4	–8.8	–	–2.4	–	mAdc
(V_{OL} = 0.4Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current, Pin2 or Pin14	I_{in}	15	–	±0.02	–	±0.00001	±0.05	–	±0.5	µAdc
Input Current, Other Inputs	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance, Pin2 or Pin14	C_{in}	–	–	–	–	25	–	–	–	pF
Input Capacitance, Other Inputs (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	µAdc
		15	–	15	–	0.015	15	–	600	µAdc
Quiescent Current, Active State (Q1 = Logic 1) (Q2 = Logic 0)	I_{DD}	5.0	–	5.0	–	35	–	–	150	µAdc
		10	–	10	–	80	–	–	300	µAdc
		15	–	15	–	1255	–	–	600	µAdc
Total Supply Current at an External Load Capacitance (C_L) and at External Timing Network (R_X, C_X) (Note 3)	I_T	5 10 15	$I_T = (3.5 \times 10^{-2}) R_X C_X f + 4 C_x f + 1 \times 10^{-5} C_L f$ $I_T = (8 \times 10^{-2}) R_X C_X f + 9 C_x f + 2 \times 10^{-5} C_L f$ $I_T = (1.25 \times 10^{-1}) R_X C_X f + 12 C_x f + 3 \times 10^{-5} C_l f$ where: I_T in µA (one monostable switching only). C_X in µF, C_L in pF, R_X in k ohms, and f in Hz is the input frequency.								

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. Noise immunity specified for worst−case input combination.
Noise margin for both "1" and "0" = 1.0Vdc min @ V_{DD} = 5Vdc
2.0Vdc min @ V_{DD} = 10Vdc
2.5Vdc min @ V_{DD} = 15Vdc

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					
t_{TLH} = (1.35ns/pf) C_L + 33ns		5.0	–	100	200	ns
t_{TLH} = (0.60ns/pf) C_L + 20ns		10	–	50	100	ns
t_{TLH} = (0.40ns/pf) C_L + 20ns		15	–	40	80	ns
Output Fall Time	t_{THL}					
t_{THL} = (1.35ns/pf) C_L + 33ns		5.0	–	100	200	ns
t_{THL} = (0.60ns/pf) C_L + 20ns		10	–	50	100	ns
t_{THL} = (0.40ns/pf) C_L + 20ns		15	–	40	80	ns
Propagation Delay Time, A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (0.90ns/pF) C_L + 255ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.36ns/pF) C_L + 132ns		10	–	150	300	ns
t_{PLH}, t_{PHL} = (0.26ns/pF) C_L + 97ns		15	–	100	220	ns
Propagation Delay Time, C_D to Q or $\overline{Q}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (0.90ns/pF) C_L + 205ns		5.0	–	250	500	
t_{PLH}, t_{PHL} = (0.36ns/pF) C_L + 107ns		10	–	125	250	ns
t_{PLH}, t_{PHL} = (0.26ns/pF) C_L + 82ns		15	–	95	190	ns
Minimum Input Pulse Width, A, B or C_D	t_{WH}, t_{WL}	5.0	–	35	70	ns
		10	–	30	60	ns
		15	–	25	50	ns
Minimum Retrigger Time	t_{rr}	5.0	0	–	–	ns
		10	0	–	–	ns
		15	0	–	–	ns
Output Pulse Width – Q or $\overline{Q}$	T					
C_X = 0.002µF, R_X = 10kΩ		5.0	210	222	234	µs
		10	212	224	236	µs
		15	214	226	238	µs
C_X = 0.1µF, R_X = 100kΩ		5.0	9.3	9.86	10.4	ms
		10	9.5	10.0	10.5	ms
		15	9.6	10.14	10.7	ms
C_X = 10µF, R_X = 100kΩ		5.0	0.915	0.965	1.015	s
		10	0.93	0.98	1.03	s
		15	0.94	0.99	1.04	s
Pulse Width Match Between Circuits in the Same Package						
C_X = 0.1µF, R_X = 100kΩ		5.0	–	±1	–	%
		10	–	±1	–	%
		15	–	±1	–	%

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Operating Conditions:

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
External Timing Resistance	R_X	–	5.0	–	Note 4	kΩ
External Timing Capacitance	C_X	–	0	–	No Limit	pF

Note 4. The maximum usable resistance R_X is a function of the leakage of the capacitor C_X, leakage of the NTE4538B, and leakage due to board layout and surface resistance.

Pin Connection Diagram