REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add one vendor CAGE 18324. Change parameters in table I. Add program procedure B. Update vendor's part numbers Change screening and group A inspection.	25 June 1987	

REV																									
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REV STATUS OF PAGES	REV	A	A			A	A	A						A				A	A	A	A		A	A	
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Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:
9 October 1986

AMSC N/A

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MILITARY DRAWING

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TITLE: MICROCIRCUITS, 1K x 8 REGISTERED PROM WITH PROGRAMMABLE INITIALIZE, MONOLITHIC SILICON

SIZE	CODE IDENT. NO.	DWG NO.
A	14933	5962-86706
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1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-86706	01	L	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	27S35 82HS187A	1024 x 8 bit registered PROM with programmable $\overline{\text{INITIALIZE}}$ (Asynchronous)	45 ns
02	27S35A 82HS187A	1024 x 8 bit registered PROM with programmable $\overline{\text{INITIALIZE}}$ (Asynchronous)	40 ns
03	27S37 82HS189A	1024 x 8 bit registered PROM with programmable $\overline{\text{INITIALIZE}}$ (Synchronous)	45 ns
04	27S37A 82HS189A	1024 x 8 bit registered PROM with programmable $\overline{\text{INITIALIZE}}$ (Synchronous)	40 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
L	D-9 (24-lead, 1/4" x 1 1/4"), dual-in-line package
K	F-6 (24-lead, 3/8" x 5/8"), flat package
3	C-4 (28-terminal, .450" x .450"), square chip carrier package
X	C-12 (32-terminal, .450" x .550"), rectangular chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
DC input voltage	-0.5 V dc to +5.5 V dc
DC voltage applied to outputs	-0.5 V dc to +5.5 V dc
DC input current	-30 mA to +5.0 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	1.0 W
Lead temperature (soldering, 10 seconds)	300°C
Thermal resistance, junction-to-case (θ_{JC}) 2/:	
Cases K and L	See MIL-M-38510, appendix C
Case 3	80°C/W 3/
Case X	75°C/W 3/
Junction temperature (T_J)	175°C
DC voltage applied to outputs during programming	21 V dc
DC current into outputs during programming (max duration of 1.0 s)	250 mA dc

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_{IH})	2.0 V dc
Maximum low-level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

1/ Must withstand the added P_D due to short circuit test (e.g., I_{SC}).
2/ Heat sinking is recommended to reduce the junction temperature.
3/ When a thermal resistance value for this case is included in MIL-M-38510, appendix C, that value shall supersede the value indicated herein.

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3.2 Design, construction, and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Logic diagram. The logic diagram shall be as specified on figure 2.

3.2.3 Truth tables.

3.2.3.1 Unprogrammed devices. Testing to the applicable truth table, or alternate testing as specified in 4.3.1.d, shall be used for unprogrammed devices for contracts involving no altered item drawing. When testing is required per 4.3 herein, the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an altered item drawing.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.9 Processing options. Since the PROM is an unprogrammed memory capable of being programmed by either the manufacturer or the user to result in a wide variety of PROM configurations, two processing options are provided for selection, using an altered item drawing.

3.9.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 4.3.1(d). It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.9.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing shall be satisfied by the manufacturer prior to delivery.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ (unless otherwise specified)	Device Type	Group A subgroups	Limits Min	Limits Max	Unit
Output high voltage	V_{OH}	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}, I_{OH} = -2.0 mA	All	1, 2, 3	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}	All	1, 2, 3		0.50	V
Input high voltage	V_{IH}	1/ 2/	All	1, 2, 3	2.0		V
Input low voltage	V_{IL}	1/ 2/	All	1, 2, 3		0.8	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA	All	1, 2, 3		-1.2	V
Input low current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.45 V	All	1, 2, 3		-250	µA
Input high current	I_{IH}	V_{CC} = 5.5 V, V_{IN} = 5.5 V	All	1, 2, 3		50	µA
Output short-circuit current	I_{SC}	V_{CC} = 5.5 V, V_{OUT} = 0 V 3/	All	1, 2, 3	-15	-90	mA
Power supply current	I_{CC}	V_{CC} = 5.5 V, All inputs = GND	All	1, 2, 3		185	mA
Output leakage current	I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	All	1, 2, 3		60	µA
		$\overline{V_G}$ = 2.4 V, V_O = 0.4 V	All	1, 2, 3		-60	µA
Functional tests		See 4.3.1(e)	All	7, 8			
Input capacitance	C_{IN}	V_{IN} = 2.0 V, f = 1.0 MHz 4/	All	4		10.0	pF
Output capacitance	C_{OUT}	V_{OUT} = 2.0 V, f = 1.0 MHz 4/	All	4		13.0	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ (unless otherwise specified)	Device Type	Group A subgroups	Limits Min	Limits Max	Unit
Address to K high, setup time	TAVKH	5/	02, 04	9, 10, 11	40		ns
			01, 03	9, 10, 11	45		ns
Address to K high, hold time	TKHAX	5/	All	9, 10, 11	5		ns
Delay from K high to output valid, for initially active outputs (high or low)	TKHQV1	5/	02, 04	9, 10, 11		25	ns
			01, 03	9, 10, 11		30	ns
K pulse width (high or low)	TKHKL, TKLKH	5/	All	9, 10, 11	25		ns
$\overline{GS}$ to K high setup time	TGSVKH	5/	All	9, 10, 11	15		ns
$\overline{GS}$ to K high hold time	TKHGSX	5/	All	9, 10, 11	5.0		ns
Delay from $\overline{I}$ low to output valid (high or low) 6/	TILQV	5/	01	9, 10, 11		40	ns
			02	9, 10, 11		35	ns
Asynchronous $\overline{I}$ recovery to K high 6/	TIHKH	5/	01, 02	9, 10, 11	25		ns
Asynchronous $\overline{I}$ pulse width (low) 6/	TILIH	5/	01, 02	9, 10, 11	30		ns
$\overline{IS}$ to K high setup time 7/	TISVKH	5/	03	9, 10, 11	35		ns
			04	9, 10, 11	30		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ (unless otherwise specified)	Device Type	Group A subgroups	Limits Min	Limits Max	Unit
$\overline{IS}$ to K high hold time 6/	TKHISX	5/	03, 04	9, 10, 11	5		ns
Delay from K high to output valid for initially high-Z outputs	TKHQV2	5/	01, 03	9, 10, 11		35	ns
			02, 04	9, 10, 11		30	ns
Delay from $\overline{G}$ low to output valid (high or low)	TGLQV	5/	01, 03	9, 10, 11		35	ns
			02, 04	9, 10, 11		30	ns
Delay from K high to output high-Z 8/	TKHQZ	5/	01, 03	9, 10, 11		35	ns
			02, 04	9, 10, 11		30	ns
Delay from $\overline{G}$ high to output high-Z 8/	TGHQZ	5/	01, 03	9, 10, 11		35	ns
			02, 04	9, 10, 11		30	ns

1/ These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

2/ V_{IL} and V_{IH} threshold levels are guaranteed for 0.8 V and 2.0 V respectively during dc testing. For ac and functional testing V_{IL} and V_{IH} limits of -0.2 V and 4.0 V are implemented to allow for noise margins needed in a high speed, automated test equipment environment, when fast switching of multiple I/O's is encountered.

3/ Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.

4/ These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

5/ AC tests are performed with input 10 to 90% rise and fall times of 5 ns or less.

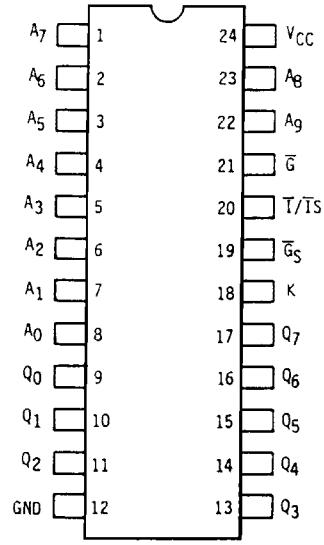
6/ Applies only when programmable initialize is in the asynchronous operation mode.

7/ Applies only when programmable initialize is in the synchronous operation mode.

8/ TKHQZ and TGHQZ are measured to the V_{OH} -0.5 V and V_{OL} +0.5 V output levels respectively. All other switching parameters are tested from and to the 1.5 V threshold levels.

9/ All voltages given are referenced to the test system ground for ac and functional testing. Voltages given for dc testing are referenced to the microcircuit ground terminal.

Device types 01 thru 04
Cases L and K



Case 3

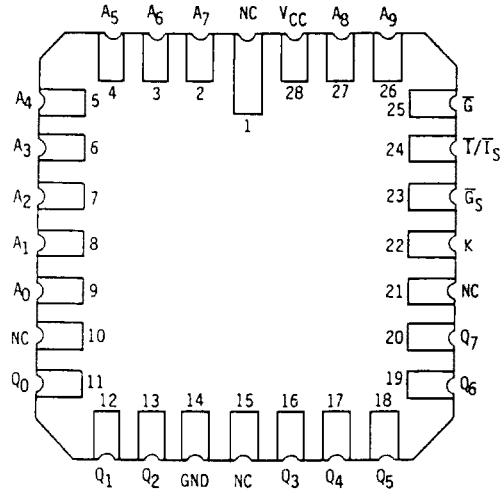


FIGURE 1. Terminal connections (top view).

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Case X

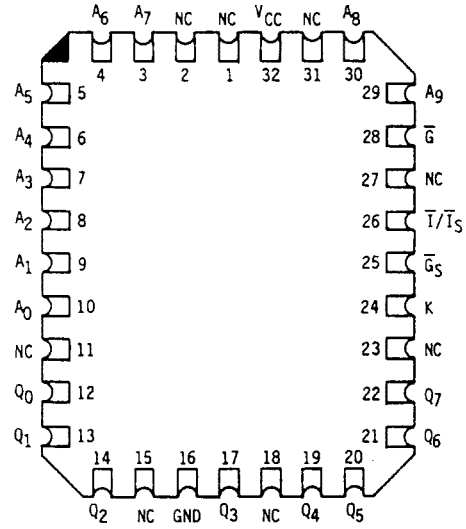

FIGURE 1. Terminal connections (top view) - continued.

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Device types 01 and 02

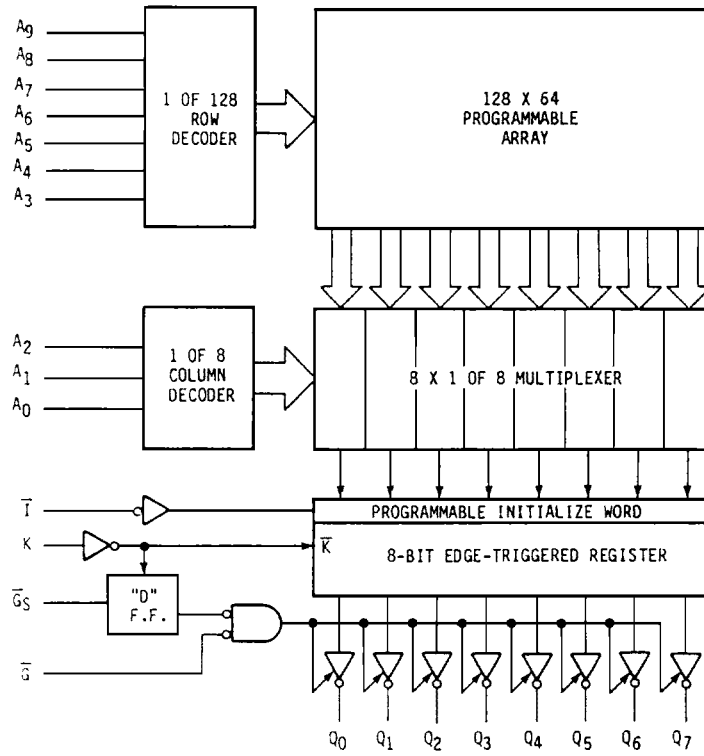

FIGURE 2. Logic diagram.

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Device types 03 and 04

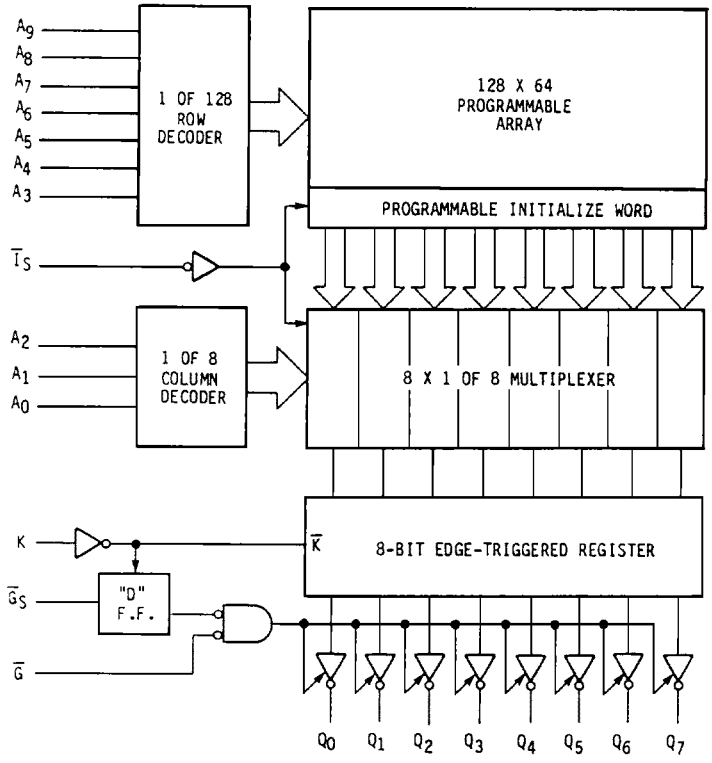

FIGURE 2. Logic diagram-continued.

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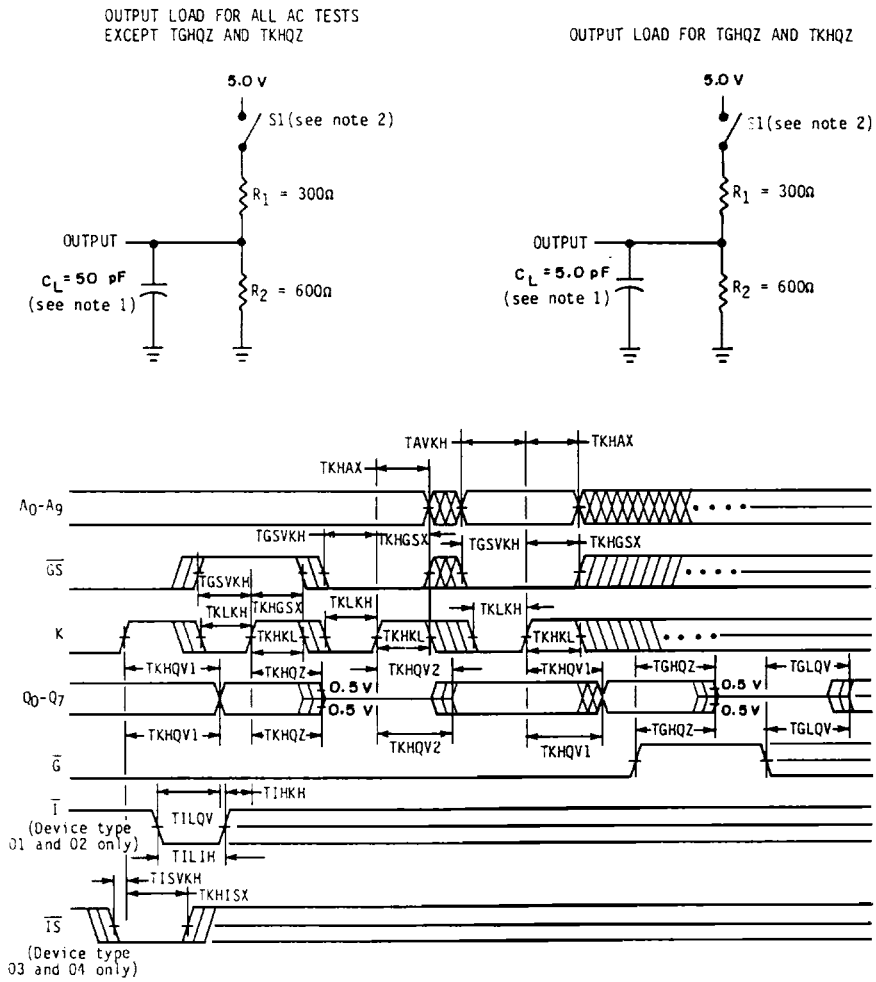

Notes:

1. C_L = includes all stray and fixture capacitance.
2. S_1 is open for output data high to high-Z and high-Z to output data high tests.
   S_1 is closed for all other tests.
3. All device test loads should be located within 2.0 inches of device outpin pin.

FIGURE 3. Switching times test circuit and waveforms.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. All devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroup 9, 10 and 11. Either of two techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing per the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.3.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than four total device failures allowed. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than four total device failures allowable.

e. Subgroups 7 and 8 must verify input to output logic combinations.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

c. The group C, subgroup 1 sample shall include devices tested in accordance with 4.3.1.d.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10**, 11**
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8,
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

4.4 Programming procedure for circuit A. The characteristics on table IIIA and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming as shown on figure 4. The waveforms on figure 4 and the programming procedures of table IIIA shall apply to these procedures.

b. Terminate all outputs, to V_{ONP} through a pull up resistor, R.

c. Apply V_{CCP} to V_{CC}.

d. Connect $\overline{G}$ and $\overline{G}_S$ to V_{ILP}.

e. Raise $\overline{I}/\overline{I}_S$ input to V_{IHP}.

f. Address the PROM with the binary address of the selected word to be programmed.

g. Apply V_{IHP} to the $\overline{G}$ input.

h. After a delay of T_1, apply a low to high transition to the clock (K).

i. After a delay of T_2, apply V_{OP} for a duration of T_3 + (rise time of the enable input) + Tp, to the output selected for programming.

j. After a delay of T_3 + rise time of the programmed output, apply V_{FE} for a duration of Tp + rise time of the programmed output + T_4, to the G input. G is then reduced to V_{ILP}.

k. After a delay of T_5, the opening of the fuse is verified. Each data verification must be preceded by a Low to High transition of the clock (K). This will load the array data into the output data register. During verification, V_{CC} remains unchanged at V_{CCP}.

l. The outputs should be programmed one at a time, since the internal decoding circuitry is capable of sinking only one unit of programming current at a time. Note that the PROM is supplied with fuses generating a low level logic output. Programming a fuse will cause the output to go to a high level logic in the verify mode.

m. Repeat 4.4a through 4.4k for all other bits to be programmed.

n. If any unit does not verify data as programmed, it shall be considered a programming reject.

4.4.1 Programming the initialized word.

a. Repeat steps 4.4a through 4.4d.

b. Connect $\overline{I}/\overline{I}_S$ to V_{ILP}. This deselects the internal programming circuitry for all other addresses.

c. The initialized word is then programmed, output by output, similar to any other address location, following 4.4g through 4.4n.

TABLE IIIA. Programming characteristics for circuit A.

Description	Parameter	Conditions T_A = +25°C ±5°C	Limits			Unit
			Min	Recommended	Max	
Fusing enable voltage at 10 to 40 mA	V_{FE}		14.5	15	15.5	V
Program voltage	V_{OP}	at 15 to 200 mA	19.5	20	20.5	V
Input high level during programming and verify	V_{IHP}		2.4	5	5.5	V
Input low level during programming and verify	V_{ILP}		0.0	0.3	0.5	V
V_{CC} during programming	V_{CCP}	at I_{CC} = 50 to 200 mA	5	5.2	5.5	V
Rate of output voltage change	dV_{OP}/dt		20		250	V/uS
Rate of fusing enable voltage change	dV_{FE}/dt		50		1000	V/uS
Fusing time first attempt	tp		40	50	100	us
Fusing time subsequent attempts	tp		4	5	1000	ms
Delays between various level changes	t_1-t_6		100		2000	ns
Period during which output is sensed for V_{BLOWN} level	t_V			500		ns
Pull-up voltage on outputs not being programmed	V_{ONP}		V_{CCP} -0.3	V_{CCP}	V_{CCP} +0.3	V
Pull-up resistor on outputs not being programmed	R		0.2	2	5.1	KΩ
Current into outputs not to be programmed	I_{ONP}				20	mA

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4.5 Programming procedure for circuit B. The programming characteristics in table IIIB and the following procedures shall be used for programming the device.

a. Connect the device, following the electrical configuration for programming. The waveforms shown on figure 4 and the programming characteristics of table IIIB shall apply to these procedures.

b. Output pins should be terminated with a 10 kΩ resistor to V_{CC}.

c. Bypass V_{CC} to ground with a 0.01 µF capacitor.

d. Apply initial voltage of V_{IH} to the programming control pin ($\overline{CE_x}$), with appropriate voltage to chip enable pins (as applicable) in accordance with table I.

e. Apply V_{IL} to all other pins.

f. Select the word to be programmed by applying V_{IL} or V_{IH} on the appropriate address pins, and reset T_P to 5 µs.

g. Wait for T_{D1} and raise the V_{CC} pin to V_{CCP}.

h. Wait for T_{D2} and raise the corresponding output pin to V_{OPF}.

i. Wait for T_{D3} and lower the programming control pin ($\overline{CE_x}$) to V_{IL} for a duration of T_P.

j. Simultaneously lower the output to V_{IL} and begin waiting for T_{D4}.

k. Return the programming control pin, $\overline{CE_x}$ to V_{IH}.

l. Wait for T_{D5} and lower V_{CC} to V_{CCV}.

m. Wait for T_{D6} and lower input programming control pin $\overline{CE_x}$ to V_{IL} for the duration of T_V.

n. A properly blown fuse will read V_{OL}, and an unblown fuse will read V_{OH}.

1. If the fuse is blown, go to 4.5q.

2. If fuse is unblown, go to 4.5o.

o. If T_P is less than 20 µs, increment T_P by 5 µs and go to 4.5g. If T_P is equal or greater than 5 µs go to 4.5p.

p. If T_P is equal to or greater than 20 µs, then the device is a reject. STOP.

q. Wait for T_{D8} and select the next output or address to be programmed.

r. Repeat steps 4.5f through 4.5n until all required addresses are programmed.

s. Program the initialization word by applying V_{IL} to the $\overline{I}/\overline{I_S}$ pin. After the $\overline{I}/\overline{I_S}$ word is programmed, return the $\overline{I}/\overline{I_S}$ pin to V_{IH}.

t. Complete address verification, refer to table III:

1. Wait for T_{D6}, keeping V_{CC} at V_{CCV}.
2. Lower $\overline{CE_X}$ input to V_{IL}.
3. Sequentially select $\overline{I}/\overline{I_S}$ word, all addresses, $\overline{G}/\overline{G_S}$ and $\overline{I}/\overline{I_S}$ in the memory.
4. A properly blown fuse will read V_{OL}, and unblown fuse will read V_{OH}.
5. End of programming procedure.

u. Programming verification, refer to table III:

1. Wait for T_{D6} and apply clock pulse of duration TWC, refer to figure 4.
2. Wait for T_{D7} and lower input programming control pin $\overline{CE_X}$ to V_{IL} for the duration of T_V.
3. Go to 4.5n.

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TABLE IIIB. Programming characteristics for circuit B.

Parameter	Symbol	Conditions	Limits			Unit
			Min	Recommended	Max	
Power supply voltage	V_{CCP}1	I_{CCP} = 500 mA	8.5	8.75	9.0	V
Verify voltage	V_{CCV}		4.75	5.0	5.25	V
High input voltage	V_{IH}	I_{IH} = 50 µA	2.4	3.0	5.5	V
Low input voltage	V_{IL}	I_{IL} = -500 µA	0.0	0.0	0.5	V
Forced output current	I_{OPF2}		150	185	220	mA
Forced output voltage	V_{OPF}3		20.5		21.0	V
Output high voltage	V_{OH}		2.0			V
Output low voltage	V_{OL}				1.0	V
Program time	T_{PP}	50 percent to 50 percent		58		µs
V_{CC} delay time	T_{D1}	50 percent add to 10 percent V_{CCP}	10	10	25	µs
V_{OUT} delay time	T_{D2}	90 percent V_{CCP} to 10 percent V_{OPF}	1	1	5	µs
Pulse sequence delays	T_{D3}-T_{D8}	See figure 4	1	1	10	µs
V_{CC} rise time	T_{R1}	10 percent to 90 percent	4	7	8	µs
V_{OUT} rise time	T_{R2}	10 percent to 90 percent	3	10	17	µs

See footnotes at end of table.

TABLE IIIB. Programming characteristics for circuit B - Continued.

Parameter	Symbol	Conditions	Limits			Unit
			Min	Recommended	Max	
V_{CC} fall time	T_{F1}	90 percent to 10 percent	2	4	10	µs
V_{OUT} fall time	T_{F2}	90 percent to 10 percent	3	7	21	µs
$\overline{CEx}$ programming	Tp4	10 percent to 90 percent	5		20	µs
$\overline{CEx}$ verify pulse	T_V width	10 percent to 10 percent	5	5	10	µs
Clock pulse width (CK)	TWC	50 percent to 50 percent	.5	.75	5	µs

1. If the overall program/verify cycle Tpp exceeds the recommended (rec) value, a 25 percent duty cycle must be used for V_{CCP}.
2. For the program current pulse I_{OPF}, a current source must be used with a voltage limit set at V_{OPF}.
3. Maximum output voltage V_{OPF} must be limited to 21.0 V.
4. T_p is 5 µs at first attempt and increments 5 µs each additional programming attempt until fuse is blown or 20 µs is reached.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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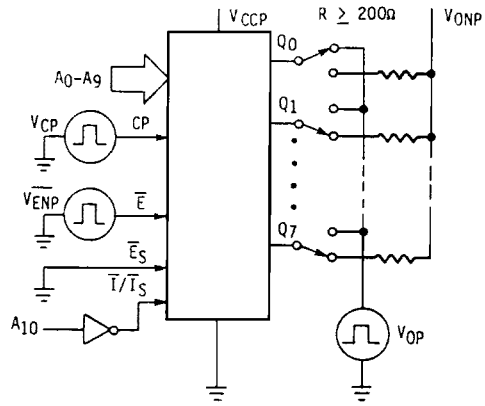
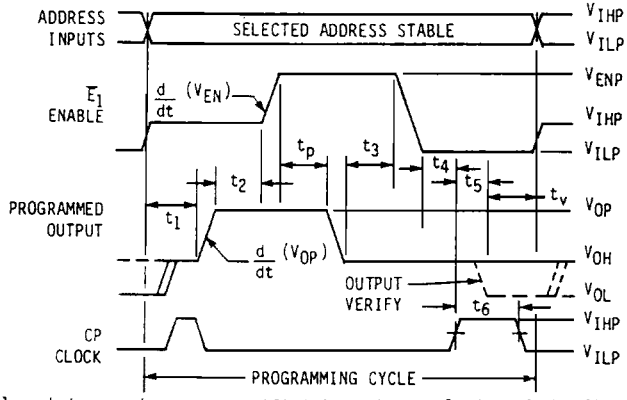
CIRCUIT A
simplified programming circuit



Programming Waveforms



Notes:

1. All delays between edges are specified from the completion of the first edge to the beginning of the second edge; i.e, not the midpoints.
2. Delays t_1 through t_6 must be greater than 100 ns; maximum delays of 1 µs are recommended to minimize heating during programming.
3. During t_v the output being programmed is switched to the load R and read to determine if additional programming pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through register R which provides output current limiting.

FIGURE 4. Programming circuit and waveforms.

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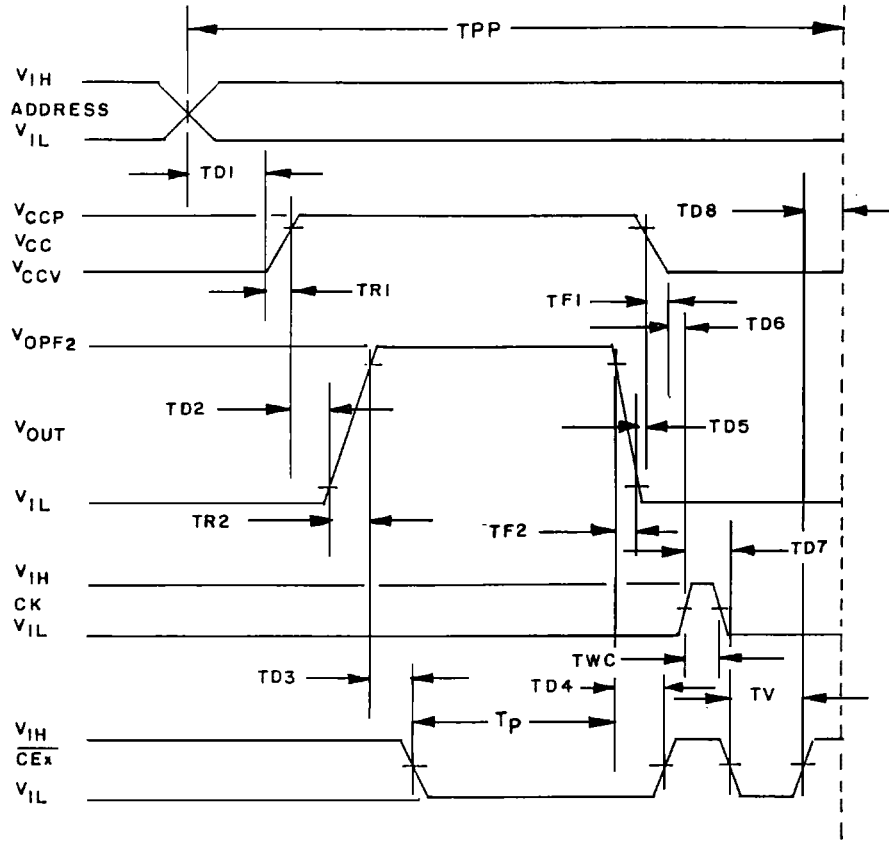
Circuit B



Current clamp will be needed.

Refer to table IIIB for I_{OPF} current clamp.

FIGURE 4. Programming circuit and waveforms - Continued.

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6.4 Approved source of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8670601LX	34335 18324	AM27S35/BLA 82HS187A/BLA
5962-8670601KX 5962-8670601XX	34335 34335	AM27S35/BKA AM27S35/BUA
5962-86706013X	34335 18324	AM27S35/B3A 82HS187A/B3X
5962-8670602LX	34335 18324	AM27S35A/BLA 82HS187A/BLA
5962-8670602KX 5962-8670602XX	34335 34335	AM27S35A/BKA AM27S35A/BUA
5962-86706023X	34335 18324	AM27S35A/B3A 82HS187A/B3X
5962-8670603LX	34335 18324	AM27S37/BLA 82HS189A/BLA
5962-8670603KX 5962-8670603XX	34335 34335	AM27S37/BKA AM27S37/BUA
5962-86706033X	34335 18324	AM27S37/B3A 82HS189A/B3X
5962-8670604LX	34335 18324	AM27S37A/BLA 82HS189A/BLA
5962-8670604KX 5962-8670604XX	34335 34335	AM27S37A/BKA AM27S37A/BUA
5962-86706043X	34335 18324	AM27S37A/B3A 82HS189/B3X

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address	Programming Procedure	Fusible Link
34335	Advanced Micro Devices, Incorporated 901 Thompson Place Sunnyvale, CA 94088	A	Platinum silicide fuse
18324	Signetics, Incorporated 4130 S. Market Court Sacramento, CA 95834	B	Zapped vertical emitter

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