

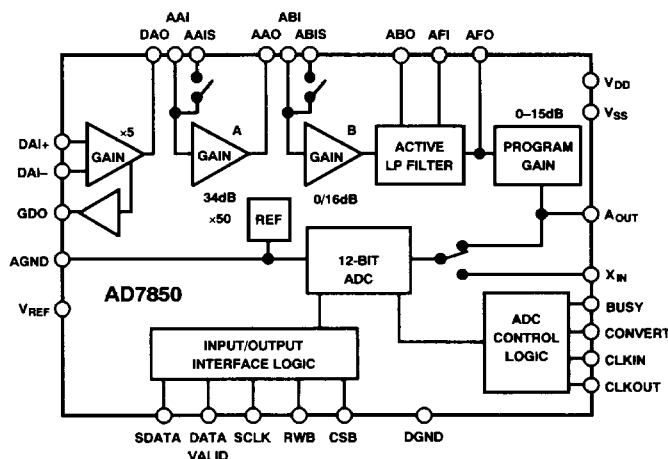
### FEATURES

**Functional Complete DAS**  
**Single Package**  
**Monolithic**  
**High Impedance Differential Inputs**  
**Guaranteed Low 1 nA Input Bias Current**  
**Guaranteed 80 dB Common-Mode Rejection**  
**External Selectable Bandpass Filter Frequencies**  
**Software Programmable Gain Selection**  
**12-Bit A/D Converter with On-Chip Reference**  
**Serial Communication Interface**  
**Max Throughput Rate of 66 kSPS**  
**± 5 V Supplies**  
**Low 175 mW (typ) Power Consumption**  
**Small 28-Terminal Surface Mount Package (PLCC)**

### APPLICATION

**Small Signal Data Acquisition**  
**ECG Signal Data Acquisition**  
**Patient Monitoring**

### FUNCTIONAL BLOCK DIAGRAM



### PRODUCT HIGHLIGHTS

1. Single chip, complete small signal DAS. It includes a high performance differential front end amplifier, programmable gain stages, externally controlled high and low corner frequencies, and a 12-bit AD converter with on-chip reference.
2. Input amplifier has extremely low input bias current of <math><1\text{ nA}</math> over full temperature range. Typical input bias current at ambient temperature is 20 pA.
3. On-chip guard driver to minimize external components.
4. Software programmable gain setting with a gain range of 0 dB to 31 dB.
5. On-chip clock oscillator to minimize external components.
6. A serial interface is provided to make it easy to use AD7850 in applications where full isolation from the mains power is required.
7. Serial interface supports multichannel applications with minimal external components.
8. LC<sup>2</sup>MOS circuitry gives low power drain (175 mW typ) from +5 V, and -5 V supplies.

### GENERAL DESCRIPTION

The AD7850 is a complete data acquisition system for very small signals (i.e., biomedical ECG) with a data sampling rate of minimum 66,000 samples/sec. It provides high accuracy, high stability, and functional completeness in a single 28-pin package.

It includes a high performance instrumentation amplifier at the front-end, bandpass filter, and an accurate 12-bit ADC with on-chip reference.

An on-chip clock circuit is provided, which may be used with a crystal for stand-alone operation. Alternatively, the clock input may be driven from an external CMOS-compatible clock source such as a microprocessor clock.

The AD7850 serial interface is compatible with many microprocessors and digital signal processors such as the ADSP-2100, TMS32020,  $\mu$ PD7720, and DSP-56000. It can also be used with general purpose serial to parallel converters such as shift registers.

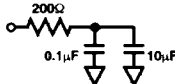
The AD7850 is fabricated in Analog Devices' linear compatible CMOS process (LC<sup>2</sup>MOS), an advanced, all ion-implanted process that combines fast CMOS logic and linear, bipolar circuits on a single chip, thus achieving excellent linear performance while still retaining low CMOS power levels.

### REV. 0

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# AD7850—SPECIFICATIONS ( $V_{DD} = +5\text{ V} \pm 5\%$ , and $V_{SS} = -5\text{ V} \pm 5\%$ . All specifications $T_{MIN}$ to $T_{MAX}$ unless otherwise noted.)

Parameter	All Grades	Units	Test Condition/Comments
<b>INPUT AMPLIFIER</b>			
<b>GAIN</b>			
Gain Range	14 5	dB V/V	
Gain Error	$\pm 0.1$	dB max	Over Full Temperature Range
<b>VOLTAGE OFFSET</b>			
Input Offset Voltage	10	mV max	
<b>INPUT CURRENT</b>			
Input Bias Current	500	pA typ	Over Full Temperature Range
Typical Input Bias	20	pA	Typical at +25°C
<b>INPUT</b>			
Input Resistance	2	G $\Omega$ typ	
Input Capacitance	6	pF typ	
Differential Input Voltage Range			
Gain = 5 (DC Coupled)	$\pm 0.5$	V max	
Common-Mode Input Voltage	$\pm 0.5$	V max	
Common-Mode Rejection Ratio	75	dB min	Typically 86 dB
<b>NOISE</b>			
Voltage Noise (RTI)	2 5	$\mu\text{V p-p typ}$ $\mu\text{V p-p typ}$	Bandwidth 0.1 Hz–10 Hz @ +25°C Bandwidth 0.1 Hz–100 Hz @ +25°C Assume Gaussian Noise $-V_{p-p} = 6.6 \times V_{rms}$ , 0.1% Probability of Error
<b>GUARD DRIVER</b>			
Capacitive Load	100	pF max	
Resistive Load	2	k $\Omega$ min	
<b>AMPLIFIER A</b>			
Gain	34 50	dB V/V	
Gain Accuracy	0.1 1.2	dB max %	
Input Offset Voltage	2	mV max	
Input Bias Current	5	nA typ	
<b>AMPLIFIER B/LOW PASS FILTER</b>			
Gain			
Low	0 1.0	dB V/V	
High	16 6.3	dB V/V	
Gain Accuracy	0.2 2.4	dB max %	
Input Offset Voltage	2	mV max	
Resistors in Network	5	% max	of Absolute Value, over Full Temperature Range
<b>PROGRAMMABLE GAIN AMPLIFIER</b>			
Gain			
Minimum Gain	0 1.0	dB V/V	
Maximum Gain	15 5.6	dB V/V	
Gain Step Size	1 12.2	dB %	
Gain Accuracy	0.2 1.0	dB max V/V	
Input Offset Voltage	2	mV max	

Parameter	All Grades	Units	Test Condition/Comments
<b>CONVERTER (Core Cell Is the AD7870)</b>			
<b>DYNAMIC PERFORMANCE</b>			
Signal-to-Noise Ratio (SNR)	68	dB min	$V_{IN} = 1 \text{ kHz Sine}, f_{SAMPLE} = 10 \text{ kHz}$
Total Harmonic Distortion	-80	dB max	$V_{IN} = 1 \text{ kHz Sine}, f_{SAMPLE} = 10 \text{ kHz}$
No Missed Codes	Guaranteed		
Track/Hold Acquisition Time	2	$\mu\text{s max}$	
Conversion Time	13.25	$\mu\text{s}$	@ 4 MHz Clock Frequency
<b>DC ACCURACY</b>			
Resolution	12	Bits	
Relative Accuracy	$\pm 1$	LSB typ	
DNL	$\pm 1$	LSB typ	
Bipolar Zero Offset	$\pm 0.3$	% typ	@ $V_{IN} = 0 \text{ V}$
Full-Scale Error	$\pm 0.3$	% typ	@ $V_{IN} = -3 \text{ V}$ or $V_{IN} = +3 \text{ V}$ , Relative to Reference
<b>ANALOG INPUT</b>			
Input Voltage Range	$\pm 3$	V	
Input Current	$\pm 550$	$\mu\text{A max}$	
<b>REFERENCE OUTPUT</b>			
Reference Voltage @ +25°C	2.98/3.02	V min/V max	AC Decoupling Required 
Reference Tempco	$\pm 40$	ppm/°C typ	
<b>DIGITAL INTERFACE</b>			
<b>INPUTS</b>			
Logic "1" Voltage	+2.0	V min	
Logic "0" Voltage	+0.8	V max	
Input Current (CLKIN)	$\pm 60$	$\mu\text{A max}$	$V_{IN} = 0 \text{ to } V_{DD}$
Input Current (Other Inputs)	$\pm 10$	$\mu\text{A max}$	$V_{IN} = 0 \text{ to } V_{DD}$
Input Capacitance	10	pF max	
<b>OUTPUTS</b>			
Logic "1" Voltage	+2.4	V min	$I_{SOURCE} = 200 \mu\text{A}$
Logic "0" Voltage	+0.4	V max	$I_{SINK} = 1.6 \text{ mA}$
Floating State Leakage	$\pm 10$	$\mu\text{A max}$	
Floating State Capacitance	15	pF max	
<b>POWER REQUIREMENTS</b>			
$V_{DD}$	+5	V nominal	$\pm 5\%$ for Specified Performance
$V_{SS}$	-5	V nominal	$\pm 5\%$ for Specified Performance
$I_{DD}$	25	mA max	
$I_{SS}$	20	mA max	
Power Dissipation	175	mW typ	
<b>TEMPERATURE RANGE (<math>T_{MIN}</math> to <math>T_{MAX}</math>)</b>	0 to +70	°C	

Specifications subject to change without notice.

### ABSOLUTE MAXIMUM RATINGS\*

( $T_A = +25^\circ\text{C}$  unless otherwise noted)

$V_{DD}$ to DGND	-0.3 V to +7 V
$V_{SS}$ to DGND	+0.3 V to -7 V
AGND to DGND	-0.3 V to $V_{DD} + 0.3 \text{ V}$
Analog Input Voltage to AGND	$V_{SS}$ to $V_{DD}$
Digital Input Voltage to DGND	-0.3 to $V_{DD} + 0.3 \text{ V}$
Digital Output Voltage to DGND	-0.3 to $V_{DD} + 0.3 \text{ V}$
Operating Temperature Range	0°C to +70°C
Storage Temperature	-65°C to +150°C
Power Dissipation (Any Package) to +75°C	450 mW
Derates above +75°C	by 6 mW/°C

\*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

### ORDERING GUIDE

Model	Temperature Range	SNR (dB min)	Package Option <sup>1</sup>
AD7850JP	0°C to +70°C	68	P-28A

<sup>1</sup>P = Plastic leaded Chip Carrier (PLCC).

### CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

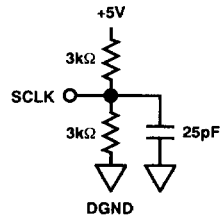


# AD7850

## TIMING CHARACTERISTICS ( $V_{DD} = +5\text{ V}$ , $V_{SS} = -5\text{ V}$ , Ambient Temperature $+25^\circ\text{C}$ )

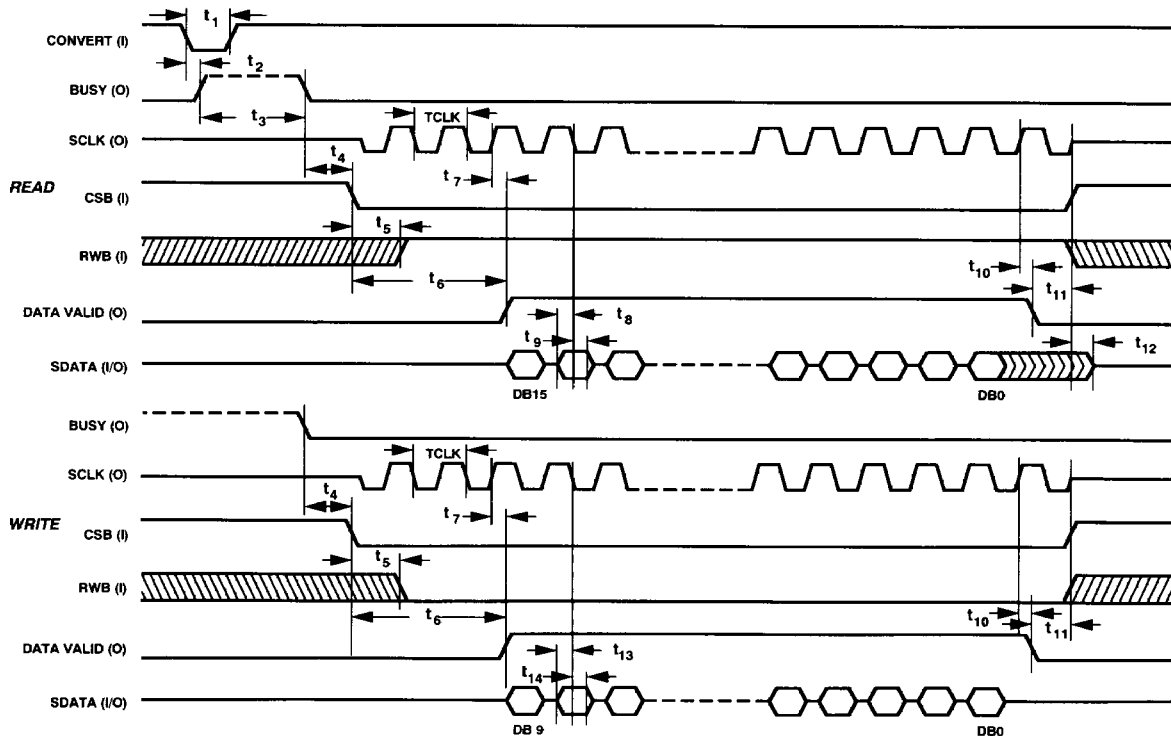
Parameter	Limit	Units	Conditions/Comments
<b>TIMING</b>			
$t_{CLK}$	10 250	$\mu\text{s}$ max ns min	Clock Cycle Time 100 kHz Clock Clock Cycle Time 4 MHz Clock
$t_1$	$t_{CLK}$	ns min	ADC Start Convert Pulse Width
$t_2$	80	ns max	CONVERT $\downarrow$ to BUSY $\uparrow$
$t_3$	$53 * t_{CLK}$	ns max	ADC Busy Period
$t_4$	0	ns min	BUSY $\downarrow$ to CSB $\downarrow$
$t_5$	$2.5 t_{CLK}$	ns max	CSB $\downarrow$ to RWB
$t_6$	$2.5 t_{CLK}$ $4.5 t_{CLK}$	ns min ns max	CSB $\downarrow$ to DATA VALID $\uparrow$ CSB $\downarrow$ to DATA VALID $\uparrow$
$t_7$	30	ns max	SCLK $\uparrow$ to DATA VALID $\uparrow$
$t_8$	30	ns min	Data at Output before SCLK $\downarrow$
$t_9$	50	ns min	Data at Output after SCLK $\downarrow$
$t_{10}$	30	ns max	SCLK $\uparrow$ to DATA VALID $\downarrow$
$t_{11}$	0	ns min	DATA VALID $\downarrow$ to CSB/RWB $\uparrow$
$t_{12}$	50	ns max	CSB $\uparrow$ to Data and SCLK Float (See diagram below.)
$t_{13}$	0	ns min	Data Setup Time before SCLK $\downarrow$
$t_{14}$	$0.5 t_{CLK}$	ns min	Data Hold Time after SCLK

\*The Internal Logic is dynamic so must be continuously clocked at 100 kHz minimum.



HIGH OR LOW TO TRI-STATE

Test Load Conditions

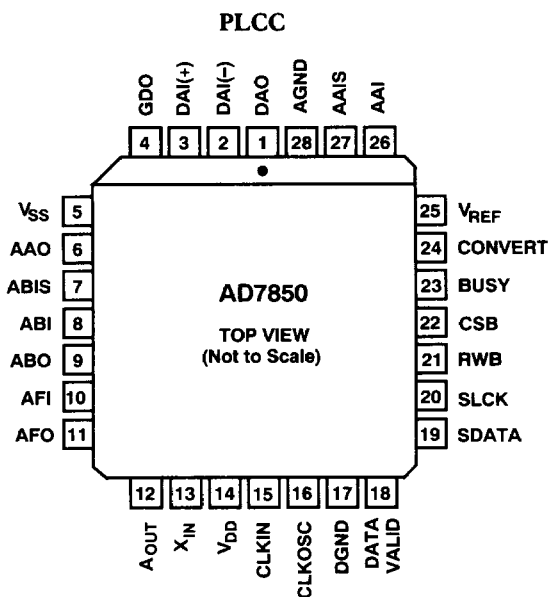


Timing Diagram

**PIN FUNCTION DESCRIPTION**

Pin	Mnemonic	Description
1	DAO	Differential Amplifier Out
2	DAI(-)	Differential Amplifier In (-)
3	DAI(+)	Differential Amplifier In (+)
4	GDO	Guard Drive Output
5	V <sub>SS</sub>	Negative Supply, -5 V
6	AAO	Amplifier A Out
7	ABIS	Amplifier B In (Switched)
8	ABI	Amplifier B In
9	ABO	Amplifier B Out
10	AFI	Active Filter In (-)
11	AFO	Active Filter Out
12	A <sub>OUT</sub>	Analog Out
13	X <sub>IN</sub>	External ADC Input
14	V <sub>DD</sub>	Positive Supply, +5 V
15	CLKIN	Clock Input Pin. An external TTL compatible clock may be applied to this pin. Alternatively, it may be used with CLKOSC to generate an internal clock (see Figure 1).
16	CLKOSC	Clock Oscillator Pin. A crystal may be connected between this pin and CLKIN to generate an internal clock. If an external clock is used, CLKOSC is not connected.
17	DGND	Digital Ground
18	DATA VALID	Status Output. When DATA VALID goes high during a read operation, it indicates that output data is valid on each succeeding SCLK falling edge. It goes low when 16 bits have been transmitted.  When DATA VALID goes high during a write operation, data will be clocked into the input latch on each succeeding SCLK falling edge. It goes low when 10 bits have been received.
19	SDATA	Serial Data Input/Output. This pin is in tristate when CSB is high.
20	SCLK	Serial Clock Output. This pin is in tristate when CSB is high.
21	RWB	Read/Write Select Input.
22	CSB	Chip Select Input.
23	BUSY	Busy Output, indicating converter status. See Timing Diagram.
24	CONVERT	Start Conversion Input.
25	V <sub>REF</sub>	Voltage Reference Out
26	AAI	Amplifier A In
27	AAIS	Amplifier A In (Switched)
28	AGND	Analog Ground

**PIN CONFIGURATION**



# AD7850

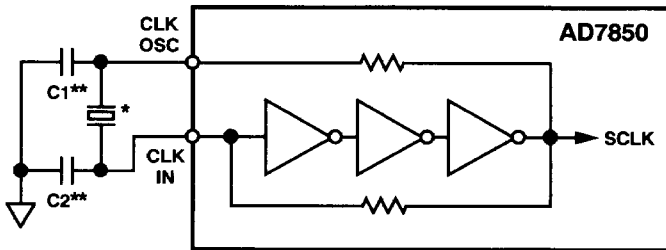
## CIRCUIT INFORMATION

### SIGNAL LEVELS

For an input gain of 5, the maximum Input Signal for Full-Scale ADC Output is  $\pm 10$  mV.

### INTERNAL CLOCK OSCILLATOR

Figure 1 shows the AD7850 internal clock circuit. A crystal or ceramic resonator may be connected as in Figure 1 to provide a clock oscillator for the internal timing. Alternatively, the crystal/resonator may be omitted and an external CMOS-compatible clock source connected to CLKIN. The mark/space ratio of the external clock must be in the range of 45/55 and 55/45. An inverted CLKIN signal will appear at the SCLK output pin.



#### NOTES:

- \* 4MHz CRYSTAL/CERAMIC RESONATOR
- \*\* C1 AND C2 CAPACITANCE VALUES DEPEND ON CRYSTAL/CERAMIC RESONATOR MANUFACTURER. TYPICAL VALUES ARE FROM 30pF TO 100pF.

Figure 1. AD7850 Internal Clock Circuit

### ACTIVE LOW-PASS FILTER

The internal active filter is implemented with a 2nd order negative feedback configuration as shown in Figure 2.

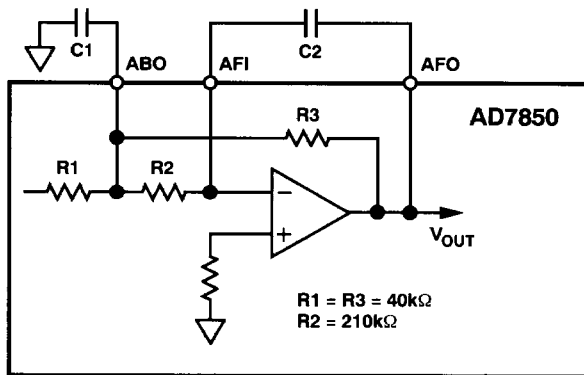


Figure 2. Low-Pass Filter

The filter cutoff frequency and filter damping factor are determined by selecting the appropriate values of  $C_1$  and  $C_2$ . The resistor value for  $R_1$  and  $R_3$  is  $40\text{ k}\Omega$  and  $R_2$  is  $210\text{ k}\Omega$ .

$$d = \sqrt{\frac{C_2}{C_1}} \left[ \sqrt{\frac{R_2}{R_3}} + \sqrt{\frac{R_3}{R_2}} + \sqrt{\frac{R_2 \times R_3}{R_1}} \right] \text{gain} = \frac{R_3}{R_1}$$

$$\text{Bandpass ripple} \frac{e_{OUT}}{e_{IN}} = -20 \log_{10} \left[ \frac{d \sqrt{4 - d^2}}{2} \right]$$

### HIGH-PASS FILTER (Example Only)

This external high-pass filter can be implemented between the input gain stage and Amplifier A.

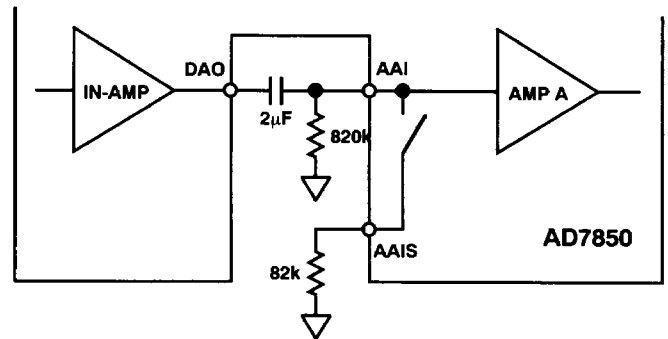


Figure 3. External High-Pass Filter

### BAND PASS FILTER (Example Only)

This external band pass filter can be implemented between Amplifier A and Amplifier B.

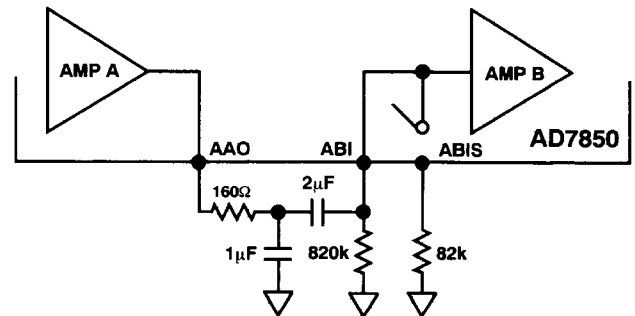


Figure 4. External Band Pass Filter

### PROGRAMMING THE AD7850

The function of the part is set by writing a ten-bit word to the control register on chip using the serial interface. The timing for the write operation is provided in the timing diagrams.

The order and function of the bits in the control register is as follows:

- DB9 A "1" sets external input to the ADC.  
 DB8 Internal use only. Must be set to a "1."  
 DB7 Internal use only. Must be set to a "1."  
 DB6-DB3 A 4-bit binary code to set the gain of the programmable gain block between 0 dB and 15 dB in steps of 1 dB.  
 "0000" is 0 dB and "1111" is 15 dB.  
 DB2 A "0" sets the gain of 3rd stage to 0 dB.  
 A "1" sets the gain of 3rd stage to 16 dB.  
 DB1 A "1" closes the internal switches at the inputs to the 2nd and 3rd stage amplifiers.  
 DB0 Internal use only. Must be set to a "0."

Valid data is available only after the first read from and write to the interface register.

Table I. Gain Setting

DB6	DB5	DB4	DB3	GAIN (dB)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
1	1	1	0	14
1	1	1	1	15

### ANALOG INPUT

Figure 5 shows the ADC analog input. The analog input range is 3 V into an input resistance of typically 15 k $\Omega$ . The designed code transition occurs midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS-3/2 LSBs). The output code is binary with 1 LSB = FS/4096 = 6 V/4096 = 1.46 mV. The ideal input/output transfer function is shown in Figure 6.

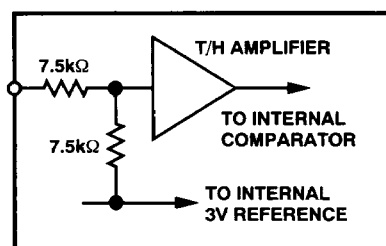


Figure 5. ADC Analog Input

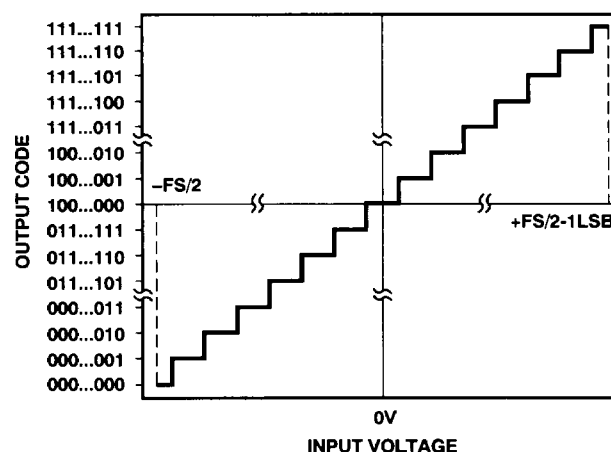


Figure 6. Bipolar Input/Output Transfer Function

**OUTLINE INFORMATION**  
 Dimensions shown in inches and (mm).

P-28A

