SiI9127A/SiI1127A HDMI Receiver with Deep Color Output

Data Sheet

SiI-DS-1059-D

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Contents

Acronyms in This Document 6
1. General Description 7
1.1. Inputs 7
1.2. Digital Video Output 7
1.3. Digital Audio Interface 8
1.4. Consumer Electronic Control 8
1.5. System Applications 8
1.6. Package 8
2. Product Family 9
3. Functional Description 10
3.1. TMDS Digital Cores 10
3.1.1. Active Port Detection and Selection 10
3.2. HDCP Decryption Engine/XOR Mask 11
3.2.1. HDCP Embedded Keys 12
3.3. Data Input and Conversion 12
3.3.1. Mode Control Logic 12
3.3.2. Video Data Conversion and Video Output 12
3.3.3. Deep Color Support 13
3.3.4. xvYCC 13
3.4. 3D Video Formats 13
3.4.1. Automatic Video Configuration 15
3.5. Audio Data Output Logic 15
3.5.1. S/PDIF 15
3.5.2. I^2S 15
3.6. Control and Configuration 16
3.6.1. Register/Configuration Logic 16
3.6.2. I^2C Serial Ports 16
3.6.3. EDID FLASH and RAM Block 17
3.6.4. CEC Interface 17
3.6.5. Standby and HDMI Port Power Supplies 17
4. Electrical Specifications 19
4.1. Absolute Maximum Conditions 19
4.2. Normal Operating Conditions 20
4.3. DC Specifications 21
4.3.1. Digital I/O Specifications 21
4.3.2. DC Power Supply Pin Specifications 22
4.4. AC Specifications 24
4.4.1. Video Output Timings 24
4.4.2. Audio Output Timings 25
4.4.3. Miscellaneous Timings 26
4.4.4. Interrupt Timings 26
5. Timing Diagrams 28
5.1. TMDS Input Timing Diagrams 28
5.2. Power Supply Control Timings 28
5.2.1. Power Supply Sequencing 28
5.3. Reset Timings 29
5.4. Digital Video Output Timing Diagrams 29
5.4.1. Output Transition Times 29
5.4.2. Output Clock to Output Data Delay 30
5.5. Digital Audio Output Timings 30
5.6. Calculating Setup and Hold Times for Video Bus 32
5.6.1. 24/30/36-Bit Mode 32

5.6.2. 12/15/18-Bit Dual-Edge Mode 33
5.7. Calculating Setup and Hold Times for I²S Audio Bus 34
6. Pin Diagram and Descriptions 35
6.1. Pin Diagram 35
6.2. Pin Descriptions 36
6.2.1. Digital Video Output Data Pins 36
6.2.2. Digital Video Output Control Pins 37
6.2.3. Digital Audio Output Pins 37
6.2.4. Configuration/Programming Pins 38
6.2.5. HDMI Control Signal Pins 38
6.2.6. TMDS Differential Signal Pins 39
6.2.7. Power and Ground Pins 39
6.2.8. Reserved and Not Connected Pins 39
7. Video Path 40
7.1. HDMI Input Modes to SiI9127A/SiI1127A Output Modes 41
7.1.1. HDMI RGB 4:4:4 Input Processing 41
7.1.2. HDMI YCbCr/xvYCC 4:4:4 Input Processing 42
7.1.3. HDMI YCbCr/xvYCC 4:2:2 Input Processing 43
7.2. SiI9127A/SiI1127A Output Mode Configuration 44
7.2.1. RGB and YCbCr 4:4:4 Formats with Separate Syncs 45
7.2.2. YC 4:2:2 Formats with Separate Syncs 47
7.2.3. YC 4:2:2 Formats with Embedded Syncs 50
7.2.4. YC Mux (4:2:2) Formats with Separate Syncs 53
7.2.5. YC Mux 4:2:2 Formats with Embedded Syncs 55
7.2.6. 12/15/18-Bit RGB and YCbCr 4:4:4 Formats with Separate Syncs 57
8. I²C Interfaces 59
8.1. HDCP E-DDC / I²C Interface 59
8.2. Local I²C Interface 60
8.3. Video Requirement for I²C Access 60
8.4. I²C Registers 60
9. Design Recommendations 61
9.1. Power Control 61
9.2. Power-on Sequencing 61
9.2.1. Power Pin Current Demands 61
9.3. HDMI Receiver DDC Bus Protection 62
9.4. Decoupling Capacitors 62
9.5. ESD Protection 62
9.6. HDMI Receiver Layout 63
9.7. EMI Considerations 64
9.8. Typical Circuit 65
9.8.1. Power Supply Decoupling 65
9.8.2. HDMI Port Connections 66
9.8.3. Digital Video Output Connections 67
9.8.4. Digital Audio Output Connections 68
9.8.5. Control Signal Connections 69
9.9. Layout 70
9.9.1. TMDS Input Port Connections 70
10. Package Information 71
10.1. ePad Requirements 71
10.2. PCB Layout Guidelines 71
10.3. Package Dimensions 72
10.4. Marking Specification 73
10.5. Ordering Information 73
References 74

Standards Documents....74
Standards Groups....74
Lattice Semiconductor Documents....74
Technical Support....74
Revision History....75

Figures

Figure 1.1. Digital Television System Diagram....7
Figure 3.1. Digital Television Receiver Block Diagram....10
Figure 3.2. Functional Block Diagram....11
Figure 3.3. Default Video Processing Path....14
Figure 3.4. I²C Register Domains....16
Figure 3.5. Power Island....18
Figure 4.1. Test Point VCCTP for VCC Noise Tolerance Specification....20
Figure 4.2. Audio Crystal Schematic....25
Figure 4.3. SCDT and CKDT Timing from DE or RXC Inactive/Active....27
Figure 5.1. TMDS Channel-to-Channel Skew Timing....28
Figure 5.2. Power Supply Sequencing....28
Figure 5.3. RESET# Minimum Timings....29
Figure 5.4. Video Digital Output Transition Times....29
Figure 5.5. Receiver Clock-to-Output Delay and Duty Cycle Limits....30
Figure 5.6. I²S Output Timings....30
Figure 5.7. S/PDIF Output Timings....31
Figure 5.8. MCLK Timings....31
Figure 5.9. 24/30/36-Bit Mode Receiver Output Setup and Hold Times....32
Figure 5.10. 12/15/18-Bit Mode Receiver Output Setup and Hold Times....33
Figure 6.1. Pin Diagram....35
Figure 7.1. Receiver Video and Audio Data Processing Paths....40
Figure 7.2. HDMI RGB 4:4:4 Input to Video Output Transformations....41
Figure 7.3. HDMI YCbCr/xvYCC 4:4:4 Input to Video Output Transformations....42
Figure 7.4. HDMI YCbCr/xvYCC 4:2:2 Input to Video Output Transformations....43
Figure 7.5. 4:4:4 Timing Diagram....46
Figure 7.6. YC Timing Diagram....49
Figure 7.7. YC 4:2:2 Embedded Sync Timing Diagram....52
Figure 7.8. YC Mux 4:2:2 Timing Diagram....54
Figure 7.9. YC Mux 4:2:2 Embedded Sync Encoding Timing Diagram....56
Figure 7.10. 18-Bit Output 4:4:4 Timing Diagram....57
Figure 7.11. 15-Bit Output 4:4:4 Timing Diagram....58
Figure 7.12. 12-Bit Output 4:4:4 Timing Diagram....58
Figure 8.1. I²C Byte Read....59
Figure 8.2. I²C Byte Write....59
Figure 8.3. Short Read Sequence....59
Figure 9.1. Decoupling and Bypass Capacitor Placement....62
Figure 9.2. Cut-out Reference Plane Dimensions....63
Figure 9.3. HDMI to Receiver Routing – Top View....64
Figure 9.4. Power Supply Decoupling and PLL Filtering Schematic....65
Figure 9.5. HDMI Port Connections Schematic....66
Figure 9.6. Digital Display Schematic....67
Figure 9.7. Audio Output Schematic....68
Figure 9.8. Controller Connections Schematic....69
Figure 9.9. TMDS Input Signal Assignments....70
Figure 10.1. 128-Pin TQFP Package Diagram....72
Figure 10.2. Marking Diagram of SiI9127A....73
Figure 10.3. Alternate Marking Diagram....73

Tables

Table 2.1. Summary of New Features 9
Table 3.1. Digital Video Output Formats 12
Table 3.2. Supported 3D Video Formats 14
Table 3.3. Default Video Processing 14
Table 3.4. AVI InfoFrame Video Path Details 15
Table 3.5. Digital Output Formats Configurable through Auto Output Format Register 15
Table 3.6. Supported MCLK Frequencies 16
Table 5.1. Calculation of 24/30/36-Bit Output Setup and Hold Times 32
Table 5.2. Calculation of 12/15/18-Bit Output Setup and Hold Times 33
Table 5.3. I^2S Setup and Hold Time Calculations 34
Table 7.1. Translating HDMI Formats to Output Formats 41
Table 7.2. Output Video Formats 44
Table 7.3. 4:4:4 Mappings 45
Table 7.4. YC 4:2:2 Separate Sync Pin Mappings 47
Table 7.5. YC 4:2:2 (Pass Through Only) Separate Sync Pin Mapping 48
Table 7.6. YC 4:2:2 Embedded Sync Pin Mappings 50
Table 7.7. YC 4:2:2 (Pass Through Only) Embedded Sync Pin Mapping 51
Table 7.8. YC Mux 4:2:2 Mappings 53
Table 7.9. YC Mux 4:2:2 Embedded Sync Pin Mapping 55
Table 7.10. 12/15/18-Bit Output 4:4:4 Mappings 57
Table 8.1. Control of the Default I^2C Addresses with the CI2CA Pin 60
Table 9.1. Maximum Power Domain Currents versus Video Mode 61

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ACR	Audio Clock Regeneration
AVI	Auxiliary Video Information
CBUS	Control Bus
CEC	Consumer Electronics Control
CPI	CEC Programming Interface
CPU	Central Processing Unit
CSC	Color Space Converter
DDC	Display Data Channel
DSC	Display Stream Compression
DSD	Direct-Stream Digital
DTV	Digital Television
EDDC	Enhanced Display Data Channel
EDID	Extended Display Identification Data
ESD	Electrostatic Discharge
GPIO	General Purpose Input/Output
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound, Integrated Interchip Sound
KSV	Key Selection Vector
NVM	Non Volatile Memory
PCM	Pulse Code Modulation
S/PDIF	Sony/Philips Digital Interface Format
TMDS	Transition Minimized Differential Signaling
TQFP	Thin Quad Flat Pack

1. General Description

The SiI9127A/SiI1127A HDMI® Receiver with Deep Color Outputs from Lattice Semiconductor Corporation is a 2-port receiver that allows DTVs that can display 10/12-bit color depth to provide the highest quality protected digital audio and video over a single cable. The SiI9127A/SiI1127A receiver can receive Deep Color video up to 12-bit, 1080p at 60 Hz. Efficient color space conversion receives RGB or YCbCr video data and sends either standard-definition or high-definition RGB or YCbCr formats.

The SiI9127A/SiI1127A receiver supports the extended gamut YCC or xvYCC color space described in the IEC 61966-2-4 Specification, which supports approximately 1.8 times the number of colors as the RGB color space. The xvYCC color space also makes full use of the range provided by the standard 8-bit resolution per pixel format.

The SiI9127A receiver is preprogrammed with High-bandwidth Digital Content Protection (HDCP) keys and contains an integrated HDCP decryption engine for receiving protected audio and video content. This set of keys helps reduce programming overhead, lowers manufacturing costs, and provides the highest level of security.

The SiI1127A receiver is functionally equivalent to the SiI9127A receiver except that the HDCP keys are not preprogrammed, therefore SiI1127A does not support HDCP decryption.

An integrated Extended Display Identification Data (EDID) block stored in non-volatile memory (NVM) can be programmed at the time of manufacture using the local I^2C bus. On-board RAM can also be loaded through the I^2C bus with EDID data from the system microcontroller during initialization if the EDID content of the NVM is not used.

The EDID is reflected on the two HDMI ports through the DDC bus. The device allows different EDID formats to be mixed in an application. Having the flexibility to provide EDID content from the sources described above or from external ROM can eliminate up to two EDID ROMs and save board space.

Flexible power management provides extremely low standby power consumption. Standby power can be supplied from an HDMI 5 V signal or from a separate standby power pin. If the NVM stores the EDID, only the 5 V power from the source device is needed to read the EDID.

1.1. Inputs

- Two HDMI/DVI-compatible ports
- The TMDS™ core runs at 25 MHz–225 MHz
- Dynamic cable equalization automatically detects the equalization required for the incoming signal

1.2. Digital Video Output

- xvYCC to extended RGB
- 36-bit RGB/YCbCr 4:4:4
- 16/20/24-bit YCbCr 4:2:2
- 8/10/12-bit YCbCr 4:2:2 (ITU BT.656)
- True 12-bit accurate output data using an internal 14-bit wide processing path
- Drive strength is programmable from 2 mA to 14 mA

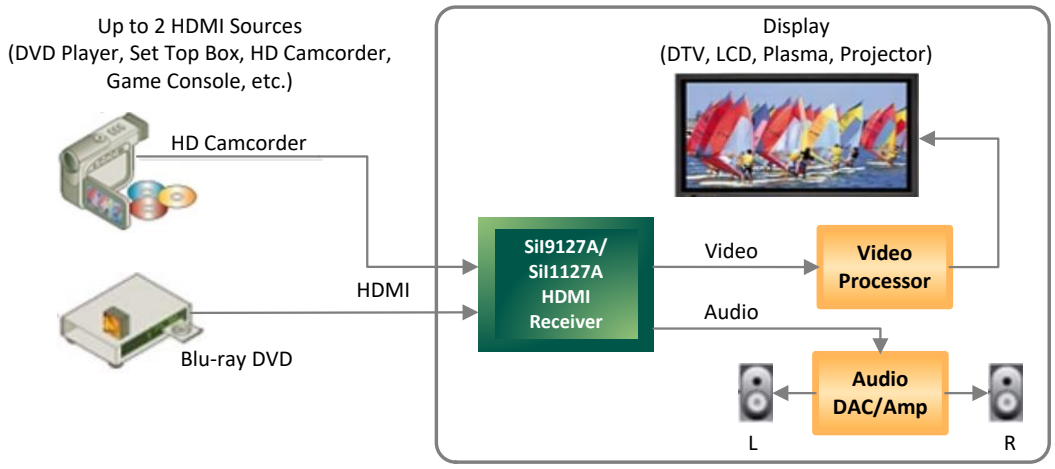


Figure 1.1. Digital Television System Diagram

1.3. Digital Audio Interface

- Sends and receives up to two channels of uncompressed digital audio at the rate of 192 kHz.
- I^2S output with one data signal for stereo formats
- S/PDIF output supports PCM, Dolby Digital, DTS digital audio transmission with a 32 kHz–192 kHz Fs sample rate
- Intelligent audio mute capability avoids pops and noise with automatic soft mute and unmute
- IEC60958 or IEC61937 compatible

1.4. Consumer Electronic Control

- Consumer Electronics Control (CEC) interface incorporates an HDMI CEC I/O
- An integrated CEC Programming Interface (CPI) relieves the burden of the microcontroller having to write low-level commands
- Automatic Feature Abort response for unsupported commands
- Automatic Message Retry on transmit

1.5. System Applications

The SiI9127A/SiI1127A receiver is designed for digital televisions that require support for HDMI Deep Color. The device allows receipt of 10/12-bit color depth up to 1080p resolutions. A single receiver chip provides two HDMI input ports. The video output interfaces to a video processor and the audio output can interface directly to an audio DAC or an audio DSP for further processing as shown in Figure 3.1.

1.6. Package

14 mm × 14 mm 128-pin TQFP package with an exposed pad (ePad).

2. Product Family

Table 2.1 summarizes the functional differences among the SiI9127A/SiI1127A, SiI9125, SiI9135A, SiI9223A and the SiI9233A receivers.

Table 2.1. Summary of New Features

Feature	SiI9125	SiI9127A/SiI1127A	SiI9135A	SiI9223A	SiI9233A
HDMI Input Connections					
TMDS Input Ports	2	2	2	4	4
Color Depth	8/10/12-bit	8/10/12-bit	8/10/12-bit	8/10/12-bit	8/10/12-bit
DDC Input Ports	2	2	2	4	4
Maximum TMDS Input Clock	225 MHz	225 MHz	225 MHz	225 MHz	225 MHz
Video Output					
Digital Video Output Ports	1	1	1	1	1
Maximum Output Pixel Clock	165 MHz	165 MHz	165 MHz	165 MHz	165 MHz
Maximum Output Bus Width	36	36	36	36	36
Audio Formats					
S/PDIF Output Ports	1	1	1	1	1
I²S Output	2 channel	2 channel	8 channel	2 channel	8 channel
DSD Output	2 channel	NA	6 channel	NA	8 channel
High Bit Rate Audio Support Compressed DTS-HD and Dolby True-HD	No	No	Yes	No	Yes
Maximum Audio Sample Rate (Fs)	192 kHz	192 kHz	192 kHz	192 kHz	192 kHz
Video Processing					
Color Space Converter	RGB to/from YCbCr	RGB to/from YCbCr xvYCC to RGB	RGB to/from YCbCr	RGB to/from YCbCr xvYCC to RGB	RGB to/from YCbCr xvYCC to RGB
Pixel Clock Divider	÷ 4, ÷ 2	÷ 4, ÷ 2	÷ 4, ÷ 2	÷ 4, ÷ 2	÷ 4, ÷ 2
Digital Video Bus Mapping	swap Cb, Cr pins	swap Cb, Cr pins	swap Cb, Cr pins	swap Cb, Cr pins	swap Cb, Cr pins
Other Features					
Local fixed I²C Device Address[1]	0x60/0x68 or 0x62/0x6A	0x60/0x68 or 0x62/0x6A	0x60/0x68 or 0x62/0x6A	0x60/0x68 or 0x62/0x6A	0x60/0x68 or 0x62/0x6A
Programmable I²C Device Address[1]	NA	0x64, 0xC0, 0xE0	NA	0x64, 0xC0, 0xE0	0x64, 0xC0, 0xE0
Reserved I²C Device Address[2]	NA	0x90, 0xD0, 0xE6	NA	0x90, 0xD0, 0xE6	0x90, 0xD0, 0xE6
3D Support	No	Yes	No	Yes	Yes
CEC	No	Yes	No	Yes	Yes
EDID	No	NVRAM	No	NVRAM	NVRAM
HDCP Repeater Support	No	No	Yes	No	Yes
Interlaced Format Detection Pin	Yes	Yes	Yes	Yes	Yes
Package	144-pin TQFP ePad	128-pin TQFP ePad	144-pin TQFP ePad	144-pin TQFP ePad	144-pin TQFP ePad

Notes:

1. Refer to the SiI9223A/SiI9233A/SiI9127A/SiI1127A HDMI Receivers Programmer Reference for a description of these I²C register addresses.
2. These are reserved I²C register addresses which are within the I²C register address map of the chip. Do not access these registers on the chip and do not use these addresses for other devices, in the system which use the same I²C bus.

3. Functional Description

The SiI9127A/SiI1127A receiver provides a complete solution for receiving HDMI-compliant digital audio and video. Specialized audio and video processing is available within the receiver to add HDMI capability to consumer electronics such as DTVs. Figure 3.1 shows the SiI9127A/SiI1127A receiver incorporated into a digital television reciever. Figure 3.2 on the next page shows the functional blocks of the chip. The receiver supports two HDMI input ports. Only one port can be active at any time.

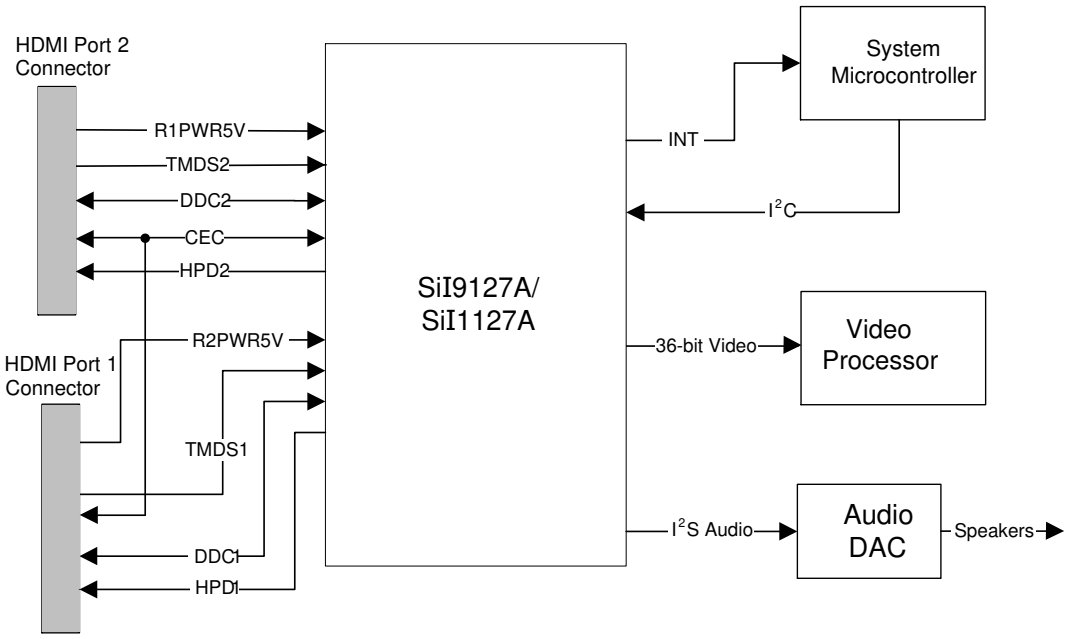


Figure 3.1. Digital Television Receiver Block Diagram

3.1. TMDS Digital Cores

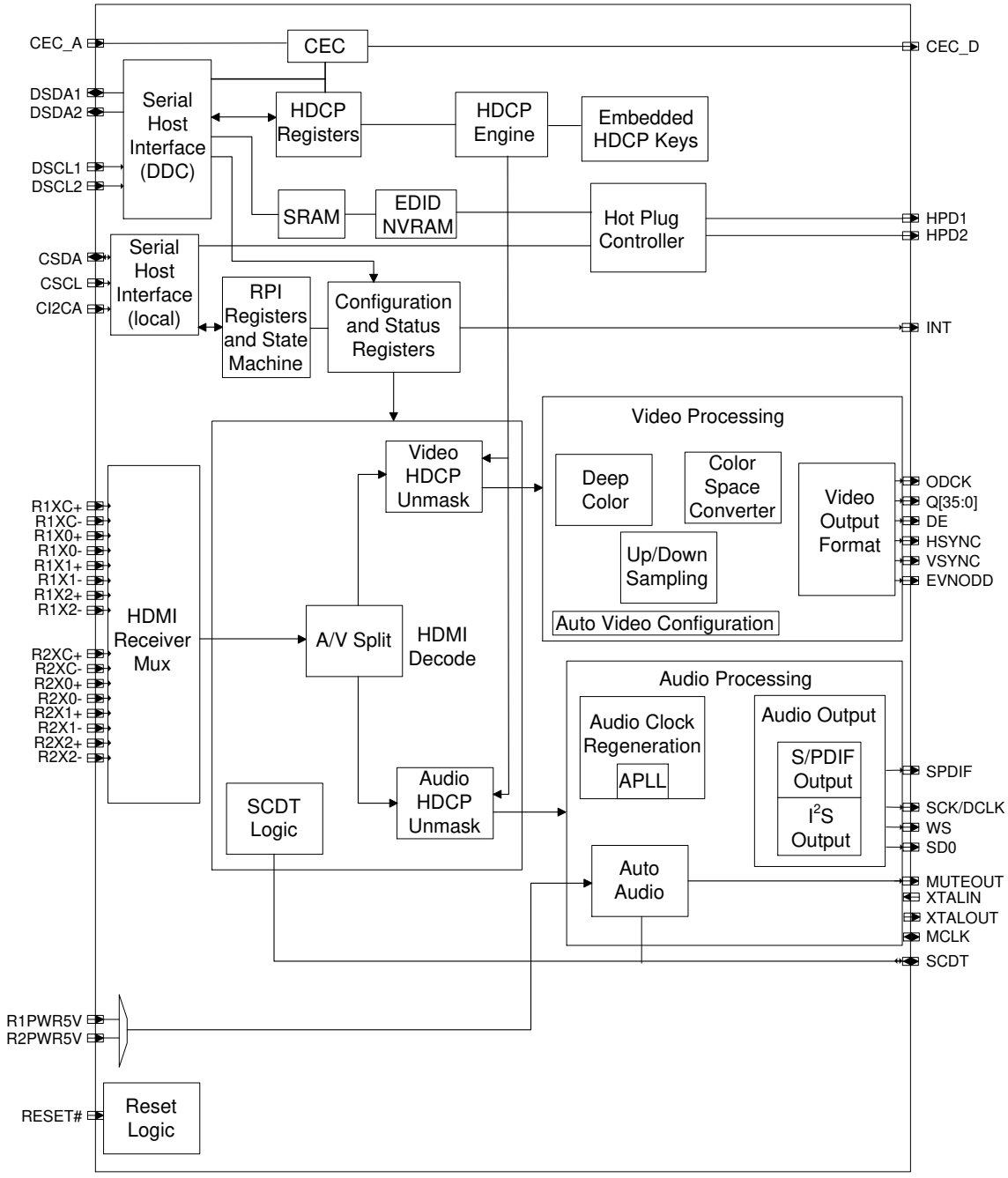
The TMDS digital core is the latest generation core that supports HDMI and the ability to carry 10/12-bit color depth. The core can receive TMDS data at up to 225 MHz. Each core performs 10-to-8 bit TMDS decoding on the video data and 10-to-4 bit TMDS decoding on the audio data received from the three TMDS differential data lines along with a TMDS differential clock. The TMDS core can sense a stopped clock or stopped video and software can put the receiver into power-down mode.

3.1.1. Active Port Detection and Selection

Only one port can be active at a time, under control of the receiver firmware. Active TMDS signaling can arrive at both ports, but only one has internal circuitry enabled. The firmware in the display controls these states using register settings.

Other control signals are associated with the TMDS signals on each HDMI port. The receiver can monitor the +5 V supply from each attached host. The firmware can poll registers to check which ports are connected. The firmware also controls functional connection to one of the two E-DDC buses, enabling one while disabling the other. An attached host determines the active status of an attached HDMI device by polling the E-DDC bus to the device.

Refer to the SiI-PR-1033 Programmer Reference (see Lattice Semiconductor Documents on page 74) for a complete description of port detection and selection. *The Programmer's Reference requires an NDA with Lattice Semiconductor.*



Note: HDCP blocks do not apply to the SiI1127A receiver.

Figure 3.2. Functional Block Diagram

3.2. HDCP Decryption Engine/XOR Mask

The HDCP decryption engine contains all the necessary logic to decrypt the incoming audio and video data. The decryption process is entirely controlled by the host-side microcontroller/microprocessor through a set sequence of register reads and writes through the DDC channel. Preprogrammed HDCP keys and Key Selection Vector (KSV) stored in the on-chip non-volatile memory are used in the decryption process. A resulting calculated value is applied to an XOR mask during each clock cycle to decrypt the audio and video data.

3.2.1. HDCP Embedded Keys

The SiI9127A receiver comes preprogrammed with a set of production HDCP keys stored on-chip in non-volatile memory. System manufacturers do not need to purchase key sets from the Digital Content Protection LLC. All purchasing, programming, and security for the HDCP keys is handled by Lattice Semiconductor. The preprogrammed HDCP keys provide the highest level of security, as keys cannot be read out of the device after they are programmed. Before receiving samples of the receiver, customers must sign the HDCP license agreement available from Digital Content Protection, LLC, or have a special NDA with Lattice Semiconductor.

The SiI1127A receiver does not come preprogrammed with a set of production HDCP keys stored on-chip in non-volatile memory.

3.3. Data Input and Conversion

3.3.1. Mode Control Logic

The mode control logic determines if the decrypted data is video, audio, or auxiliary information, and directs it to the appropriate logic block.

3.3.2. Video Data Conversion and Video Output

The SiI9127A/SiI1127A receiver can output video in many different formats (see the examples in Table 3.1) and can process the video data before it is sent, as shown in Figure 3.3. It is possible to bypass each of the processing blocks by setting the appropriate register bits.

Table 3.1. Digital Video Output Formats

Color Space	Video Format	Bus Width	HSYNC/ VSYNC	Output Clock (MHz)								Notes
				480i/576i[2, 3]	480p	XGA	720p	1080i	SXGA	1080p	UXGA	
RGB	4:4:4	36	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		30	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		24	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		12/15/18	Separate	27	27	65	74.25	74.25	—	—	—	4
YCbCr	4:4:4	36	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		30	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		24	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		12/15/18	Separate	27	27	65	74.25	74.25	—	—	—	4
	4:2:2	16/20/24	Separate	27	27	—	74.25	74.25	—	148.5	162	—
		16/20/24	Embedded	27	27	—	74.25	74.25	—	148.5	162	1
		8/10/12	Separate	27	54	—	148.5	148.5	—	—	—	—
		8/10/12	Embedded	27	54	—	148.5	148.5	—	—	—	1

Notes:

1. Embedded syncs use SAV/EAV coding.
2. 480i and 576i modes can output a 13.25 MHz clock using the internal clock divider.
3. Output clock frequency depends on programming of internal registers. Differential TMDS clock is always 25 MHz or faster.
4. Output clock supports 12/15/18-bit mode by using both edges.

Color Range Scaling

The color range depends on the video format, according to the CEA-861D specification. In some applications the 8-bit input range uses the entire span of 0x00 (0) to 0xFF (255) values. In other applications the range is scaled narrower. The receiver cannot detect the incoming video data range and there is no required range specification in the HDMI AVI packet. The device chooses scaling depending on the detected video format. 10 and 12-bit color range scaling are both handled the same way. Refer to the SiI-PR-1033 Programmer Reference for more details.

When the receiver outputs embedded syncs (SAV/EAV codes), it also limits the YCbCr data output values to 1 to 254.

Up Sample/Down Sample

Additional logic can convert from 4:2:2 to 4:4:4 (8/10/12-bit) or from 4:4:4 (8/10/12-bit) to 4:2:2 YCbCr format. All processing is done with 14 bits of accuracy for true 12-bit data.

3.3.3. Deep Color Support

The HDMI 1.3 Specification introduces Color Depth modes greater than 24 bits, known as Deep Color modes, to the HDMI system architecture. The Deep Color modes employ a new pixel packing scheme to enable the extra bits of higher color depth data to be carried over the existing TMDS data encoding scheme. Currently, three Deep Color modes are defined: 30-bit, 36-bit, and 48-bit. The SiI9127A/SiI1127A receiver supports two of these three Deep Color modes; 30-bit, and 36-bit modes. In addition, each Deep Color mode is supported up to 1080p HD format.

For Deep Color modes, the TMDS clock is run faster than the pixel clock in order to create extra bandwidth for the additional bits of the higher color depth data. The increase in the TMDS clock is by the ratio of the pixel size to 24 bits, as follows:

- 30-bit mode: TMDS clock = 1.25x pixel clock (5:4)
- 36-bit mode: TMDS clock = 1.5x pixel clock (3:2)

Because the receiver supports 36-bit mode at 1080p, the highest TMDS clock rate it supports is therefore 225 MHz. When in Deep Color mode, the transmitter periodically sends a General Control Packet with the current color depth and pixel packing phase information to the receiver. The receiver captures the color depth information in a register, which the firmware can then use to set the appropriate clock divider to recover the pixel clock and data.

3.3.4. xvYCC

The SiI9127A/SiI1127A receiver adds support for the extended gamut xvYCC color space; this extended format has roughly 1.8 times more colors than the RGB color space. The use of the xvYCC color space is made possible because of the availability of LED and laser based light sources for the next generation displays. This format also makes use of the full range of values 1 to 254 in an 8-bit space instead of 16 to 235 in the RGB format. The use of xvYCC along with Deep Color helps in reducing color banding and allows display of a larger range of colors than is currently possible.

3.3.4.1. Color Space Conversion

Color space converter (CSC) blocks are provided to convert RGB data to Standard-Definition (ITU.601) or High-Definition (ITU.709) YCbCr formats, and vice-versa. To support the latest extended-gamut xvYCC displays, the SiI9127A/SiI1127A receiver implements color space converter blocks to convert RGB data to extended-gamut Standard-Definition (ITU.601) or High-Definition (ITU.709) xvYCC formats, and vice-versa.

RGB to YCbCr

The RGB→YCbCr color space converter (CSC) can convert from video data RGB to standard definition (ITU.601) or to high definition (ITU.709) YCbCr formats. The HDMI AVI packet defines the color space of the incoming video.

YCbCr to RGB

The YCbCr→RGB color space converter is available to interface to MPEG decoders with RGB-only inputs. The CSC can convert from YCbCr in standard-definition (ITU.601) or high-definition (ITU.709) to RGB.

3.4. 3D Video Formats

The SiI9127A/SiI1127A receiver has support for the 3D video modes described in the HDMI 1.4 Specification. All modes support RGB 4:4:4, YCbCr 4:4:4, and YCbCr 4:2:2 color formats and 8-, 10-, and 12-bit data width per color component. Table 3.2 on the next page shows only the maximum possible resolution with a given frame rate; for example, Side-by-Side (Half) mode is defined for 1080p60, which implies that 720p60 and 480p60 are also supported. Furthermore, a frame rate of 24 Hz also means that a frame rate of 23.98 Hz is supported and a frame rate of 60 Hz also means a frame rate of 59.94 Hz is supported. The input pixel clock changes accordingly.

When using Side-by-Side formats the use of 4:2:2 to 4:4:4 up-sampling and 4:4:4 to 4:2:2 down-sampling should not be enabled as it may result in visible artifacts.

Video processing should be bypassed in the case of L + depth format.

Table 3.2. Supported 3D Video Formats

3D Format	Extended Definition	Resolution	Frame Rate (Hz)	Input Pixel Clock (MHz)
Frame Packing	—	1080p	24	148.5
		720p	50 / 60	
	interlaced	1080i	50 / 60	
L + depth	—	1080p	24	
		720p	50 / 60	
Side-by-Side	full	1080p	24	
		720p	50 / 60	
	half	1080p	50 / 60	
		1080i	50 / 60	74.25

Default Video Configuration

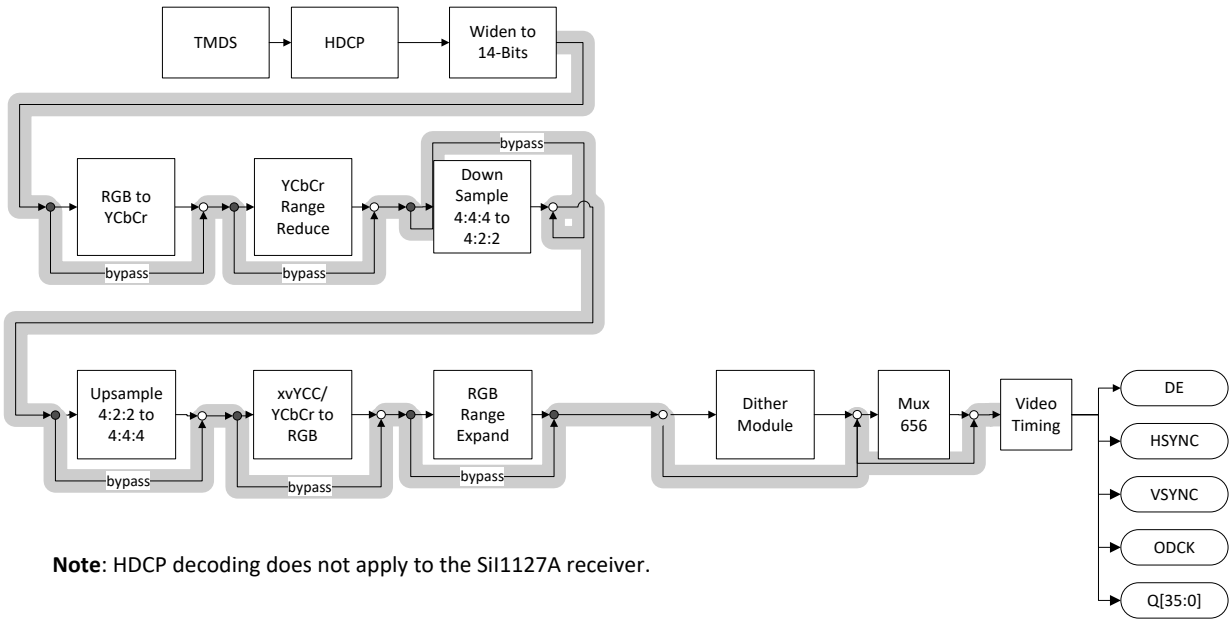
After hardware reset, the SiI9127A/SiI1127A chip is configured in its default mode. This mode is summarized in Table 3.3. For more details and for a complete register listing, refer to the SiI-PR-1033 Programmer Reference.

Table 3.3. Default Video Processing

Video Control	Default after Hardware Reset
HDCP Decryption	HDCP decryption is OFF
Color Space Conversion	No color space conversion
Color Space Selection	BT.601 selected
Color Range Scaling	No range scaling
Upsampling/Downsampling	No upsampling or downsampling
HSYNC & VSYNC Timing	No inversions of HSYNC or VSYNC
Data Bit Width	Uses 8-bit data
Pixel Clock Replication	No pixel clock replication
Power Down	Everything is powered down

Notes:

1. The receiver assumes DVI mode after reset, which is RGB 24-bit 4:4:4 video with a range of 0–255.
2. HDCP decryption is not supported on the SiI1127A receiver.



Note: HDCP decoding does not apply to the SiI1127A receiver.

Figure 3.3. Default Video Processing Path

3.4.1. Automatic Video Configuration

The SiI9127A/SiI1127A receiver adds automatic video configuration to simplify the firmware task of updating the video path whenever the incoming video changes format. Bits in the HDMI Auxiliary Video Information (AVI) InfoFrame are used to reprogram the registers in the video path.

Table 3.4. AVI InfoFrame Video Path Details

AVI Byte 1 Bits [6:5]		AVI Byte 2 Bits [7:6]		AVI Byte 5 Bits [3:0]	
Y[1:0]	**Color Space**	**C[1:0]**	**Colorimetric**	**PR[3:0]**	**Pixel Repetition**
00	RGB 4:4:4	00	No Data	0000	No repetition
01	YCbCr 4:2:2	01	ITU 601	0001	Pixel sent 2 times
10	YCbCr 4:4:4	10	ITU 709	0010	Pixel sent 3 times
11	Future	11	Extended Colorimetry Information Valid	0011	Pixel sent 4 times
				0100	Pixel sent 5 times
				0101	Pixel sent 6 times
				0110	Pixel sent 7 times
				0111	Pixel sent 8 times
				1000	Pixel sent 9 times
				1001	Pixel sent 10 times

Notes:

1. The Auto Video Configuration assumes that the AVI information is accurate. If information is not available, then the receiver must choose the video path based on measurement of the incoming resolution.
2. Refer to EIA/CEA-861D Specification for details.
3. The SiI9127A/SiI1127A device can support only pixel replication modes 0b0000, 0b0001, and 0b0011. Other modes are unsupported and can result in an unpredictable behavior.

The format of the digital video output bus can be automatically configured to many different formats by programming the Auto Output Format Register. The available formats are listed in Table 3.5. For detailed definitions of how to set this register, refer to the SiI-PR-1033 Programmer Reference.

Table 3.5. Digital Output Formats Configurable through Auto Output Format Register

Digital Output Formats			
Color	**Width**	**MUX**	**Sync**
RGB	4:4:4	N	Separate
YCbCr	4:4:4	N	Separate
YCbCr	4:2:2	N	Separate
YCbCr	4:2:2	Y	Separate
YCbCr	4:2:2	Y	Embedded

3.5. Audio Data Output Logic

The SiI9127A/SiI1127A receiver can send digital audio over S/PDIF and two-channel I^2S outputs.

3.5.1. S/PDIF

The S/PDIF stream can carry 2-channel uncompressed PCM data (IEC 60958). The audio data output logic forms the audio data output stream from the decoded HDMI audio packets. The S/PDIF output supports audio sampling rates from 32 kHz to 192 kHz. A separate master clock output (MCLK), coherent with the S/PDIF output, is provided for time-stamping purposes. *Coherent* means that the MCLK and S/PDIF are created from the same clock source.

3.5.2. I^2S

The I^2S bus format is programmable through registers, to allow interfacing with I^2S audio DACs or audio DSPs with I^2S inputs. Refer to the SiI-PR-1033 Programmer Reference for the different options on the I^2S bus. Additionally, the MCLK (audio master clock) frequency is selectable to be an integer multiple of the audio sample rate F_s.

MCLK frequencies support various audio sample rates as shown in Table 3.6 on the next page.

Table 3.6. Supported MCLK Frequencies

Multiple of Fs	Audio Sample Rate, Fs: I²S and S/PDIF Supported Rates						
	32 kHz	44.1 kHz	48 kHz	88.2 kHz	96 kHz	176.4 kHz	192 kHz
128	4.096 MHz	5.645 MHz	6.144 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz
192	6.144 MHz	8.467 MHz	9.216 MHz	16.934 MHz	18.432 MHz	33.868 MHz	36.864 MHz
256	8.192 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz
384	12.288 MHz	16.934 MHz	18.432 MHz	33.864 MHz	36.864 MHz		
512	16.384 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz		

3.6. Control and Configuration

3.6.1. Register/Configuration Logic

The Register/Configuration Logic block incorporates all the registers required for configuring and managing the features of the SiI9127A/SiI1127A receiver. These registers are used to perform HDCP authentication; audio, video, or auxiliary format processing; CEA-861B InfoFrame Packet format; and power-down control.

The registers are accessible from one of the two serial ports. The first port is the DDC port, which is connected through the HDMI cable to the HDMI host. It is used to control the receiver from the host system for HDCP operation. The second port is the local I²C port, which is used to control the receiver from the display system. This is shown in Figure 3.4. The Local Bus accesses the General Registers and the Common Registers. The DDC Bus accesses the HDCP Operation registers and the Common Registers. The HDCP Operation registers are not applicable to the SiI1127A receiver.

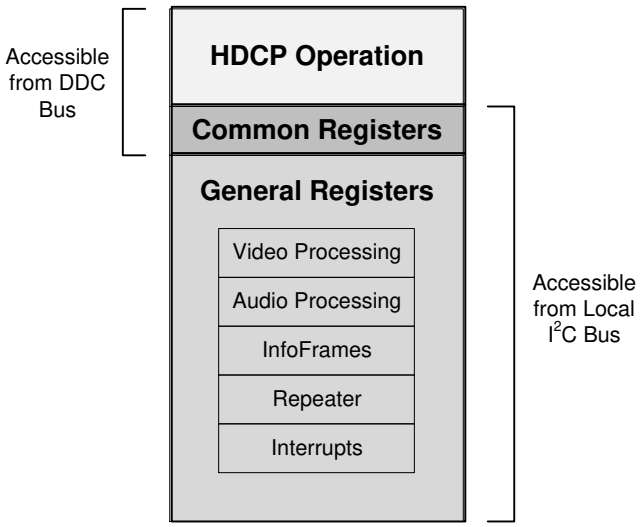


Figure 3.4. I²C Register Domains

3.6.2. I²C Serial Ports

The SiI9127A/SiI1127A receiver provides three I²C serial interfaces: two DDC ports to communicate back to the HDMI or DVI hosts, along with one I²C port for initialization and control by a local microcontroller in the display. Each interface is 5 V tolerant.

E-DDC Bus Interface to HDMI Host

The two DDC interfaces, DSDA1-2 and DSCL1-2, on the receiver are slave interfaces that can run up to 100 kHz. Each interface is connected to one E-DDC bus and is used for reading the integrated EDID in addition to HDCP authentication.

The SiI9127A/SiI1127A receiver is accessible on the E-DDC bus at device addresses 0xA0 for the EDID, and 0x74 for HDCP control. This feature complies with the HDCP Specification.

3.6.3. EDID FLASH and RAM Block

The EDID block consists of 512 bytes of RAM. Each port has a block of 256 bytes of RAM for EDID data. This feature allows simultaneous reads of both ports from two different source devices that are connected to the SiI9127A/SiI1127A device.

In addition to the RAM, the EDID block contains 256 bytes of FLASH that is shared by both ports. As a result, the timing information must be identical between both ports if the internal EDID is used. An additional area of FLASH contains unique CEC physical address and checksum values for each of the ports. This feature allows simultaneous reads of both ports from two different source devices if they are connected and attempt an EDID read at the same time. If independent EDIDs are required on any of the ports, a CPU can externally load the 256 bytes of RAM for that port, by using the local I^2C bus.

The internal EDID can be selected on a per-port basis using registers on the local I^2C bus. For example, Port 1 can use the internal EDID, and Port 2 can use a discrete EEPROM for the EDID.

3.6.4. CEC Interface

The Consumer Electronics Control (CEC) Interface block provides CEC electrically compliant signals between CEC devices and a CEC master. It allows products to meet the electrical specifications of CEC signaling by translating the LVTTL signals of an external microcontroller (CEC host-side or transmit-side) to CEC signaling levels for CEC devices at the receive side, and vice versa.

Additionally, a CEC controller compatible with the Lattice Semiconductor CEC Programming Interface (CPI) is included on-chip. This CEC controller has a high-level register interface accessible through the I^2C interface which can be used to send and receive CEC commands. This controller makes CEC control very easy and straightforward, and removes the burden of having a host CPU perform these low-level transactions on the CEC bus. As a result, CEC pass-through mode is neither required nor supported.

I^2C Interface to Display Controller

The Controller I^2C interface (CSDA, CSCL) on the SiI9127A/SiI1127A receiver is a slave interface capable of running up to 400 kHz. This bus is used to configure the chip by reading or writing to the appropriate registers. It is accessible on the local I^2C bus at two device addresses. Refer to the SiI-PR-1033 Programmer Reference for more information.

3.6.5. Standby and HDMI Port Power Supplies

The receiver incorporates a power island that continues to supply power to the EDID memory, the DDC ports, and the CEC bus when power is removed from the VCC pins, as long as power continues to be provided through at least one connected HDMI cable or by system standby power. Refer to Figure 3.5 on the next page. The internal power multiplexer selects power from either SBVCC5, if it is available, or from one of the R*n*PWR5V pins.

The power island results in an extremely low power standby mode, but allows the EDID to be readable and the CEC controller to be functional. No damage will occur to the device when in this mode.

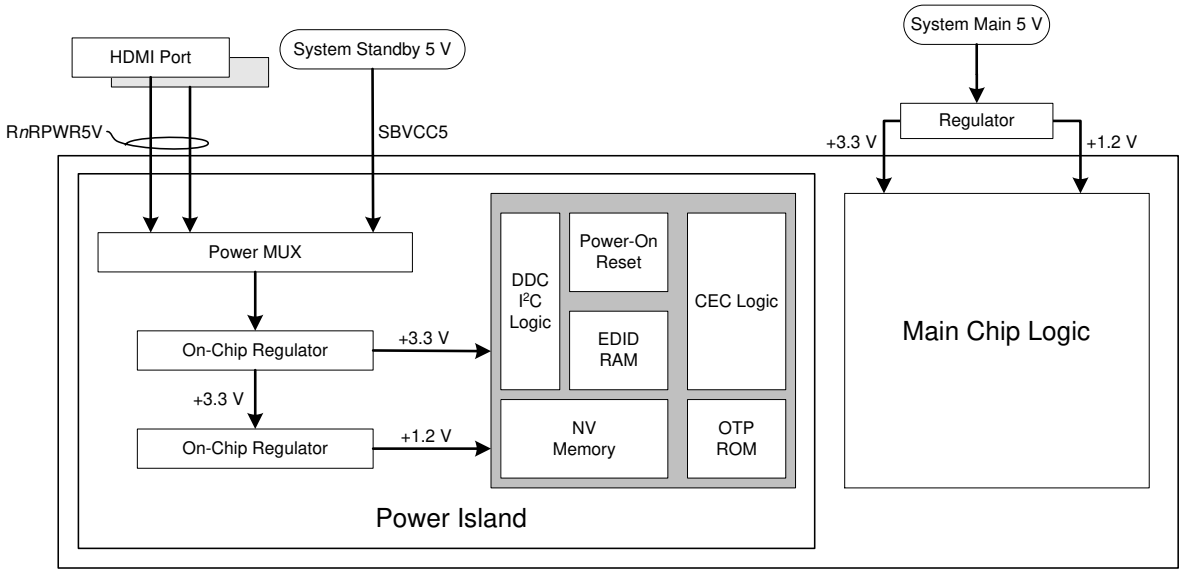


Figure 3.5. Power Island

4. Electrical Specifications

4.1. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC33	I/O Pin Supply Voltage	–0.3	—	4.0	V	1, 2, 3
AVCC12	TMDS Analog Supply Voltage	–0.3	—	1.9	V	1, 2
AVCC33	TMDS Analog Supply Voltage	–0.3	—	4.0	V	1, 2
APVCC12	Audio PLL Supply Voltage	–0.3	—	1.9	V	1, 2
CVCC12	Digital Core Supply Voltage	–0.3	—	1.9	V	1, 2
XTALVCC33	ACR PLL Crystal Oscillator Supply Voltage	–0.3	—	4.0	V	1, 2
SBVCC5	Standby Supply Voltage	–0.3	—	5.7	V	1,2
V_I	Input Voltage	–0.3	—	IOVCC33 + 0.3	V	1, 2
$V_{5V\text{-}Tolerant}$	Input Voltage on 5 V tolerant Pins	–0.3	—	5.5	V	5
T_J	Junction Temperature	—	—	125	°C	—
T_{STG}	Storage Temperature	–65	—	150	°C	—

Notes:

1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described in the Normal Operating Conditions section on page 20.
3. Voltage undershoot or overshoot cannot exceed absolute maximum conditions.
4. Refer to the SiI9127A/SiI1127A receiver Qualification Report for information on ESD performance.
5. All VCC supplies must be available to the device. If the device is not powered and 5 V is applied to these inputs, damage can occur.

4.2. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC33	I/O Pin Supply Voltage	3.13	3.3	3.47	V	1, 4
AVCC12	TMDS Analog Supply Voltage	1.14	1.2	1.26	V	3
AVCC33	TMDS Analog Supply Voltage	3.13	3.3	3.47	V	1, 6
APVCC12	Audio PLL Supply Voltage	1.14	1.2	1.26	V	—
CVCC12	Digital Core Supply Voltage	1.14	1.2	1.26	V	2
XTALVCC33	ACR PLL Crystal Oscillator Supply Voltage	3.13	3.3	3.47	V	4
SBVCC5	Standby Supply Voltage	4.75	5.0	5.25	V	10
R*n*PWR5V	DDC I^2C I/O Reference Voltage	4.7	5.00	5.3	V	11
DIFF33	Difference between two 3.3-V Power Pins	—	—	1.0	V	4
DIFF12	Difference between two 1.2-V Power Pins	—	—	1.0	V	4
DIFF3312	Difference between any 3.3-V and 1.2-V Pin	–1.0	—	2.6	V	4, 5
V_{CCN}	Supply Voltage Noise	—	—	100	mV_{P-P}	7
T_A	Ambient Temperature (with power applied)	0	25	70	°C	—
Θ_{ja}	Ambient Thermal Resistance (Theta JA)	—	—	27	°C/W	—

Notes:

1. IOVCC33 and AVCC33 pins should be controlled from one power source.
2. CVCC12 should be controlled from one power source.
3. AVCC12 pin should be regulated.
4. Power supply sequencing must guarantee that power pins stay within these limits of each other. See Figure 5.2.
5. No 1.2 V pin can be more than DIFF3312[min] higher than any 3.3 V pin. No 3.3 V pin can be more than DIFF3312[max] higher than any 1.2 V pin.
6. The HDMI Specification requires termination voltage (AVCC33) to be controlled to 3.3 V±5%. The SiI9127A/SiI1127A receiver tolerates a wider range of ±300 mV.
7. The supply voltage noise is measured at test point VCCTP in Figure 4.1. The ferrite bead provides filtering of power supply noise. The figure is representative and applies to other VCC pins as well.
8. Airflow at 0 m/s.
9. The schematics on page 65 show decoupling and power supply regulation.
10. SBVCC5V should provide a stable 5 V before any other VCC is applied to the device; see the Power Supply Sequencing section on page 28.
11. Maximum current draw from this source is 50 mA. There is no power-on sequence requirement for this source.

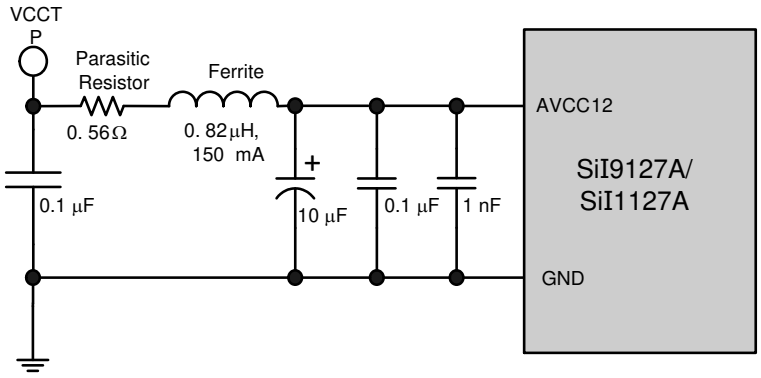


Figure 4.1. Test Point VCCTP for VCC Noise Tolerance Specification

Notes:

1. The Ferrite (0.82 µH, 150 mA) attenuates the PLL power supply noise at 10 kHz and above.
2. The optional parasitic resistor minimizes the peaking. The typical value used here is 0.56 Ω. 1 Ω is the maximum.

4.3. DC Specifications

4.3.1. Digital I/O Specifications

Symbol	Parameter	Pin Type[3]	Conditions[2]	Min	Typ	Max	Units	Note
V_{IH}	HIGH-level Input Voltage	LVTTL	—	2.0	—	—	V	—
V_{IL}	LOW-level Input Voltage	LVTTL	—	—	—	0.8	V	—
V_{TH+}	LOW to HIGH Threshold RESET # Pin	Schmitt	—	1.46	—	—	V	5
V_{TH-}	HIGH to LOW Threshold RESET# Pin	Schmitt	—	—	—	0.96	V	5
DDC V_{TH+}	LOW to HIGH Threshold DSDA0, DSDA1, DSCL0, and DSCL1 pins.	Schmitt	—	3.0	—	—	V	—
DDC V_{TH-}	HIGH to LOW Threshold DSDA0, DSDA1, DSCL0, and DSCL1 pins.	Schmitt	—	—	—	1.5	V	—
Local I^2C V_{TH+}	LOW to HIGH Threshold CSCL and CSDA pins	Schmitt	—	2.1	—	—	V	11, 13
Local I^2C V_{TH-}	HIGH to LOW Threshold CSCL and CSDA pins	Schmitt	—	—	—	0.86	V	11, 13
V_{OH}	HIGH-level Output Voltage	LVTTL	—	2.4	—	—	V	10
V_{OL}	LOW-level Output Voltage	LVTTL	—	—	—	0.4	V	10
I_{OL}	Output Leakage Current	—	High Impedance	–10	—	10	µA	—
V_{ID}	Differential Input Voltage	—	—	75	250	780	mV	4
I_{OD4}	4 mA Digital Output Drive	Output	V_{OUT} = 2.4 V	4	—	—	mA	1, 6, 7
			V_{OUT} = 0.4 V	4	—	—	mA	1, 6, 7
I_{OD8}	8 mA Digital Output Drive	Output	V_{OUT} = 2.4 V	8	—	—	mA	1, 6, 8
			V_{OUT} = 0.4 V	8	—	—	mA	1, 6, 8
I_{OD12}	12 mA Digital Output Drive	Output	V_{OUT} = 2.4 V	12	—	—	mA	1, 6, 9
			V_{OUT} = 0.4 V	12	—	—	mA	1, 6, 9
R_{PD}	Internal Pull Down Resistor	Outputs	IOVCC33 = 3.3 V	25	50	110	kΩ	1, 12
I_{OPD}	Output Pull Down Current	Outputs	IOVCC33 = 3.6 V	—	60	90	µA	1, 12
I_{IPD}	Input Pull Down Current	Input	IOVCC33 = 3.6 V	—	60	90	µA	1

Notes:

1. These limits are guaranteed by design.
2. Under normal operating conditions unless otherwise specified, including output pin loading C_L = 10 pF.
3. See the Pin Descriptions section on page 36 for pin type designations for all package pins.
4. Differential input voltage is a single-ended measurement, according to DVI Specification.
5. Schmitt trigger input pin thresholds V_{TH+} and V_{TH-} correspond to V_{IH} and V_{IL}, respectively.
6. Minimum output drive specified at ambient = 70 °C and IOVCC33 = 3.0 V. Typical output drive specified at ambient = 25 °C and IOVCC33 = 3.3 V. Maximum output drive specified at ambient = 0 °C and IOVCC33 = 3.6 V.
7. I_{OD4} Output applies to pins SPDIF, SCK, WS, SD[3:0], DCLK, INT, and CSDA.
8. I_{OD8} Output applies to pins DE, HSYNC, VSYNC, Q[35:0].and MCLK.
9. I_{OD12} Output applies to pin ODCK.
10. Note that the S/PDIF output drives LVTTL levels, not the low-swing levels defined by IEC958.
11. The SCL and SDA pins are not true open-drain buffers. When no VCC is applied to the chip, these pins can continue to draw a small current, and prevent the master IC from communicating with other devices on the I^2C bus. Therefore, do not power-down the SiI9127A/SiI1127A receiver (remove VCC) unless the attached I^2C bus is completely idle.
12. The chip includes an internal pull-down resistor on many of the output pins. When in the high-impedance state, these pins draw a pull- down current according to this specification when the signal is driven HIGH by another source device.
13. With –10% IOVCC33 supply, the HIGH-to-LOW threshold on DDC and I^2C bus is marginal. A –5% tolerance on the IOVCC33 power supply is recommended.

4.3.2. DC Power Supply Pin Specifications

Total Power versus Power-Down Modes

Symbol	Parameter	Mode	Frequency	Typ[3]			Max[4]			Units	Notes
				3.3 V	1.2 V	SBVCC5	3.3 V	1.2 V	SBVCC5		
I_{PDQ3}	Complete Power-Down Current	A	—				65	3	8	mA	1, 6
I_{PDS}	Sleep Power-down Current	B	27 MHz				68	15	8	mA	2, 7
			74.25 MHz				85	19	8	mA	
			150 MHz				74	19	8	mA	
			225 MHz				74	19	8	mA	
I_{STBY}	Standby Current	C	27 MHz				0	0	8	mA	2, 8
			74.25 MHz				0	0	8	mA	
			150 MHz				0	0	8	mA	
			225 MHz				0	0	8	mA	
I_{UNS}	Unselected Current	D	27 MHz	67	111	8	68	119	8	mA	2, 9
			74.25 MHz	70	173	8	72	180	8	mA	
			150 MHz	75	291	8	79	299	8	mA	
			225 MHz	78	313	8	79	315	8	mA	
I_{CCTD}	Full Power Digital Out Current	E	27 MHz	97	112	8	102	121	8	mA	2, 10
			74.25 MHz	158	175	8	167	177	8	mA	
			150 MHz	259	295	8	280	302	8	mA	
			225 MHz	335	321	8	366	326	8	mA	

Notes:

1. Power is not related to input TMDS clock (RxC) frequency because the selected TMDS port is powered down.
2. Power is related to input TMDS clock (RxC) frequency at the selected TMDS port. Only one port can be selected.
3. Typical power specifications measured with supplies at typical normal operating conditions, and a video pattern that combines gray scale, checkerboard and text.
4. Maximum power limits measured with supplies at maximum normal operating conditions, minimum normal operating ambient temperature, and a video pattern with single-pixel vertical lines.
5. Registers are always accessible on local I2C (CSDA/CSCL) without active link clock.
6. Power Down Mode A: Minimum power. Everything is powered off. Host sees no termination of TMDS signals on either TMDS port. I2C access is still available.
7. Power Down Mode B: Powers down TMDS core. CKDT remains enabled and state can be polled in register. Host device can sense TMDS termination.
8. Power Down Mode C: Power off to 3.3 V and 1.2 V supplies. Power on to SBVCC5 standby supply.
9. Power Down Mode D: Monitor SCDT on selected TMDS port with outputs in the high-impedance state. HDCP continues in the selected port, but the output of the receiver can be connected to a shared bus.
10. Digital Functional Mode E: Full operation on one port with digital outputs.

Power Down Mode Definitions

Mode		3.3 V Supply	1.2 V Supply	SBVCC5	Register Bit States				Description
					PDTOT#	PD_TMDS#	PD_AO#	PD_VO#	
A	Power Down	ON	ON	ON	0	1	1	1	Minimum power. Everything is powered off. Host sees no termination of TMDS signals on either TMDS port. I^2C access is still available.
B	Sleep Mode Power	ON	ON	ON	1	0	1	1	Powers down TMDS core. CKDT remains enabled and state can be polled in register. Host device can sense TMDS termination.
C	Standby Power	OFF	OFF	ON	1	1	1	1	Power off to 3.3 V and 1.2 V supplies. Power on to SBVCC5 standby supply.
D	Unselected Power	ON	ON	ON	1	1	0	0	Monitor SCDT on selected TMDS port with outputs in the high-impedance state. HDCP continues in the selected port, but the output of the receiver can be connected to a shared bus.
E	Digital	ON	ON	ON	1	1	1	1	Full operation on one port with digital outputs.

Notes:

1. PD Clks include PD_MCLK#, PD_XTAL#, PD_APLL#, and PD_PCLK# all set to zero.
2. PD Outs include PD_AO#, and PD_VO# all set to zero.
3. Refer to the SiI-PR-1033 Programmer Reference for register bit descriptions. *The Programmer's Reference requires an NDA with Lattice Semiconductor.*

4.4. AC Specifications

TMDS Input Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{DPS}	Intra-Pair Differential Input Skew	—	—	—	T_{BIT}	ps	—	2, 4
T_{CCS}	Channel to Channel Differential Input Skew	—	—	—	T_{CIP}	ns	Figure 5.1	2, 3
F_{RXC}	Differential Input Clock Frequency	—	25	—	225	MHz	—	—
T_{RXC}	Differential Input Clock Period	—	4.44	—	40	ns	—	—
T_{IJIT}	Differential Input Clock Jitter tolerance (0.3 Tbit)	74.25 MHz	—	—	400	ps	—	2, 5, 6

Notes:
1. Under normal operating conditions unless otherwise specified, including output pin loading of C_L = 10 pF.
2. Guaranteed by design.
3. IDCK Period. Refer to the applicable Lattice Semiconductor HDMI Transmitter Data Sheet.
4. 1/10 of IDCK Period. Refer to the applicable Lattice Semiconductor HDMI Transmitter Data Sheet.
5. Jitter as defined by the HDMI Specification.
6. Jitter measured with Clock Recovery Unit per HDMI Specification. Actual jitter tolerance can be higher depending on the frequency of the jitter.

Refer to the SiI-PR-1033 Programmer Reference for more details on controlling timing modes.

4.4.1. Video Output Timings

12/15/18-Bit Data Output Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
D_{LHT}	LOW-to-HIGH Rise Time Transition	C_L = 10 pF	—	—	1.5	ns	Figure 5.4	2
D_{HLT}	HIGH-to-LOW Fall Time Transition	C_L = 10 pF	—	—	1.5	ns	Figure 5.4	2
R_{CIP}	ODCK Cycle Time	C_L = 10 pF	13	—	40	ns	Figure 5.5	8
F_{CIP}	ODCK Frequency	C_L = 10 pF	25	—	82.5	MHz	—	5
T_{DUTY}	ODCK Duty Cycle	C_L = 10 pF	40%	—	60%	R_{CIP}	Figure 5.5	3
T_{CK2OUT}	ODCK-to-Output Delay	C_L = 10 pF	0.6	—	3.8	ns	Figure 5.5	—

16/20/24/30/36-Bit Data Output Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
D_{LHT}	LOW-to-HIGH Rise Time Transition	C_L = 10 pF	—	—	1.5	ns	Figure 5.4	2
D_{HLT}	HIGH-to-LOW Fall Time Transition	C_L = 10 pF	—	—	1.5	ns	Figure 5.4	2
R_{CIP}	ODCK Cycle Time	C_L = 10 pF	—	—	40	ns	Figure 5.5	5, 8
F_{CIP}	ODCK Frequency	C_L = 10 pF	—	—	165	MHz	Figure 5.5	5
T_{DUTY}	ODCK Duty Cycle	C_L = 10 pF	40%	—	60%	R_{CIP}	Figure 5.5	3
T_{CK2OUT}	ODCK-to-Output Delay	C_L = 10 pF	0.4	—	2.5	ns	Figure 5.5	—

Notes:
1. Under normal operating conditions unless otherwise specified, including output pin loading of C_L = 10 pF.
2. Rise time and fall time specifications apply to HSYNC, VSYNC, DE, ODCK, EVNODD and Q[35:0].
3. Output clock duty cycle is independent of the differential input clock duty cycle. Duty cycle is a component of output setup and hold times.
4. See Table 5.2 on page 33 for calculation of worst case output setup and hold times.
5. All output timings are defined at the maximum operating ODCK frequency, F_{CIP}, unless otherwise specified.
6. F_{CIP} can be the same as F_{RXC} or one-half of F_{RXC}, depending on OCLKDIV setting. F_{CIP} can also be F_{RXC} /1.25 or F_{RXC} /1.5 if Deep Color mode is being transmitted.
7. R_{CIP} is the inverse of F_{CIP} and is not a controlling specification.
8. Output skew specified when ODCK is programmed to divide-by-two mode.

4.4.2. Audio Output Timings

I²S Output Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{tr}	SCK Clock Period (TX)	C_L = 10 pF	1.00	—	—	T_{tr}	Figure 5.6	1
T_{HC}	SCK Clock HIGH Time	C_L = 10 pF	0.35	—	—	T_{tr}		1
T_{LC}	SCK Clock LOW Time	C_L = 10 pF	0.35	—	—	T_{tr}		1
T_{SU}	Setup Time, SCK to SD/WS	C_L = 10 pF	$0.4T_{TR} - 5$	—	—	ns		1
T_{HD}	Hold Time, SCK to SD/WS	C_L = 10 pF	$0.4T_{TR} - 5$	—	—	ns		1
$T_{SCKDUTY}$	SCK Duty Cycle	C_L = 10 pF	40%	—	60%	T_{tr}		1
T_{SCK2SD}	SCK to SD or WS Delay	C_L = 10 pF	–5	—	+5	ns		2
T_{AUDDLY}	Audio Pipeline Delay	—	—	40	80	µs	—	—

Notes:
1. Refer to Figure 5.6. Meets timings in Philips I²S Specification.
2. Applies also to SDC-to-WS delay.

S/PDIF Output Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{SPCYC}	S/PDIF Cycle Time	C_L = 10 pF	—	1.0	—	UI	Figure 5.7	1, 2
F_{SPDIF}	S/PDIF Frequency	—	4	—	24	MHz		3
T_{SPDUTY}	S/PDIF Duty Cycle	C_L = 10 pF	90%	—	110%	UI		2, 5
$T_{MCLKCYC}$	MCLK Cycle Time	C_L = 10 pF	20	—	250	ns	Figure 5.8	1, 2, 4
F_{MCLK}	MCLK Frequency	C_L = 10 pF	4	—	50	MHz		1, 2, 4
$T_{MCLKDUTY}$	MCLK Duty Cycle	C_L = 10 pF	40%	—	60%	$T_{MCLKCYC}$		2, 4
T_{AUDDLY}	Audio Pipeline Delay	—	—	40	80	µs	—	—

Notes:
1. Guaranteed by design.
2. Proportional to unit time (UI), according to sample rate.
3. S/PDIF is not a true clock, but is generated from the internal 128Fs clock, for Fs from 128 to 512 kHz.
4. MCLK refers to MCLKOUT.
5. Intrinsic jitter on S/PDIF output can limit its use as an S/PDIF transmitter. The S/PDIF intrinsic jitter is approximately 0.1 UI.

Audio Crystal Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
F_{XTAL}	External Crystal Freq.	—	26	27	28.5	MHz	Figure 4.2

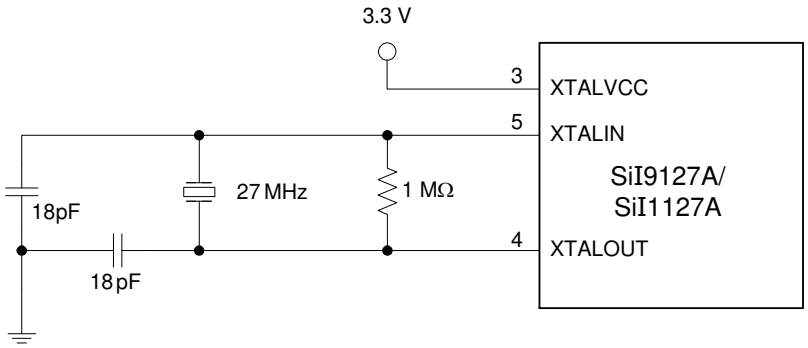


Figure 4.2. Audio Crystal Schematic

4.4.3. Miscellaneous Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{I2CDVD}	SDA Data Valid delay from SCL falling edge	C_L = 400 pF	—	—	700	ns	—	—
F_{DDC}	Speed on TMDS DDC Ports	C_L = 400 pF	—	—	100	kHz	—	2
$F_I{}^2{}_C$	Speed on Local I²C Port	C_L = 400 pF	—	—	400	kHz	—	3
T_{RESET}	RESET# Signal LOW Time for valid reset	—	50	—	—	µs	Figure 5.3	—
$T_{STARTUP}$	Startup time from power supplies valid	—	—	—	100	ms	—	5
$T_{BKSVINIT}$	HDCP BKSV Load Time	—	—	—	2.2	ms	—	4

Notes:

1. Under normal operating conditions unless otherwise specified, including output pin loading of C_L = 10 pF.
2. DDC ports are limited to 100 kHz by the HDMI Specification, and meet I²C standard mode timings.
3. Local I²C port (CSCL/CSDA) meets standard mode I²C timing requirements to 400 kHz.
4. The time required to load the KSV values internal to the receiver after a RESET# and the start of an active TMDS clock. An attached HDCP host device should not attempt to read the receiver BKSV values until after this time. The $T_{BKSVINIT}$ Min and Max values are based on the maximum and minimum allowable XCLK frequencies. The loading of the BKSV values requires a valid XCLK and TMDS clock.
5. $T_{STARTUP}$ is the startup time required for the device to be operational once power is stable. This startup time is due to the on-board voltage regulator for the EDID and CEC and a power-on reset circuit.

4.4.4. Interrupt Timings

Interrupt Output Pin Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{FSC}	Link disabled (DE inactive) to SCDT LOW	—	—	0.15	40	ms	Figure 4.3	1, 2, 3, 8
T_{HSC}	Link enabled (DE active) to SCDT HIGH	—	—	—	4	DE	Figure 4.3	1, 2, 4, 8
T_{CICD}	RXC inactive to CKDT LOW	—	—	—	100	µs	Figure 4.3	1, 2, 8
T_{CACD}	RXC active to CKDT HIGH	—	—	—	10	µs	Figure 4.3	1, 2, 8
T_{INT}	Response Time for INT from Input Change	—	—	—	100	µs	—	1, 5, 8
T_{CIOD}	RXC inactive to ODCK inactive	—	—	—	100	ns	—	1, 8
T_{CAOD}	RXC active to ODCK active and stable	—	—	—	10	ms	—	1, 6, 8
T_{SRRF}	Delay from SCDT rising edge to Software Reset falling edge	—	—	—	100	ms	Figure 5.3	7

Notes:

1. Guaranteed by design.
2. SCDT and CKDT are register bits in this device.
3. SCDT changes to LOW after DE is HIGH for approximately 4096 pixel clock cycles, or after DE is LOW for approximately 1,000,000 clock cycles. At 27 MHz pixel clock, this delay for DE HIGH is approximately 150 µs, and the delay for DE LOW is approximately 40 ms.
4. SCDT changes to HIGH when clock is active (T_{CACD}) and at least 4 DE edges have been recognized. At 720p, the DE period is 22 µs, so SCDT responds approximately 50 µs after T_{CACD}.
5. The INT pin changes state after a change in input condition when the corresponding interrupt is enabled.
6. Output clock (ODCK) becomes active before it becomes stable. Use the SCDT signal as an indicator of stable video output timings, as this depends on decoding of DE signals with active RXC (see T_{FSC}).
7. Software reset must be asserted and then de-asserted within the specified maximum time after rising edge of Sync Detect (SCDT). Access to both SWRST and SCDT can be limited by the speed of the I²C connection.
8. SCDT is HIGH only when CKDT is also HIGH. When the receiver is in a powered-down mode, the INT output pin indicates the current state of SCDT. Thus, a powered-down receiver signals a microcontroller connected to the INT pin whenever SCDT changes from LOW to HIGH or HIGH to LOW.

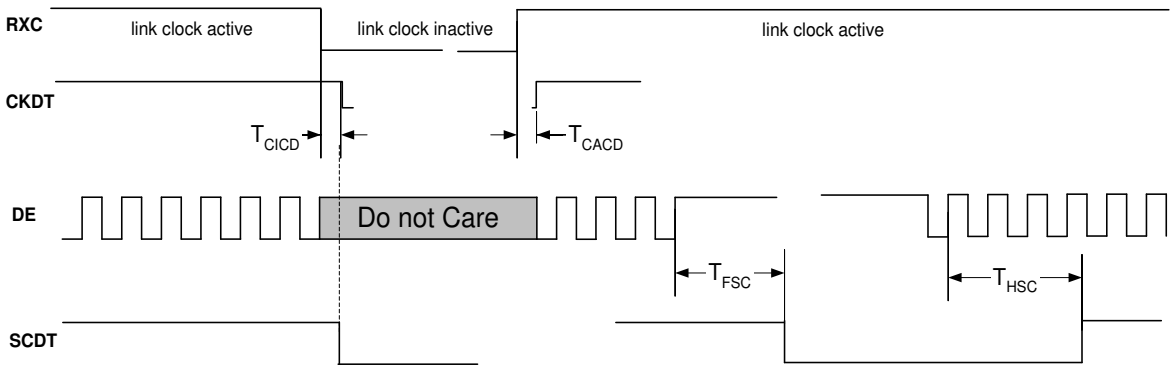


Figure 4.3. SCDT and CKDT Timing from DE or RXC Inactive/Active

Notes:

1. The SCDT shown in Figure 4.3 is a register bit. SCDT remains HIGH if DE is stuck in LOW while RXC remains active, but SCDT changes to LOW if DE is stuck HIGH while RXC remains active.
2. The CKDT shown in Figure 4.3 is a register bit. CKDT changes to LOW whenever RXC stops, and changes to HIGH when RXC starts. SCDT changes to LOW when CKDT changes to LOW.
3. SCDT changes to LOW when CKDT changes to LOW. SCDT changes to HIGH at T_{HSC} after CKDT changes to HIGH.
4. The INT output pin changes state after the SCDT or CKDT register bit is set or cleared if those interrupts are enabled.

Refer to the SiI-PR-1033 Programmer Reference for more details on controlling timing modes. *The Programmer's Reference requires an NDA with Lattice Semiconductor.*

5. Timing Diagrams

5.1. TMDS Input Timing Diagrams

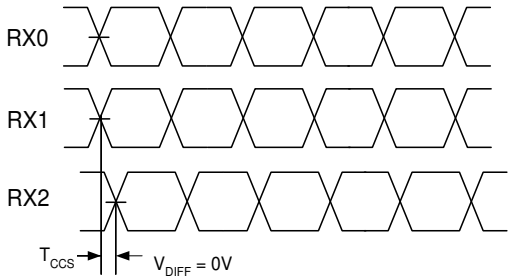
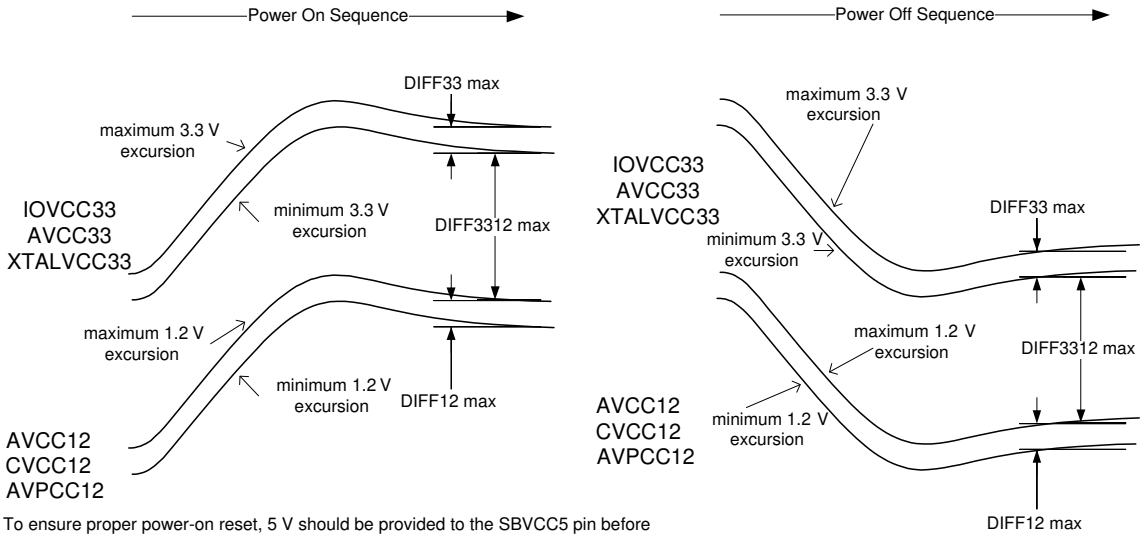


Figure 5.1. TMDS Channel-to-Channel Skew Timing

5.2. Power Supply Control Timings

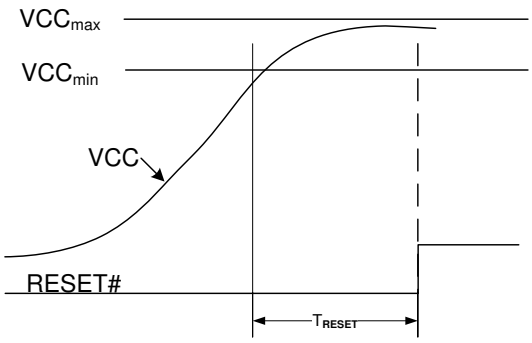
5.2.1. Power Supply Sequencing



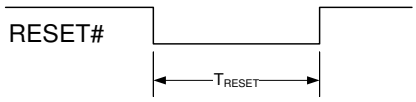
To ensure proper power-on reset, 5 V should be provided to the SBVCC5 pin before the power-on sequence shown here begins.

Figure 5.2. Power Supply Sequencing

5.3. Reset Timings



Note that VCC must be stable between its limits for Normal Operating Conditions for T_{RESET} before RESET# is HIGH.



RESET# must be pulled LOW for T_{RESET} before accessing registers. This can be done by holding RESET# LOW until T_{RESET} after stable power (at left), or by pulling RESET# LOW from a HIGH state (at right) for at least T_{RESET}.

Figure 5.3. RESET# Minimum Timings

5.4. Digital Video Output Timing Diagrams

5.4.1. Output Transition Times

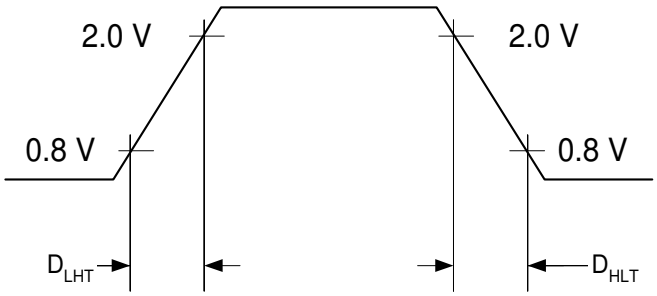


Figure 5.4. Video Digital Output Transition Times

5.4.2. Output Clock to Output Data Delay

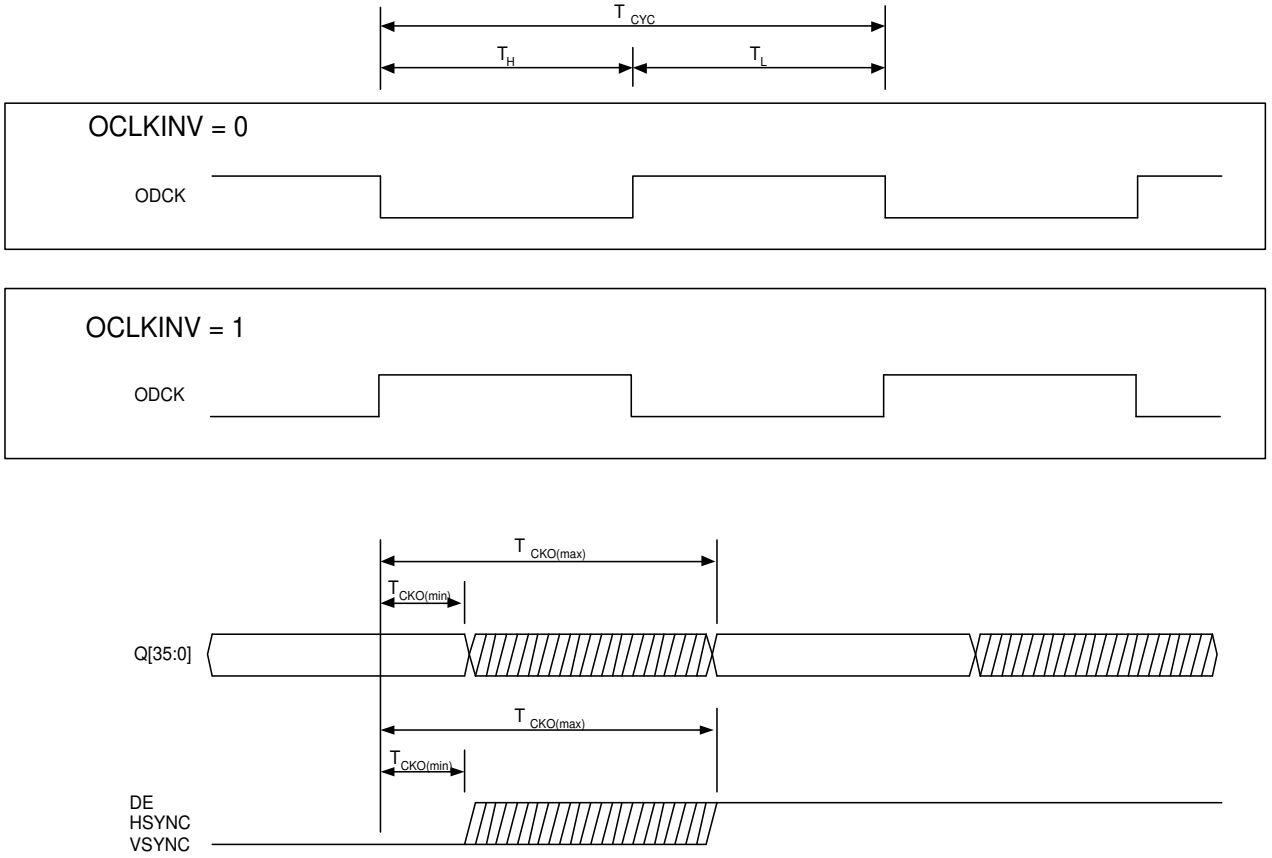


Figure 5.5. Receiver Clock-to-Output Delay and Duty Cycle Limits

5.5. Digital Audio Output Timings

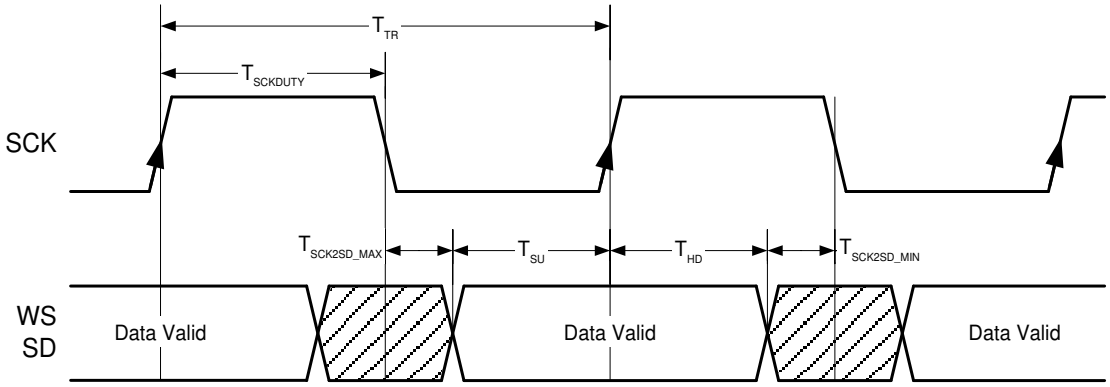


Figure 5.6. I²S Output Timings

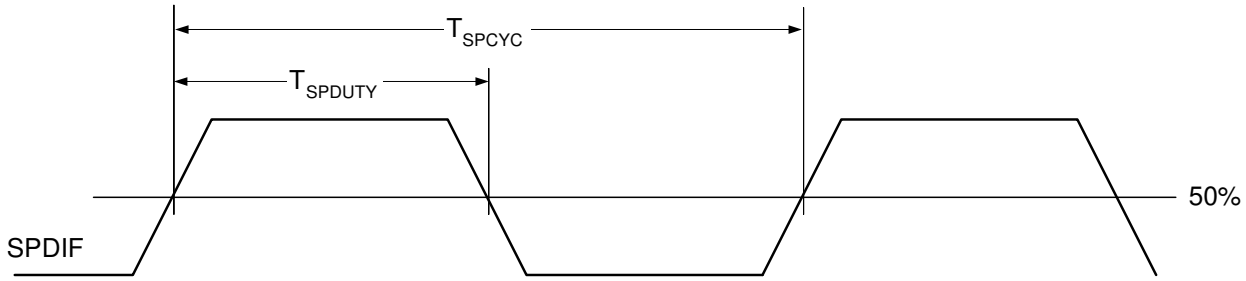


Figure 5.7. S/PDIF Output Timings

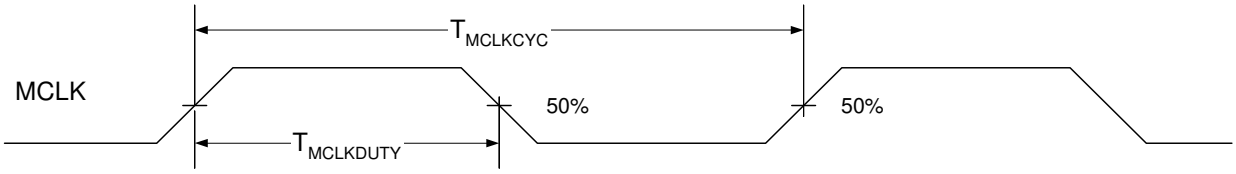


Figure 5.8. MCLK Timings

5.6. Calculating Setup and Hold Times for Video Bus

5.6.1. 24/30/36-Bit Mode

Output data is clocked out on one rising or falling edge of ODCK, and is then captured downstream using the same polarity ODCK edge one clock period later. The setup time of data to ODCK and hold time of ODCK to data are therefore a function of the worst case ODCK to output delay, as shown in Figure 5.9. The active rising ODCK edge is shown with an arrowhead. For OCK_INV = 1, reverse the logic.

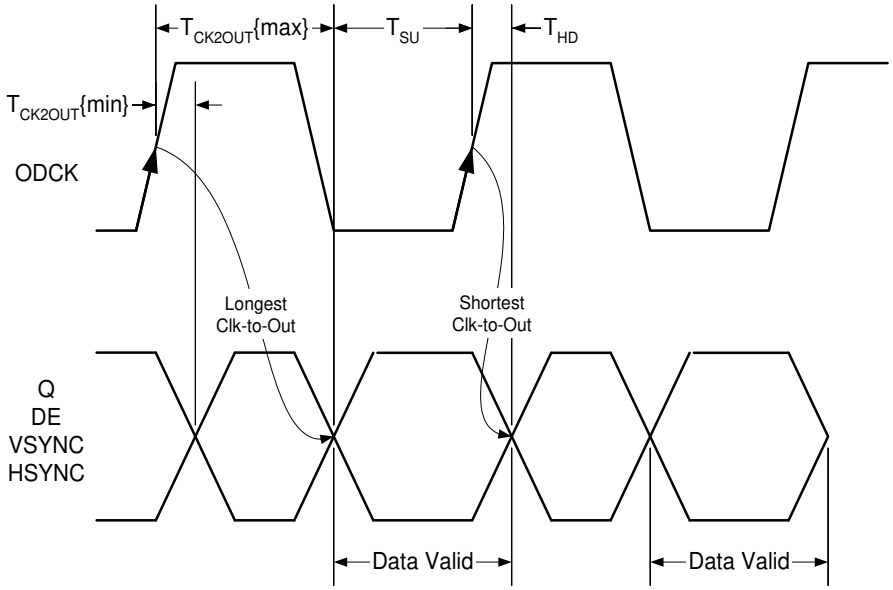


Figure 5.9. 24/30/36-Bit Mode Receiver Output Setup and Hold Times

Table 5.1 shows minimum calculated setup and hold times for commonly used ODCK frequencies. The setup and hold times apply to DE, VSYNC, HSYNC, and Data output pins, with an output load of 10 pF. These are approximations. Hold time is not related to ODCK frequency.

Table 5.1. Calculation of 24/30/36-Bit Output Setup and Hold Times

Mode	Symbol	Parameter	T_{ODCK}		Min
24/30/36-Bit Mode	T_{SU}	Setup Time to ODCK = $T_{ODCK} - T_{CK2OUT}$\{max\}	27 MHz	37.0 ns	34.5 ns
			74.25 MHz	13.5 ns	11.0 ns
	T_{HD}	Hold Time from ODCK = T_{CK2OUT}\{min\}	27 MHz	37.0 ns	0.4 ns

5.6.2. 12/15/18-Bit Dual-Edge Mode

Output data is clocked out on both the rising and falling edges of ODCK, and is then captured downstream using the opposite ODCK edge. This is shown in Figure 5.10. The setup time of data to ODCK is a function of the shortest duty cycle and the longest ODCK to output delay. The hold time does not depend on duty cycle since every edge is used, and is a function only of the shortest ODCK to output delay.

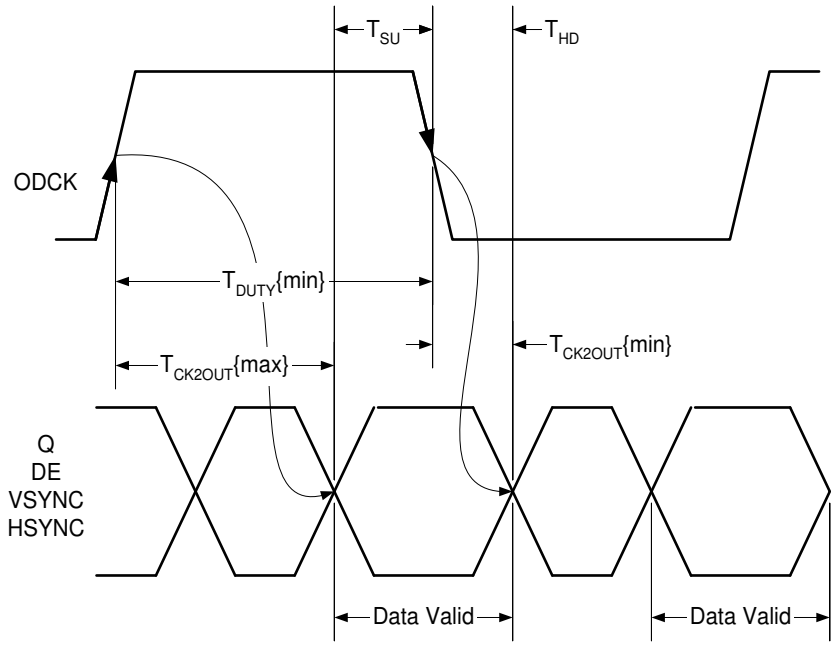


Figure 5.10. 12/15/18-Bit Mode Receiver Output Setup and Hold Times

Table 5.2 shows minimum calculated setup and hold times for commonly used ODCK frequencies, up to the maximum allowed for 12/15/18-bit mode. The setup and hold times apply to DE, VSYNC, HSYNC, and Data output pins, with output load of 10 pF. These are approximations. Hold time is not related to ODCK frequency.

Table 5.2. Calculation of 12/15/18-Bit Output Setup and Hold Times

Mode	Symbol	Parameter	T_{ODCK}		Min
12/15/18-Bit Mode	T_{SU}	Setup Time to ODCK = T_{ODCK} • T_{DUTY}{min} – T_{CK2OUT}{max}	27 MHz	37.0 ns	11 ns
			74.25 MHz	13.5 ns	1.6 ns
	T_{HD}	Hold Time from ODCK = T_{CK2OUT}{min}	27 MHz	37.0 ns	0.4 ns

5.7. Calculating Setup and Hold Times for I²S Audio Bus

Valid serial data is available at Tsck2sd after the falling edge of the first SCK cycle, and then captured downstream using the active rising edge of SCK one clock period later. The setup time of data to SCK (T_{SU}) and hold time of SCK to data (T_{HD}) are therefore a function of the worst case SCK-to-output data delay (Tsck2sd). Figure 5.6 illustrates this timing relationship. The active SCK edge (rising edge) is shown with an arrowhead. For a falling edge sampling clock, the logic is reversed.

Table 5.3 shows the setup and hold time calculation examples for various audio sample frequencies. The formula used in these examples also applies when calculating the setup and hold times for other audio sampling frequencies.

Table 5.3. I²S Setup and Hold Time Calculations

Symbol	Parameter	FWS (kHz)	FSCLK (MHz)	Ttr	Min
T_{SU}	Setup Time, SCK to SD/WS $= T_{TR} - (T_{SCKDUTY\_WORST} + T_{SCK2SD\_MAX})$ $= T_{TR} - (0.6T_{TR} + 5 ns)$ $= 0.4T_{TR} - 5 ns$	32 kHz	2.048	488 ns	190 ns
		44.1 kHz	2.822	354 ns	136 ns
		48 kHz	3.072	326 ns	125 ns
		96 kHz	6.144	163 ns	60 ns
		192 kHz	12.288	81 ns	27 ns
T_{HD}	Hold Time, SCK to SD/WS $= (T_{SCKDUTY\_WORST} - T_{SCK2SD\_MIN})$ $= 0.4T_{TR} - 5 ns$	32 kHz	2.048	488 ns	190 ns
		44.1 kHz	2.822	354 ns	136 ns
		48 kHz	3.072	326 ns	125 ns
		96 kHz	6.144	163 ns	60 ns
		192 kHz	12.288	81 ns	27 ns

Note: The sample calculations shown are based on WS = 64 SCLK rising edges.

6. Pin Diagram and Descriptions

6.1. Pin Diagram

Figure 6.1 shows the pin connections for the SiI9127A/SiI1127A receiver in the 128-pin TQFP package. Individual pin functions are described in the Pin Descriptions section on the next page.

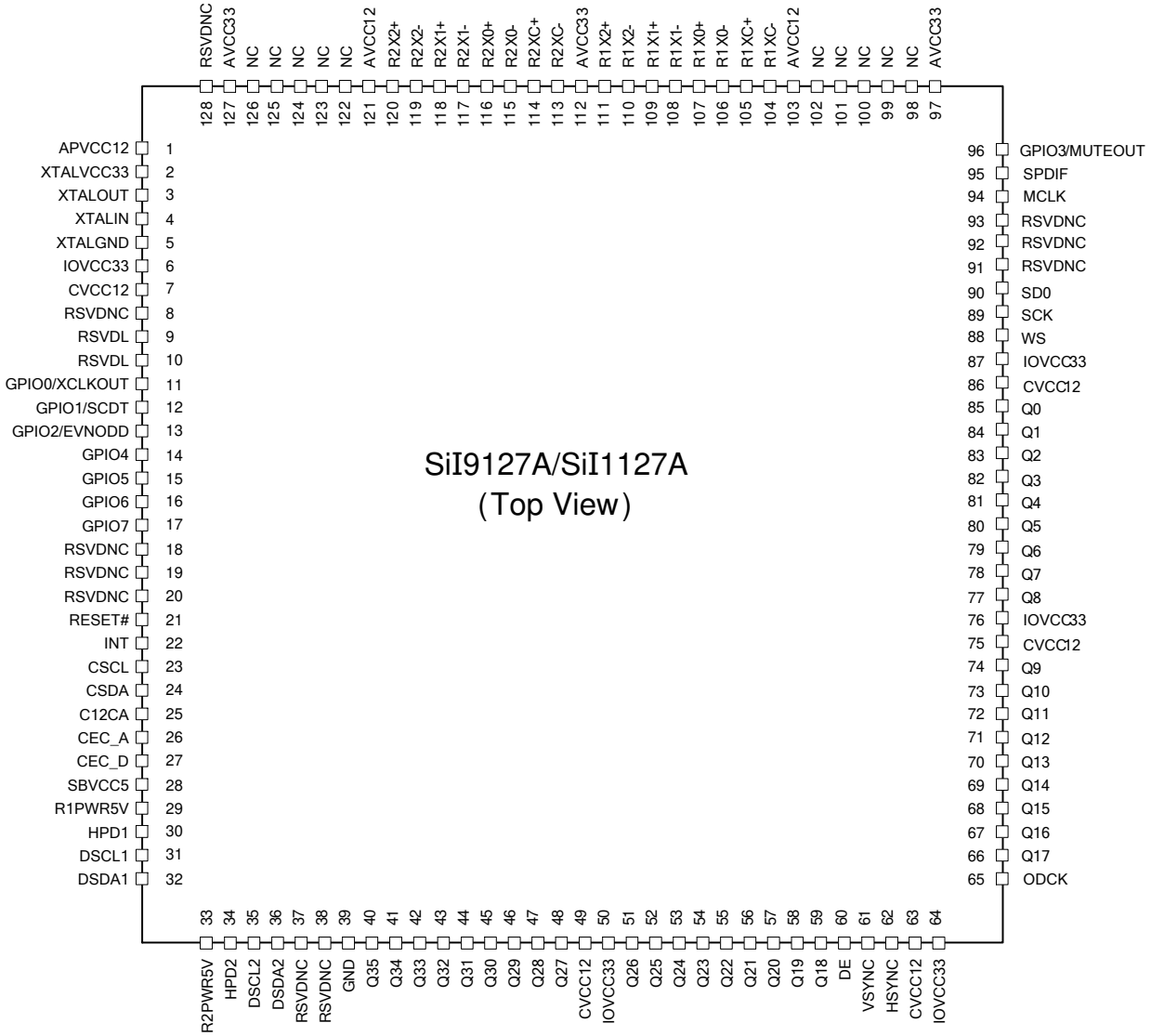


Figure 6.1. Pin Diagram

6.2. Pin Descriptions

6.2.1. Digital Video Output Data Pins

Pin Name	Pin	Type	Dir	Description
Q0	85	LVTTL 2 mA to 14 mA	Output	36-Bit Output Pixel Data Bus. Q[35:0] is highly configurable using the various video configuration registers. It supports a wide array of output formats, including multiple RGB and YCbCr bus formats. Using the appropriate bits in the PD_SYS2 register, the output drivers can be put into a high impedance state.
Q1	84			
Q2	83			
Q3	82			
Q4	81			
Q5	80			
Q6	79			
Q7	78			
Q8	77			
Q9	74			
Q10	73			
Q11	72			
Q12	71			
Q13	70			
Q14	69			
Q15	68			
Q16	67			
Q17	66			
Q18	59			
Q19	58			
Q20	57			
Q21	56			
Q22	55			
Q23	54			
Q24	53			
Q25	52			
Q26	51			
Q27	48			
Q28	47			
Q29	46			
Q30	45			
Q31	44			
Q32	43			
Q33	42			
Q34	41			
Q35	40			

Notes:

1. When transporting video data that uses fewer than 36 bits, the unused bits on the Q[] bus can still carry switching pixel data signals. Unused Q[35:0] bus pins should be unconnected, masked, or ignored by downstream devices. For example, carrying YCbCr 4:2:2 data with 16-bit width (see page 47), the bits Q[0] through Q[7] output switching signals.
2. The output data bus, Q[35:0], can be wire-ORed to another device so one device is always in high impedance state. However, these pins do not have internal pull-up or pull-down resistors, and so cannot pull the bus HIGH or LOW when all connected devices are in the high-impedance state.
3. The drive strength of Q[0:35] can be programmed in 2 mA steps between 2 mA and 14 mA.

6.2.2. Digital Video Output Control Pins

Pin Name	Pin	Type	Dir	Description
DE	60	LVTTL 2 mA to 14 mA	Output	Data Enable.
HSYNC	62	LVTTL 2 mA to 14 mA	Output	Horizontal Sync Output.
VSYNC	61	LVTTL 2 mA to 14 mA	Output	Vertical Sync Output.
GPIO2/ EVNODD	13	LVTTL 8 mA	Input Output	Programmable GPIO2.
GPIO2/ EVNODD			Output	Indicates Even or Odd Field for Interlaced Formats.
ODCK	65	LVTTL 2 mA to 14 mA	Output	Output Data Clock.

Notes:

1. HSYNC and VSYNC outputs carry sync signals for both embedded and separate sync configurations.
2. The drive strength of DE, HSYNC, VSYNC, and ODCK can be programmed in 2 mA steps between 2 mA and 14 mA.

6.2.3. Digital Audio Output Pins

Pin Name	Pin	Type	Dir	Description
XTALIN	4	5 V tolerant LVTTL	Input	Crystal Clock Input. Also allows LVTTL input. Frequency required: 26–28.5 MHz.
XTALOUT	3	LVTTL 4 mA	Output	Crystal Clock Output.
GPIO0/ XCLKOUT	11	LVTTL 4 mA	Input Output	Programmable GPIO0.
GPIO0/ XCLKOUT			Output	Additional Clock Output from crystal oscillator circuit.
MCLK	94	LVTTL 8 mA	Output	Audio Master Clock Output.
SCK	89	LVTTL 4 mA	Output	I^2S Serial Clock Output.
WS	88	LVTTL 4 mA	Output	I^2S Word Select Output.
SD0	90	LVTTL 4 mA	Output	I^2S Serial Data Output.
SPDIF	95	LVTTL 4 mA	Output	S/PDIF Audio Output.
GPIO3/ MUTEOUT	96	LVTTL 4 mA	Input Output	Programmable GPIO3.
GPIO3/ MUTEOUT			Output	Mute Audio Output. Signal to the external downstream audio device, audio DAC, etc. to mute audio output.

Note: The XTALIN pin can either be driven at LVTTL levels by a clock (leaving XTALOUT unconnected), or connected through a crystal to XTALOUT. Refer to the schematic on page 68.

6.2.4. Configuration/Programming Pins

Pin Name	Pin	Type	Dir	Description
INT	22	LVTTL 4 mA	Output	Interrupt Output. Configurable polarity and push-pull output. Multiple sources of interrupt can be enabled through the INT_EN register. See note below.
RESET#	21	Schmitt 5 V tolerant	Input	Reset Pin. Active LOW.
CSCL	23	Schmitt 5 V tolerant	Input	Configuration/Status I²C Clock. Chip configuration/status, CEA-861 support and downstream HDCP registers are accessed via this I²C port. True open drain, so does not pull to GND if power is not applied.
CSDA	24	Schmitt 5 V tolerant 3 mA	Input Output	Configuration/Status I²C Data. Chip configuration/status, CEA-861 support and downstream HDCP registers are accessed via this I²C port. True open drain, so does not pull to GND if power is not applied.
CI2CA	25	LVTTL 5 V tolerant	Input	Local I²C Address Select. LOW = Addresses 0x60/0x68 HIGH = Addresses 0x62/0x6A
GPIO1/SCDT	13	LVTTL 4 mA	Output	Programmable GPIO1.
GPIO1/SCDT				Sync Detection Indicator. Indicates Active Video at HDMI Input Port.
GPIO4	14	LVTTL 4 mA	Input Output	Programmable GPIO4.
GPIO5	15	LVTTL 4 mA	Input Output	Programmable GPIO5.
GPIO6	16	LVTTL 4 mA	Input Output	Programmable GPIO6.
GPIO7	17	LVTTL 4 mA	Input Output	Programmable GPIO7.

Note: The INT pin can be programmed to be either a push-pull LVTTL output or an open-drain output.

6.2.5. HDMI Control Signal Pins

Pin Name	Pin	Type	Dir	Description
DSCL1 DSCL2	31 35	Schmitt Open drain 5 V tolerant	Input	DDC I²C Clock for respective port. HDCP KSV, An and Ri values are exchanged over an I²C port during authentication. True open drain, so does not pull to GND if power is not applied.
DSDA1 DSDA2	32 36	Schmitt Open drain 5 V tolerant 3 mA	Input Output	DDC I²C Data for respective port. HDCP KSV, An and Ri values are exchanged over an I²C port during authentication. True open drain, so does not pull to GND if power is not applied.
HPD1 HPD2	30 34	LVTTL 4 mA	Output	Hot plug output signal to HDMI connector for respective port. Indicates EDID is readable.
R1PWR5V R2PWR5V	29 33	LVTTL 5 V tolerant	Input	5 V power and port detection input for respective port. Used to power internal EDID when device is not powered. These pins require a 10 µF capacitor to ground.
CEC_A	26	CEC compliant 5 V tolerant	Input Output	HDMI compliant CEC I/O used to interface to CEC devices. This pin connects to the CEC signal of all HDMI connectors in the system. This pin has an internal pull-up resistor.
CEC_D	27	Schmitt 5 V tolerant	Input Output	CEC interface to local system. True open-drain. An external pull-up is required. This pin typically connects to the local CPU.

6.2.6. TMDS Differential Signal Pins

Pin Name	Pin	Type	Dir	Description
R1X0+ R1X0− R1X1+ R1X1− R1X2+ R1X2−	107 106 109 108 111 110	TMDS analog	Input	Port 1 TMDS input data pairs.
R1XC+ R1XC−	105 104	TMDS analog	Input	Port 1 TMDS input clock pair.
R2X0+ R2X0− R2X1+ R2X1− R2X2+ R2X2−	116 115 118 117 120 119	TMDS analog	Input	Port 2 TMDS input data pairs.
R2XC+ R2XC−	114 113	TMDS analog	Input	Port 2 TMDS input clock pair.

6.2.7. Power and Ground Pins

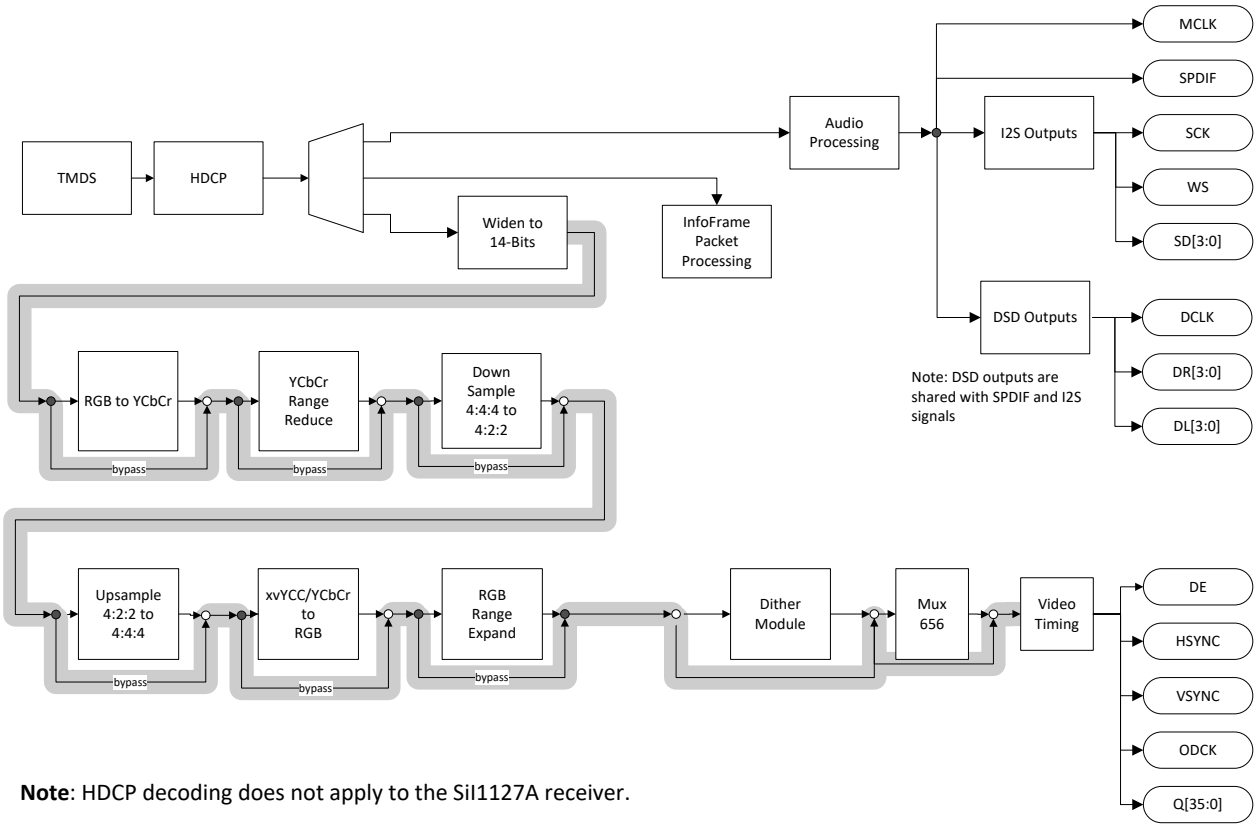
Pin Name	Pin	Type	Description	Supply
CVCC12	7, 49, 63, 75, 86	Power	Digital Logic VCC.	1.2 V
IOVCC33	6, 50, 64, 76, 87	Power	Input/Output Pin VCC.	3.3 V
AVCC33	97, 112, 127	Power	TMDS Analog VCC 3.3 V.	3.3 V
AVCC12	103, 121	Power	TMDS Analog VCC 1.2 V.	1.2 V
APVCC12	1	Power	Audio Clock Regeneration PLL Analog VCC. Must be connected to 1.2 V.	1.2 V
XTALVCC33	2	Power	Audio Clock Regeneration PLL crystal oscillator power. Must be connected to 3.3 V.	3.3 V
XTALGND	5	Ground	Audio Clock Regeneration ground.	Ground
SBVCC5	28	Power	Standby power supply. All other supplies can be off with SBVCC5 on. This pin requires a 10 µF capacitor to ground.	5 V
GND	39, ePad (bottom of package)	Ground	Ground. The ePad ***must*** be soldered to ground.	Ground

6.2.8. Reserved and Not Connected Pins

Pin Name	Pin	Type	Description	Supply
RSVDNC	8, 18–20, 37, 38, 91, 92, 93, 128	Reserved	Reserved, must be left unconnected.	No connection
RSVDL	9, 10	Reserved	Reserved, must be tied to ground.	Ground
NC	98–102, 122–126	Not connected	Must be left unconnected.	No connection

7. Video Path

The SiI9127A/SiI1127A receiver accepts all valid HDMI input formats and can transform that video in a variety of ways to produce the proper video output format. The following pages describe how to control the video path formatting and how to assign output pins for each video output format. The processing blocks in Figure 7.1 correspond to those shown in Figure 7.2 through Figure 7.4.



Note: HDCP decoding does not apply to the SiI1127A receiver.

Figure 7.1. Receiver Video and Audio Data Processing Paths

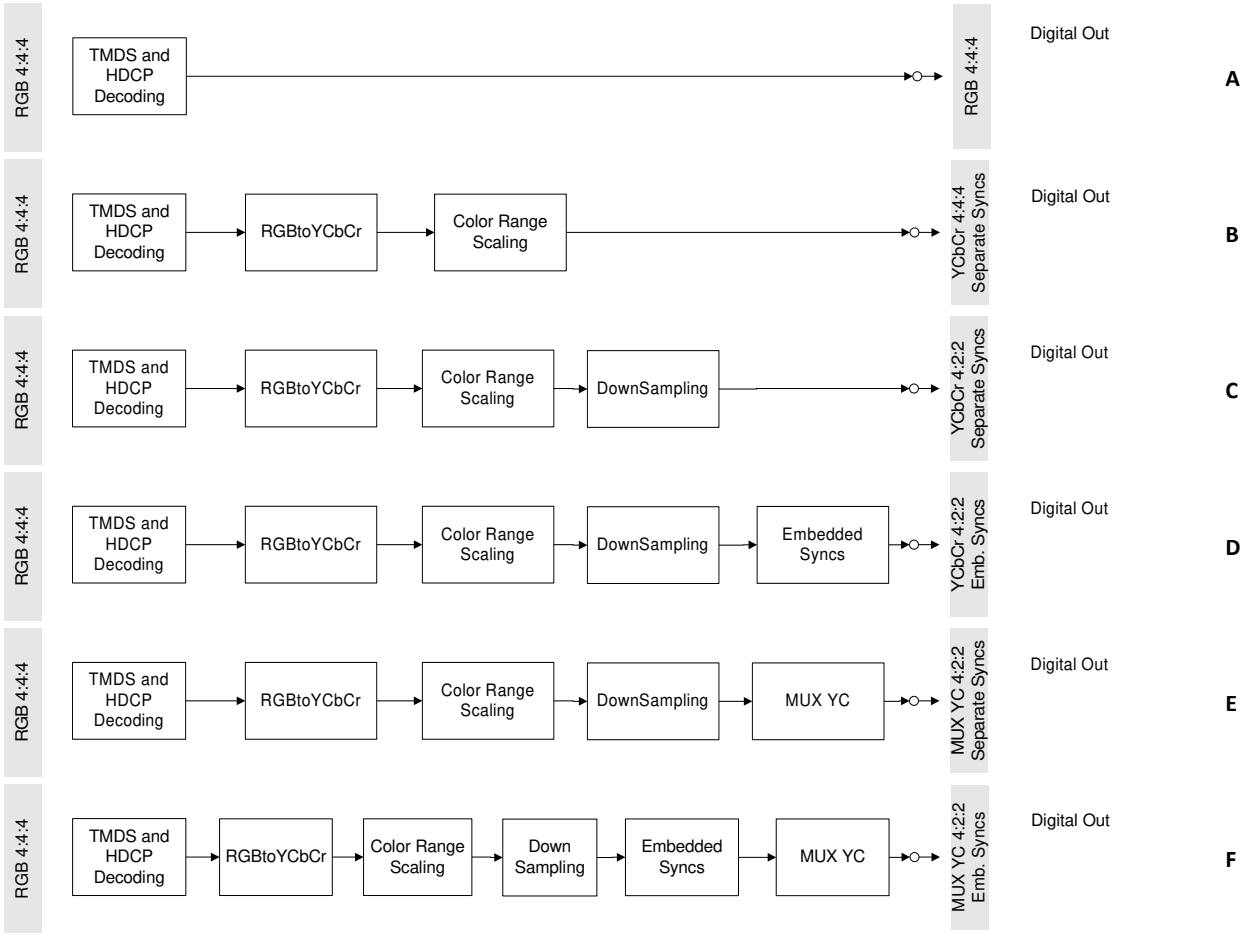
7.1. HDMI Input Modes to SiI9127A/SiI1127A Output Modes

The HDMI link supports transport of video in any of the three modes; RGB 4:4:4, YCbCr/xvYCC 4:4:4, or YCbCr/xvYCC 4:2:2. The flexible video path in the SiI9127A/SiI1127A receiver allows reformatting of video data to a set of output modes. Table 7.1 lists the supported transformations and points to the figure for each. In every case, the HDMI link itself carries separate syncs.

Table 7.1. Translating HDMI Formats to Output Formats

HDMI Input Mode	Digital Output Format					
	RGB 4:4:4 Separate Sync	YCbCr 4:4:4 Separate Sync	YCbCr 4:2:2 Separate Sync	YCbCr 4:2:2 Embedded Sync	YC Mux Separate Sync	YC Mux Embedded Sync
RGB 4:4:4	Figure 7.2A	Figure 7.2B	Figure 7.2C	Figure 7.2D	Figure 7.2E	Figure 7.2F
YCbCr/xvYCC 4:4:4	Figure 7.3A	Figure 7.3B	Figure 7.3C	Figure 7.3D	Figure 7.3E	Figure 7.3F
YCbCr/xvYCC 4:2:2	Figure 7.4A	Figure 7.4B	Figure 7.4C	Figure 7.4D	Figure 7.4E	Figure 7.4F

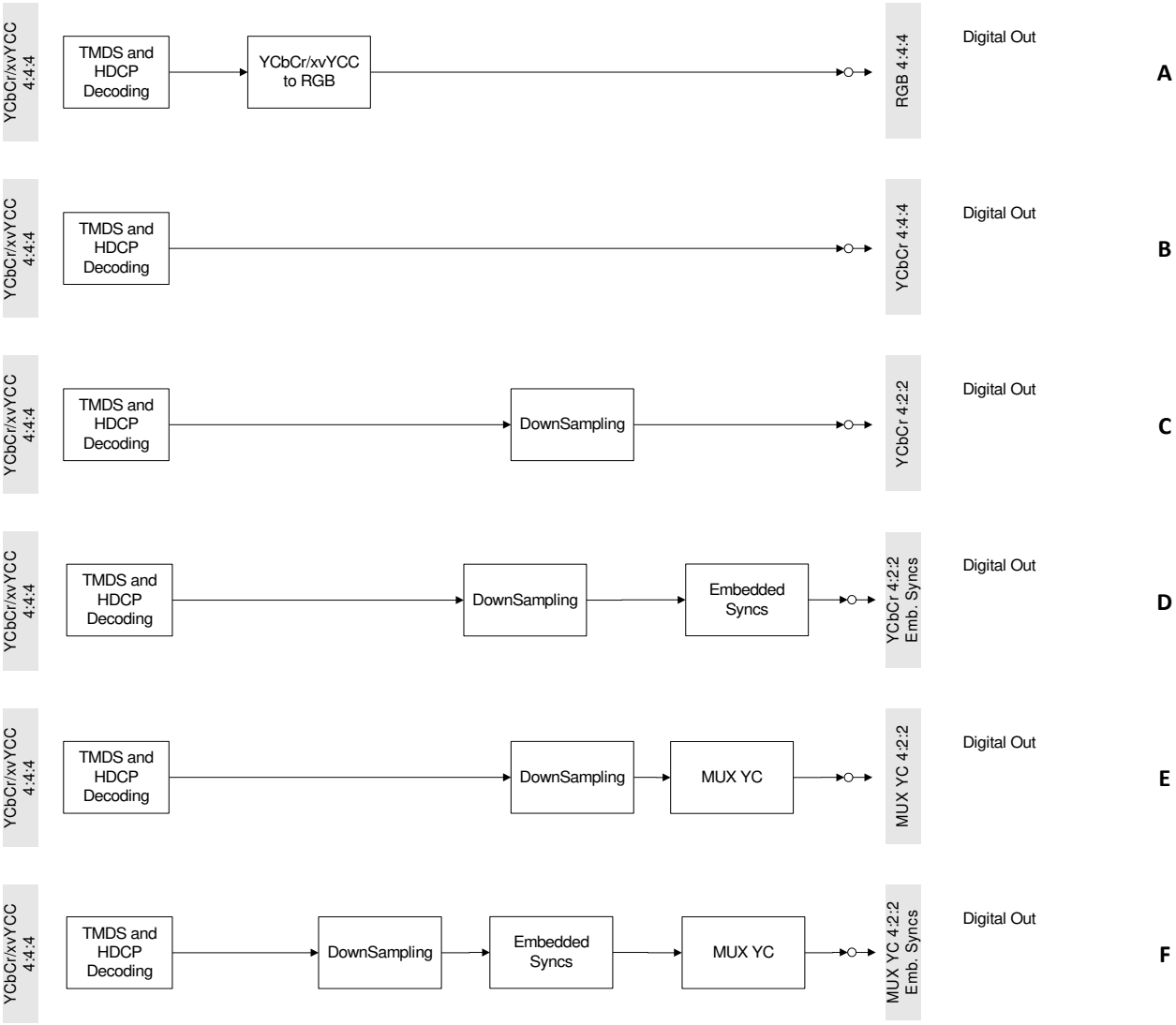
7.1.1. HDMI RGB 4:4:4 Input Processing



Note: HDCP decoding does not apply to the SiI1127A receiver.

Figure 7.2. HDMI RGB 4:4:4 Input to Video Output Transformations

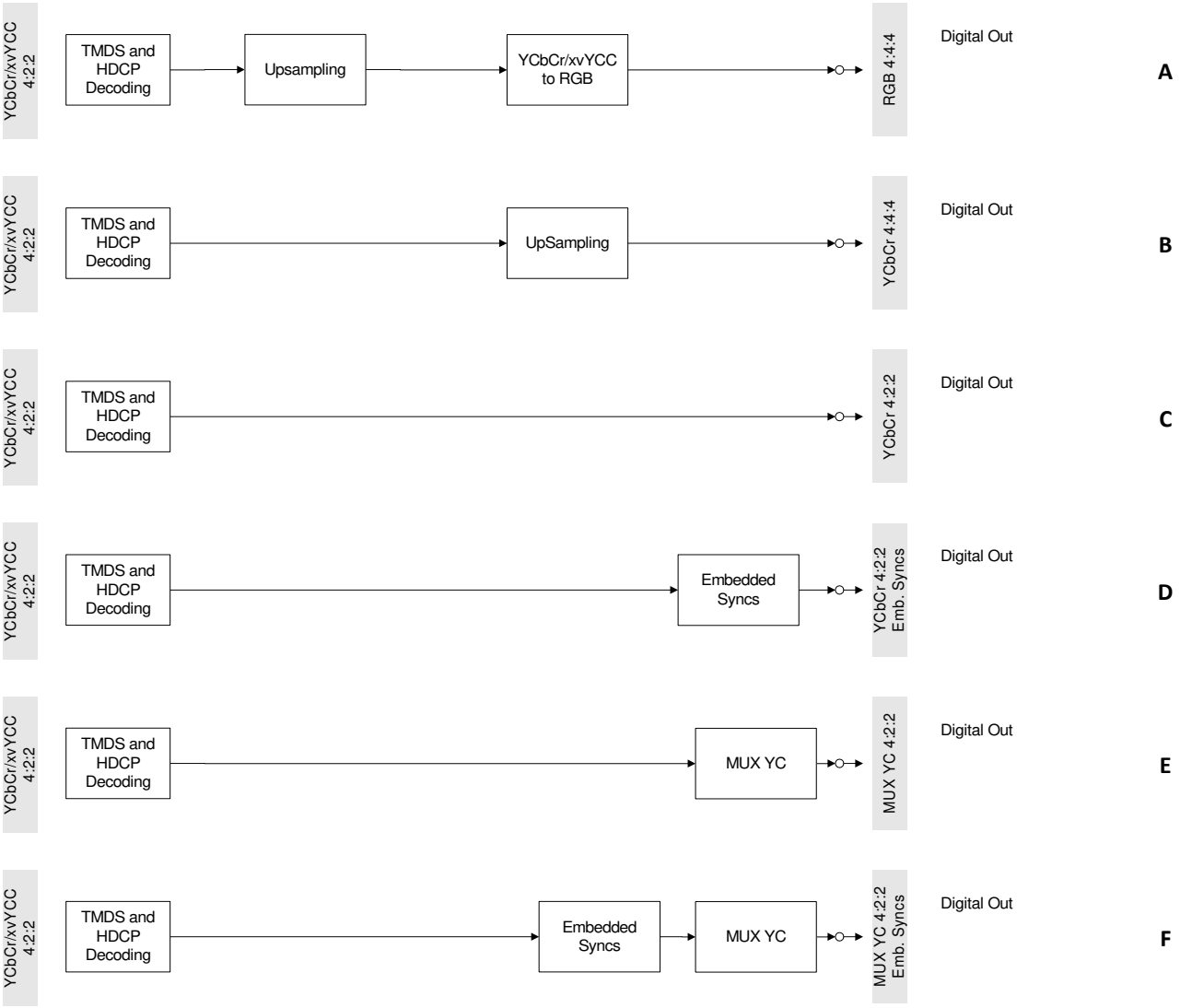
7.1.2. HDMI YCbCr/xvYCC 4:4:4 Input Processing



Note: HDCP decoding does not apply to the SiI1127A receiver.

Figure 7.3. HDMI YCbCr/xvYCC 4:4:4 Input to Video Output Transformations

7.1.3. HDMI YCbCr/xvYCC 4:2:2 Input Processing



Note: HDCP decoding does not apply to the SiI1127A receiver.

Figure 7.4. HDMI YCbCr/xvYCC 4:2:2 Input to Video Output Transformations

7.2. SiI9127A/SiI1127A Output Mode Configuration

The SiI9127A/SiI1127A receiver supports multiple output data mappings. Some have separate control signals while others have embedded control signals. The selection of data mapping mode should be consistent at both the pins and in the corresponding register settings. Refer to the SiI-PR-1033 Programmer Reference for more details.

Table 7.2. Output Video Formats

Output Mode	Data Widths	Pixel Replication	Syncs	Page	Notes
RGB 4:4:4	24, 30, 36	1x	Separate	45	3, 7
YCbCr 4:4:4	24, 30, 36	1x	Separate	45	1, 3, 7
YC 4:2:2 Sep. Syncs	16, 20, 24	1x	Separate	47	2, 3
YC 4:2:2 Sep. Syncs	16, 20, 24	2x	Separate	47	2, 3, 8
YC 4:2:2 Emb. Syncs	16, 20, 24	1x	Embedded	50	2, 5
YC MUX 4:2:2	8, 10, 12	2x	Separate	53	2, 4, 8, 9
YC MUX 4:2:2 Emb. Syncs	8, 10, 12	2x	Embedded	55	2, 5, 6, 8, 9

Notes:

1. YC 4:4:4 data contains one Cr, one Cb and one Y value for every pixel.
2. YC 4:2:2 data contains one Cr and one Cb value for every two pixels; and one Y value for every pixel.
3. These formats can be carried across the HDMI link. Refer to the HDMI Specification, Section 6.2.3. The link clock must be within the specified range of the receiver.
4. In YC MUX mode data is sent to one or two 8/10/12-bit channels.
5. YC MUX with embedded SAV/EAV signal.
6. Syncs are embedded using SAV/EAV codes.
7. A 2x clock can also be sent with 4:4:4 data.
8. When sending a 2x clock the HDMI source must also send AVI InfoFrames with an accurate pixel replication field. Refer to the HDMI Specification, Section 6.4.
9. 2x clocking does not support YC 4:2:2 MUX timings for resolutions greater than 720p or 1080i, because the output clock frequency would exceed the range allowed for the receiver.

The SiI9127A/SiI1127A receiver can output video in various formats on its parallel digital output bus. Some transformation of the data received over HDMI is necessary in some modes. Digital output is used with either 4:4:4 or 4:2:2 data.

The diagrams do not show separation of the audio and InfoFrame packets from the HDMI stream, which occurs immediately after the TMDS and optional HDCP decoding. The HDMI link always carries separate HSYNC and VSYNC and DE. Therefore the SAV/EAV sync encoder must be used whenever the output mode includes embedded sync.

The timing diagrams in Figure 7.5 through Figure 7.9 show only a representation of the DE, HSYNC, and VSYNC timings. These timings are specific to the video resolution, as defined by EIA/CEA-861B and other specs. The number of pixels shown per DE HIGH time is representative, to show the data formatting.

7.2.1. RGB and YCbCr 4:4:4 Formats with Separate Syncs

The pixel clock runs at the pixel rate, and a complete definition of each pixel is output on each clock. Figure 7.5 shows RGB data. The same timing format is used for YCbCr 4:4:4 as listed in Table 7.3.

Figure 7.5 shows timings with OCLKDIV = 0 and OCKINV = 1.

Table 7.3. 4:4:4 Mappings

Pin Name	36-bit		30-bit		24-bit	
	RGB	YCbCr	RGB	YCbCr	RGB	YCbCr
Q0	B0	Cb0	NC	NC	NC	NC
Q1	B1	Cb1	NC	NC	NC	NC
Q2	B2	Cb2	B0	Cb0	NC	NC
Q3	B3	Cb3	B1	Cb1	NC	NC
Q4	B4	Cb4	B2	Cb2	B0	Cb0
Q5	B5	Cb5	B3	Cb3	B1	Cb1
Q6	B6	Cb6	B4	Cb4	B2	Cb2
Q7	B7	Cb7	B5	Cb5	B3	Cb3
Q8	B8	Cb8	B6	Cb6	B4	Cb4
Q9	B9	Cb9	B7	Cb7	B5	Cb5
Q10	B10	Cb10	B8	Cb8	B6	Cb6
Q11	B11	Cb11	B9	Cb9	B7	Cb7
Q12	G0	Y0	NC	NC	NC	NC
Q13	G1	Y1	NC	NC	NC	NC
Q14	G2	Y2	G0	Y0	NC	NC
Q15	G3	Y3	G1	Y1	NC	NC
Q16	G4	Y4	G2	Y2	G0	Y0
Q17	G5	Y5	G3	Y3	G1	Y1
Q18	G6	Y6	G4	Y4	G2	Y2
Q19	G7	Y7	G5	Y5	G3	Y3
Q20	G8	Y8	G6	Y6	G4	Y4
Q21	G9	Y9	G7	Y7	G5	Y5
Q22	G10	Y10	G8	Y8	G6	Y6
Q23	G11	Y11	G9	Y9	G7	Y7
Q24	R0	Cr0	NC	NC	NC	NC
Q25	R1	Cr1	NC	NC	NC	NC
Q26	R2	Cr2	R0	Cr0	NC	NC
Q27	R3	Cr3	R1	Cr1	NC	NC
Q28	R4	Cr4	R2	Cr2	R0	Cr0
Q29	R5	Cr5	R3	Cr3	R1	Cr1
Q30	R6	Cr6	R4	Cr4	R2	Cr2
Q31	R7	Cr7	R5	Cr5	R3	Cr3
Q32	R8	Cr8	R6	Cr6	R4	Cr4
Q33	R9	Cr9	R7	Cr7	R5	Cr5
Q34	R10	Cr10	R8	Cr8	R6	Cr6
Q35	R11	Cr11	R9	Cr9	R7	Cr7
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

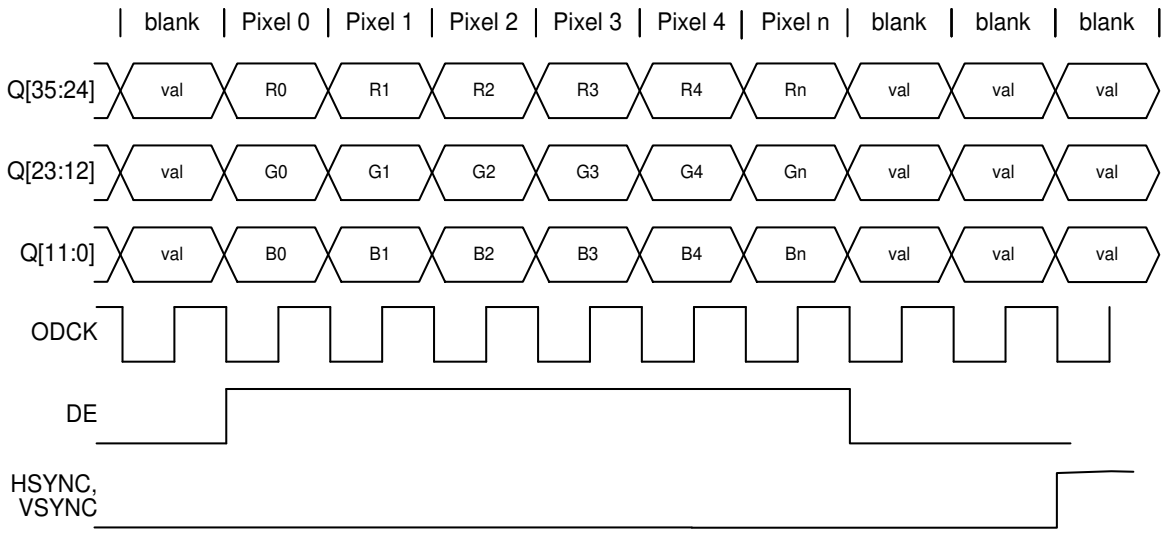


Figure 7.5. 4:4:4 Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9127A/SiI1127A registers, because no pixel data is carried on HDMI during blanking.

7.2.2. YC 4:2:2 Formats with Separate Syncs

The YC 4:2:2 formats output one pixel for every pixel clock period. A luminance (Y) value is sent for every pixel, but the chrominance values Cb and Cr are sent over two pixels. Pixel data can be 24-bit, 20-bit or 16-bit. HSYNC and VSYNC are output separately on their own pins. The DE HIGH time must contain an even number of pixel clocks. Figure 7.6 shows timings with OCLKDIV = 0 and OCKINV = 1.

Table 7.4. YC 4:2:2 Separate Sync Pin Mappings

Pin Name	16-bit YC		20-bit YC		24-bit YC	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	NC	NC
Q5	NC	NC	NC	NC	NC	NC
Q6	NC	NC	NC	NC	NC	NC
Q7	NC	NC	NC	NC	NC	NC
Q8	NC	NC	NC	NC	NC	NC
Q9	NC	NC	NC	NC	NC	NC
Q10	NC	NC	NC	NC	NC	NC
Q11	NC	NC	NC	NC	NC	NC
Q12	NC	NC	NC	NC	Y0	Y0
Q13	NC	NC	NC	NC	Y1	Y1
Q14	NC	NC	Y0	Y0	Y2	Y2
Q15	NC	NC	Y1	Y1	Y3	Y3
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q19	Y3	Y3	Y5	Y5	Y7	Y7
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q21	Y5	Y5	Y7	Y7	Y9	Y9
Q22	Y6	Y6	Y8	Y8	Y10	Y10
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q24	NC	NC	NC	NC	Cb0	Cr0
Q25	NC	NC	NC	NC	Cb1	Cr1
Q26	NC	NC	Cb0	Cr0	Cb2	Cr2
Q27	NC	NC	Cb1	Cr1	Cb3	Cr3
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

Table 7.5. YC 4:2:2 (Pass Through Only) Separate Sync Pin Mapping

Pin Name	16-bit YC		20-bit YC		24-bit YC	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	Y0	Y0
Q5	NC	NC	NC	NC	Y1	Y1
Q6	NC	NC	Y0	Y0	Y2	Y2
Q7	NC	NC	Y1	Y1	Y3	Y3
Q8	NC	NC	NC	NC	Cb0	Cr0
Q9	NC	NC	NC	NC	Cb1	Cr1
Q10	NC	NC	Cb0	Cr0	Cb2	Cr2
Q11	NC	NC	Cb1	Cr1	Cb3	Cr3
Q12	NC	NC	NC	NC	NC	NC
Q13	NC	NC	NC	NC	NC	NC
Q14	NC	NC	NC	NC	NC	NC
Q15	NC	NC	NC	NC	NC	NC
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q19	Y3	Y3	Y5	Y5	Y7	Y7
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q21	Y5	Y5	Y7	Y7	Y9	Y9
Q22	Y6	Y6	Y8	Y8	Y10	Y10
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q24	NC	NC	NC	NC	NC	NC
Q25	NC	NC	NC	NC	NC	NC
Q26	NC	NC	NC	NC	NC	NC
Q27	NC	NC	NC	NC	NC	NC
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

Note: This pin mapping is only valid when the input video format is YC 4:2:2 and the output video format is YC 4:2:2 also. No video processing blocks should be enabled when this pin mapping is used.

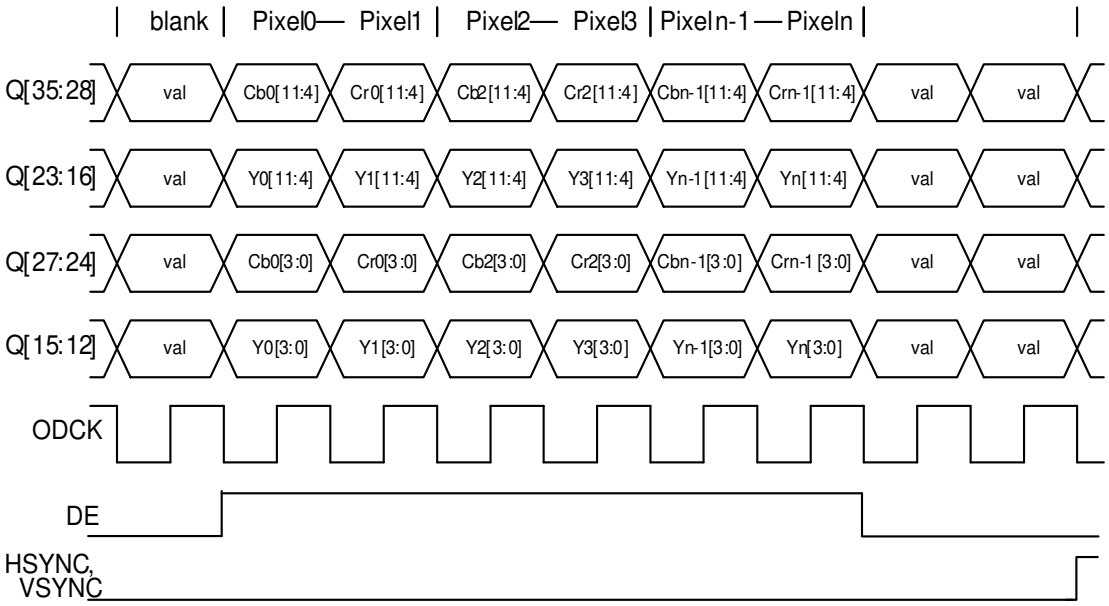


Figure 7.6. YC Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9127A/SiI1127A receiver registers, because no pixel data is carried on HDMI during blanking.

7.2.3. YC 4:2:2 Formats with Embedded Syncs

The YC 4:2:2 embedded sync format is identical to the previous format (YC 4:2:2), except that the syncs are embedded and not separate. Pixel data can be 24-bit, 20-bit or 16-bit. DE is always output. Figure 7.7 shows the Start of Active Video (SAV) preamble, the End of Active Video (EAV) suffix, and shows timings with OCLKDIV = 0 and OCKINV = 1.

Table 7.6. YC 4:2:2 Embedded Sync Pin Mappings

Pin Name	16-bit YC		20-bit YC		24-bit YC	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	NC	NC
Q5	NC	NC	NC	NC	NC	NC
Q6	NC	NC	NC	NC	NC	NC
Q7	NC	NC	NC	NC	NC	NC
Q8	NC	NC	NC	NC	NC	NC
Q9	NC	NC	NC	NC	NC	NC
Q10	NC	NC	NC	NC	NC	NC
Q11	NC	NC	NC	NC	NC	NC
Q12	NC	NC	NC	NC	Y0	Y0
Q13	NC	NC	NC	NC	Y1	Y1
Q14	NC	NC	Y0	Y0	Y2	Y2
Q15	NC	NC	Y1	Y1	Y3	Y3
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q19	Y3	Y3	Y5	Y5	Y7	Y7
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q21	Y5	Y5	Y7	Y7	Y9	Y9
Q22	Y6	Y6	Y8	Y8	Y10	Y10
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q24	NC	NC	NC	NC	Cb0	Cr0
Q25	NC	NC	NC	NC	Cb1	Cr1
Q26	NC	NC	Cb0	Cr0	Cb2	Cr2
Q27	NC	NC	Cb1	Cr1	Cb3	Cr3
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
VSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
DE	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded

Table 7.7. YC 4:2:2 (Pass Through Only) Embedded Sync Pin Mapping

Pin Name	16-bit YC		20-bit YC		24-bit YC	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	Y0	Y0
Q5	NC	NC	NC	NC	Y1	Y1
Q6	NC	NC	Y0	Y0	Y2	Y2
Q7	NC	NC	Y1	Y1	Y3	Y3
Q8	NC	NC	NC	NC	Cb0	Cr0
Q9	NC	NC	NC	NC	Cb1	Cr1
Q10	NC	NC	Cb0	Cr0	Cb2	Cr2
Q11	NC	NC	Cb1	Cr1	Cb3	Cr3
Q12	NC	NC	NC	NC	NC	NC
Q13	NC	NC	NC	NC	NC	NC
Q14	NC	NC	NC	NC	NC	NC
Q15	NC	NC	NC	NC	NC	NC
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q19	Y3	Y3	Y5	Y5	Y7	Y7
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q21	Y5	Y5	Y7	Y7	Y9	Y9
Q22	Y6	Y6	Y8	Y8	Y10	Y10
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q24	NC	NC	NC	NC	NC	NC
Q25	NC	NC	NC	NC	NC	NC
Q26	NC	NC	NC	NC	NC	NC
Q27	NC	NC	NC	NC	NC	NC
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
VSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
DE	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded

Note: This pin mapping is only valid when the input video format is YC 4:2:2 and the output video format is YC 4:2:2 also. No video processing blocks should be enabled when this pin mapping is used.

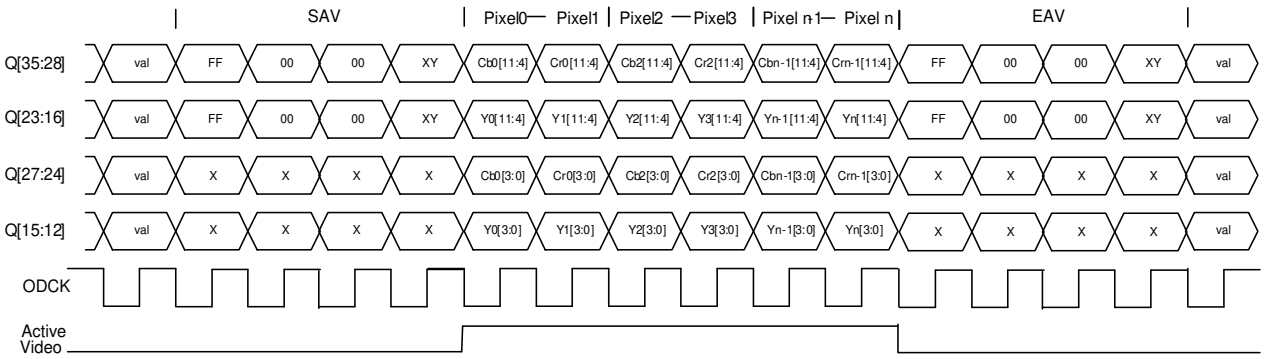


Figure 7.7. YC 4:2:2 Embedded Sync Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9127A/SiI1127A registers, because no pixel data is carried on HDMI during blanking. SAV/EAV codes appear as an 8-bit field on both Q[35:28] (per SMPTE) and Q[23:16].

7.2.4. YC Mux (4:2:2) Formats with Separate Syncs

The video data is multiplexed onto fewer pins than the mapping in Table 7.8, but complete luminance (Y) and chrominance (Cb and Cr) data is still provided for each pixel because the output pixel clock runs at twice the pixel rate. Figure 7.8 on the next page shows the 24-bit mode. The 16-bit and 20-bit mappings use fewer output pins for the pixel data. The separate syncs. Figure 7.8 shows timings with OCLKDIV = 0 and OCKINV = 1.

Table 7.8. YC Mux 4:2:2 Mappings

Pin Name	8-bit YCbCr	10-bit YCbCr	12-bit YCbCr
Q0	NC	NC	NC
Q1	NC	NC	NC
Q2	NC	NC	NC
Q3	NC	NC	NC
Q4	NC	NC	NC
Q5	NC	NC	NC
Q6	NC	NC	NC
Q7	NC	NC	NC
Q8	NC	NC	NC
Q9	NC	NC	NC
Q10	NC	NC	NC
Q11	NC	NC	NC
Q12	NC	NC	D0
Q13	NC	NC	D1
Q14	NC	D0	D2
Q15	NC	D1	D3
Q16	D0	D2	D4
Q17	D1	D3	D5
Q18	D2	D4	D6
Q19	D3	D5	D7
Q20	D4	D6	D8
Q21	D5	D7	D9
Q22	D6	D8	D10
Q23	D7	D9	D11
Q24	NC	NC	NC
Q25	NC	NC	NC
Q26	NC	NC	NC
Q27	NC	NC	NC
Q28	NC	NC	NC
Q29	NC	NC	NC
Q30	NC	NC	NC
Q31	NC	NC	NC
Q32	NC	NC	NC
Q33	NC	NC	NC
Q34	NC	NC	NC
Q35	NC	NC	NC
HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE

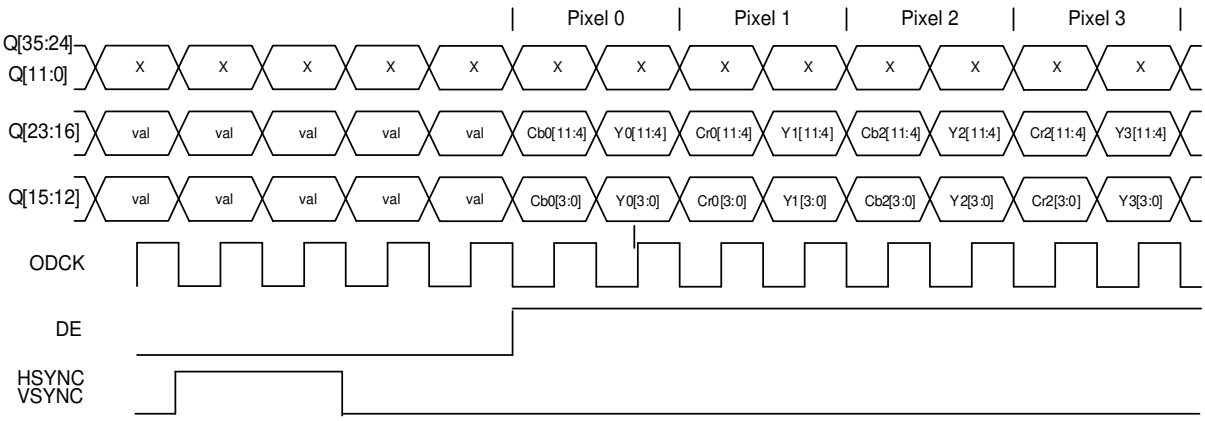


Figure 7.8. YC Mux 4:2:2 Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9127A/SiI1127A registers, because no pixel data is carried on HDMI during blanking.

7.2.5. YC Mux 4:2:2 Formats with Embedded Syncs

This mode is similar to that on page 53, but with embedded syncs. It is similar to YC 4:2:2 with embedded syncs, but also multiplexes the luminance (Y) and chrominance (Cb and Cr) onto the same pins on alternating pixel clock cycles. Normally this mode is used only for 480i, 480p, 576i and 576p modes. Output clock rate is half the pixel clock rate on the link. SAV code is shown before rise of DE. EAV follows the falling edge of DE. See the ITU-R BT.656 Specification for more information. 480p 54 MHz output can be achieved if the input differential clock is 54 MHz. Figure 7.9 on the next page shows OCLKDIV = 0 and OCKINV = 1.

Table 7.9. YC Mux 4:2:2 Embedded Sync Pin Mapping

Pin Name	8-bit YCbCr	10-bit YCbCr	12-bit YCbCr
Q0	NC	NC	NC
Q1	NC	NC	NC
Q2	NC	NC	NC
Q3	NC	NC	NC
Q4	NC	NC	NC
Q5	NC	NC	NC
Q6	NC	NC	NC
Q7	NC	NC	NC
Q8	NC	NC	NC
Q9	NC	NC	NC
Q10	NC	NC	NC
Q11	NC	NC	NC
Q12	NC	NC	D0
Q13	NC	NC	D1
Q14	NC	D0	D2
Q15	NC	D1	D3
Q16	D0	D2	D4
Q17	D1	D3	D5
Q18	D2	D4	D6
Q19	D3	D5	D7
Q20	D4	D6	D8
Q21	D5	D7	D9
Q22	D6	D8	D10
Q23	D7	D9	D11
Q24	NC	NC	NC
Q25	NC	NC	NC
Q26	NC	NC	NC
Q27	NC	NC	NC
Q28	NC	NC	NC
Q29	NC	NC	NC
Q30	NC	NC	NC
Q31	NC	NC	NC
Q32	NC	NC	NC
Q33	NC	NC	NC
Q34	NC	NC	NC
Q35	NC	NC	NC
HSYNC	Embedded	Embedded	Embedded
VSYNC	Embedded	Embedded	Embedded
DE	Embedded	Embedded	Embedded

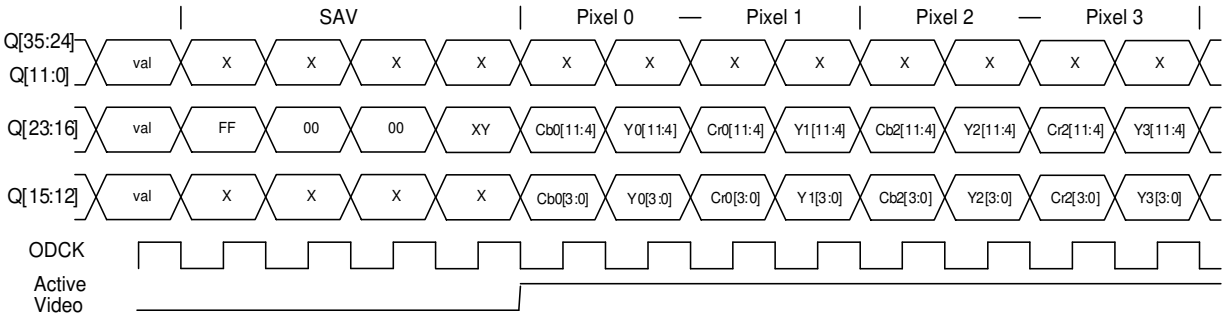


Figure 7.9. YC Mux 4:2:2 Embedded Sync Encoding Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9127A/SiI1127A registers, because no pixel data is carried on HDMI during blanking. Refer to the SiI-PR-1033 Programmer Reference for details. *The Programmer's Reference requires an NDA with Lattice Semiconductor.*

7.2.6. 12/15/18-Bit RGB and YCbCr 4:4:4 Formats with Separate Syncs

The An output clock runs at the pixel rate, and a complete definition of each pixel is output on each clock. One clock edge drives out half the pixel data on 12/15/18 pins. The opposite clock edge drives out the remaining half of the pixel data on the same 12/15/18 pins. Figure 7.10 shows RGB data. The same timing format is used for YCbCr 4:4:4 as listed in the columns of Table 7.10. Control signals (DE, HSYNC, and VSYNC) change state with respect to the first edge of ODCK.

Table 7.10. 12/15/18-Bit Output 4:4:4 Mappings

Pin Name	24-bit				30-bit				36-bit			
	RGB		YCbCr		RGB		YCbCr		RGB		YCbCr	
	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge
Q0	NC	NC	NC	NC	NC	NC	NC	NC	B0	G6	Cb0	Y6
Q1	NC	NC	NC	NC	NC	NC	NC	NC	B1	G7	Cb1	Y7
Q2	NC	NC	NC	NC	NC	NC	NC	NC	B2	G8	Cb2	Y8
Q3	NC	NC	NC	NC	B0	G5	Cb0	Y5	B3	G9	Cb3	Y9
Q4	NC	NC	NC	NC	B1	G6	Cb1	Y6	B4	G10	Cb4	Y10
Q5	NC	NC	NC	NC	B2	G7	Cb2	Y7	B5	G11	Cb5	Y11
Q6	B0	G4	Cb0	Y4	B3	G8	Cb3	Y8	B6	R0	Cb6	Cr0
Q7	B1	G5	Cb1	Y5	B4	G9	Cb4	Y9	B7	R1	Cb7	Cr1
Q8	B2	G6	Cb2	Y6	B5	R0	Cb5	Cr0	B8	R2	Cb8	Cr2
Q9	B3	G7	Cb3	Y7	B6	R1	Cb6	Cr1	B9	R3	Cb9	Cr3
Q10	B4	R0	Cb4	Cr0	B7	R2	Cb7	Cr2	B10	R4	Cb10	Cr4
Q11	B5	R1	Cb5	Cr1	B8	R3	Cb8	Cr3	B11	R5	Cb11	Cr5
Q12	B6	R2	Cb6	Cr2	B9	R4	Cb9	Cr4	G0	R6	Y0	Cr6
Q13	B7	R3	Cb7	Cr3	G0	R5	Y0	Cr5	G1	R7	Y1	Cr7
Q14	G0	R4	Y0	Cr4	G1	R6	Y1	Cr6	G2	R8	Y2	Cr8
Q15	G1	R5	Y1	Cr5	G2	R7	Y2	Cr7	G3	R9	Y3	Cr9
Q16	G2	R6	Y2	Cr6	G3	R8	Y3	Cr8	G4	R10	Y4	Cr10
Q17	G3	R7	Y3	Cr7	G4	R9	Y4	Cr9	G5	R11	Y5	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE

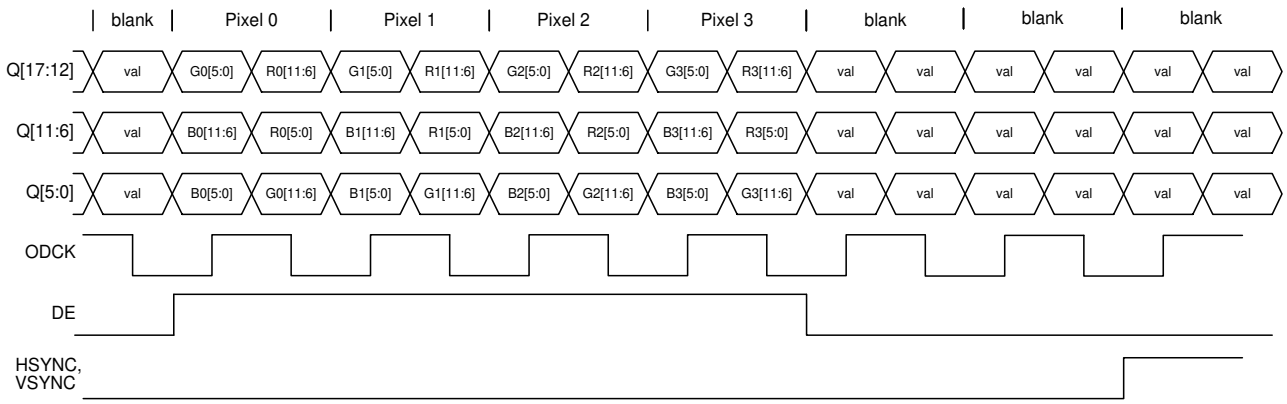


Figure 7.10. 18-Bit Output 4:4:4 Timing Diagram

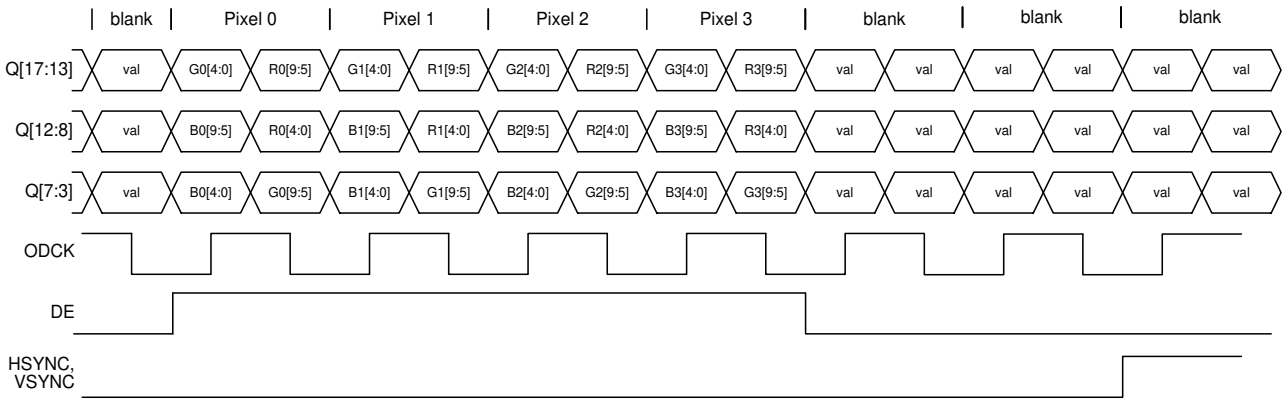


Figure 7.11. 15-Bit Output 4:4:4 Timing Diagram

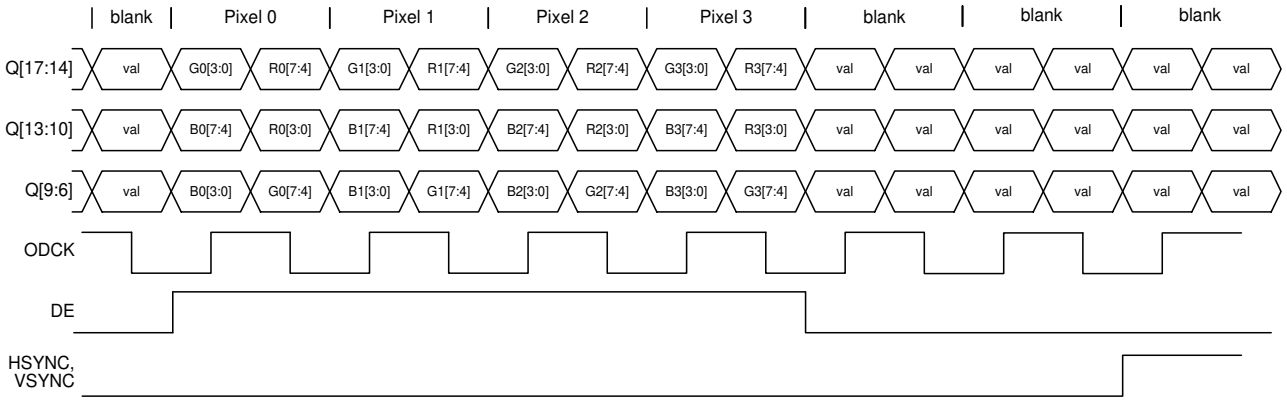


Figure 7.12. 12-Bit Output 4:4:4 Timing Diagram

8. I²C Interfaces

8.1. HDCP E-DDC / I²C Interface

For the SiI9127A device, the HDCP protocol requires values to be exchanged between the video transmitter and the video receiver. These values are exchanged over the DDC channel of the DVI interface. The E-DDC channel follows the I²C serial protocol. The SiI9127A/SiI1127A device is the video receiver in a system design using the SiI9127A/SiI1127A receiver and it has a connection to the E-DDC bus with a slave address of 0x74. The I²C read operation is shown in Figure 8.1, and the write operation is shown in Figure 8.2.

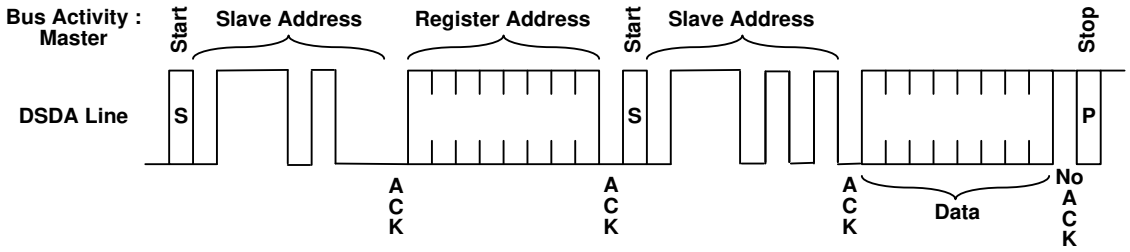


Figure 8.1. I²C Byte Read

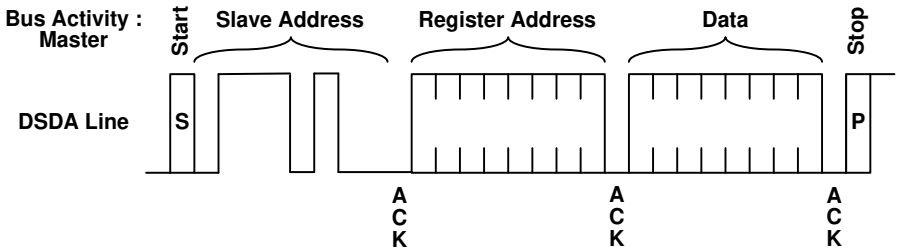


Figure 8.2. I²C Byte Write

Multiple bytes can be transferred in each transaction, regardless of whether they are reads or writes. The operations are similar to those in Figure 8.1 and Figure 8.2 except that there is more than one data phase. An ACK follows each byte except the last byte in a read operation. Byte addresses increment, with the least significant byte transferred first, and the most significant byte last. See the I²C specification for more information.

There is also a Short Read format, designed to improve the efficiency of Ri register reads, which must be done every two seconds while encryption is enabled. This transaction is shown in Figure 8.3. With this format, there is only the slave address phase, and no register address phase, because the register address is reset to 0x08 (Ri) after a hardware or software reset, and after the STOP condition on any preceding I²C transaction.

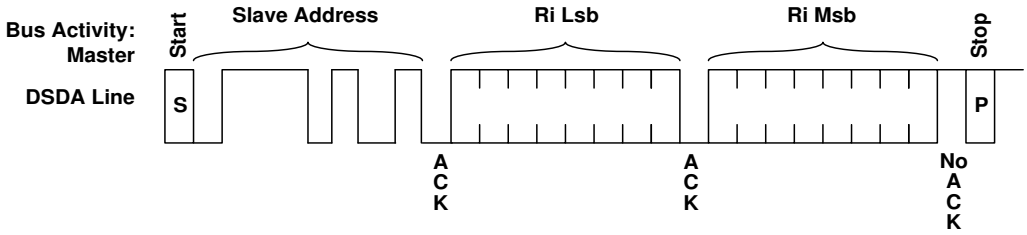


Figure 8.3. Short Read Sequence

8.2. Local I²C Interface

The SiI9127A/SiI1127A receiver has a second I²C port accessible only to the controller in the display device. It is separate from the E-DDC bus. The receiver is a slave device that responds to the six binary I²C device addresses of seven bits each. This I²C interface only supports the read operation shown in Figure 8.1, and the write operation shown in Figure 8.2. It does not support the short read operation shown in Figure 8.3. The I²C data pin for the local I²C bus is CSDA, instead of the DSDA pin shown in these figures.

The local I²C interface on the receiver (pins CSCL and CSDA) is a slave interface that can run up to 400 kHz. This bus is used to configure and control the SiI9127A/SiI1127A device by reading or writing to necessary registers.

The local I²C interface consists of 5 separate I²C slave addresses. Therefore, it appears as 5 separate devices on the I²C local bus. The first two of these addresses, used for HDMI Control and general low level register control, are fixed and can only be set to one of two values by using the CI2CA pin. Table 8.1 shows the address selected for each state of the CI2CA pin at reset. The other 3 addresses, used for CEC, EDID and xvYCC, have an I²C register-programmable address mapped into the HDMI Control register space, so the default value can be changed if there is a bus conflict with another device.

Table 8.1. Control of the Default I²C Addresses with the CI2CA Pin

Register Group	CI2CA = LOW	CI2CA = HIGH
HDMI Control and low level registers (fixed)	0x60 & 0x68	0x62 & 0x6A

The HDMI Control and low level registers are fixed after a reset based on CI2CA pin and cannot be changed. The I²C slave address for the xvYCC registers, EDID Control registers, and the CEC Control registers each have a register associated with them that allows the address to be changed. Refer to the SiI-PR-1033 Programmer Reference for more information.

8.3. Video Requirement for I²C Access

The SiI9127A/SiI1127A receiver does not require an active video clock to access its registers from either the E-DDC port or the local I²C port. Read-Write registers can be written and then read back. Read-only registers that provide values for an active video or audio stream return indeterminate values if there is no video clock and no active syncs.

Use the SCDT and CKDT register bits to determine when active video is being received by the chip.

8.4. I²C Registers

The register values that are exchanged over the HDMI DDC I²C serial interface with the receiver for HDCP are described in the HDCP Specification in Section 2.6 – HDCP Port. Refer to the SiI-PR-1033 Programmer Reference for details on these and all other SiI9127A/SiI1127A registers.

9. Design Recommendations

The following information is provided as recommendations that are based on the experience of Lattice Semiconductor engineers and customers. If you choose to deviate from these recommendations for a particular application, Lattice Semiconductor strongly suggests that you contact one of its technical representatives for an evaluation of the change.

9.1. Power Control

The low-power standby state feature of the SiI9127A/SiI1127A receiver provides a design option of leaving the chip always powered, as opposed to powering it on and off. Leaving the chip powered and using the PD# register bit to put it in a lower power state can result in faster system response time, depending on the system Vcc supply ramp-up delay.

9.2. Power-on Sequencing

Due to timing considerations with the power-on reset circuits within the chip, Lattice Semiconductor recommends that 5 V power is available to the device before the 3.3 V and 1.2 V VCC supplies are enabled. If the 3.3 V and 1.2 V supplies reach their operating levels before the 5 V power supply to the power island, the chip may not reset properly.

9.2.1. Power Pin Current Demands

The limits shown in Table 9.1 indicate the current demanded by each group of power pins on the device. These limits were characterized at maximum VCC, 0 °C ambient temperature and for fast-fast silicon. Actual application current demands can be lower than these figures and vary with video resolution and audio clock frequency.

Table 9.1. Maximum Power Domain Currents versus Video Mode

Mode	ODCK (MHz)	3.3 V Power Domain Currents (mA)		
		IOVCC33	AVCC33	XTALVCC33
480p	27.0	39	62	2
1080i	74.25	104	62	2
1080p	148.5	217	62	2
1080p@12-bit[1]	225	302	62	2

Mode	ODCK (MHz)	1.2 V Power Domain Currents (mA)		
		AVCC12	CVCC12	APVCC12
480p	27.0	79	40	3
1080i	74.25	86	88	3
1080p	148.5	118	158	3
1080p@12-bit[1]	225	95	191	3

Notes:

1. Measured with 12 bits/pixel video data.
2. Measured with 192 kHz, 8-channel audio, except for 480p mode which used 48 kHz, 8-channel audio.
3. Measured with RGB input, vertical black-white/1-pixel stripe (Moire2) pattern, converting to YCbCr output (digital for IOVCC33).
4. Only one core can be selected at a time. The TMDSxSEL register bit turns off the unselected core, except for the termination to AVCC33.

AVCC33 current includes 40 mA for the unselected TMDS core. Only 5 mA of this current is dissipated as power in the receiver; the remainder is dissipated in the HDMI transmitter. The AVCC33 current on the unselected core can be reduced to 5 mA by asserting the corresponding PD_TERMx# register bit.

9.3. HDMI Receiver DDC Bus Protection

The VESA DDC Specification (see Standards Groups on page 74) defines the DDC I^2C interconnect bus to be a 5 V signaling path. The I^2C pins on the SiI9127A/SiI1127A chip are 5 V tolerant and are true open-drain I/O. The pull-up resistors on the DDC bus should be pulled up using the 5 V supply from the HDMI connector. See Figure 9.9 on page 70.

9.4. Decoupling Capacitors

Designers should include decoupling and bypass capacitors at each power pin in the layout. These are shown schematically in Figure 9.4 on page 65. Place these components as close as possible to the SiI9127A/SiI1127A pins and avoid routing through vias. Figure 9.1 shows various types of power pins on the receiver.

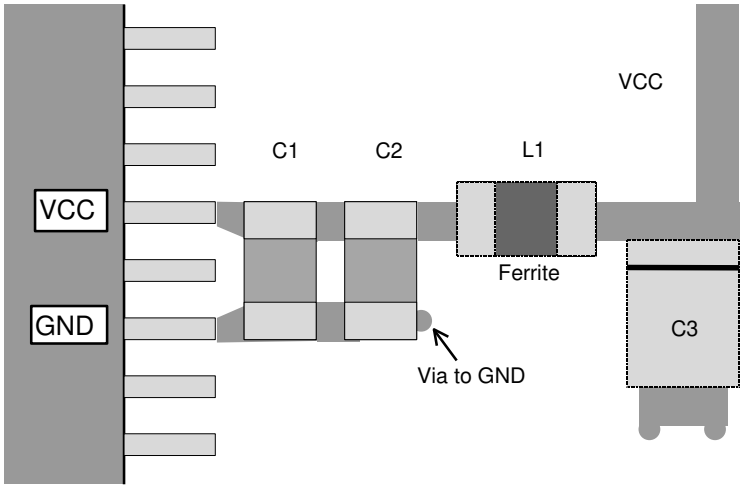


Figure 9.1. Decoupling and Bypass Capacitor Placement

9.5. ESD Protection

The SiI9127A/SiI1127A chip is designed to withstand an electrostatic discharge up to 2 kV. In applications where higher protection levels are required, ESD limiting components can be placed on the differential lines coming into the chip. These components typically have a capacitive effect, reducing the signal quality at higher clock frequencies on the link. Use of the lowest capacitance devices is suggested; the capacitance value should not exceed 5 pF in any case.

Series resistors can be included on the TMDS lines (see Figure 9.9 on page 70) to counteract the impedance effects of ESD protection diodes. The diodes typically lower the impedance because of their capacitance. The resistors raise the impedance to stay within the HDMI Specification, centered on a 100 Ω differential.

9.6. HDMI Receiver Layout

The SiI9127A/SiI1127A chip should be placed as close as possible to the input connectors that carry the TMDS signals. For a system using industry-standard HDMI connectors (see Standards Groups on page 74), the differential lines should be routed as directly as possible from the connector to the receiver. Lattice Semiconductor receivers are tolerant of skews between differential pairs, so spiral skew compensation for path length differences is not required. Each differential pair should be routed together, minimizing the number of vias through which the signal lines are routed. The distance separating the two traces of the differential pair should be kept to a minimum.

In order to achieve optimal input TMDS signal quality, follow the layout guidelines below:

- Lay out all differential pairs with a controlled differential impedance of 100 Ω.
- Cut out all ground and power copper planes that are less than 45 mils underneath the TMDS traces near the receiver with the dimensions shown in Figure 9.2.
- If ESD suppression devices or common mode chokes are used, place them near the HDMI connector, away from the SiI9127A/SiI1127A package. Do not place them over the ground and power plane cutout near the receiver.

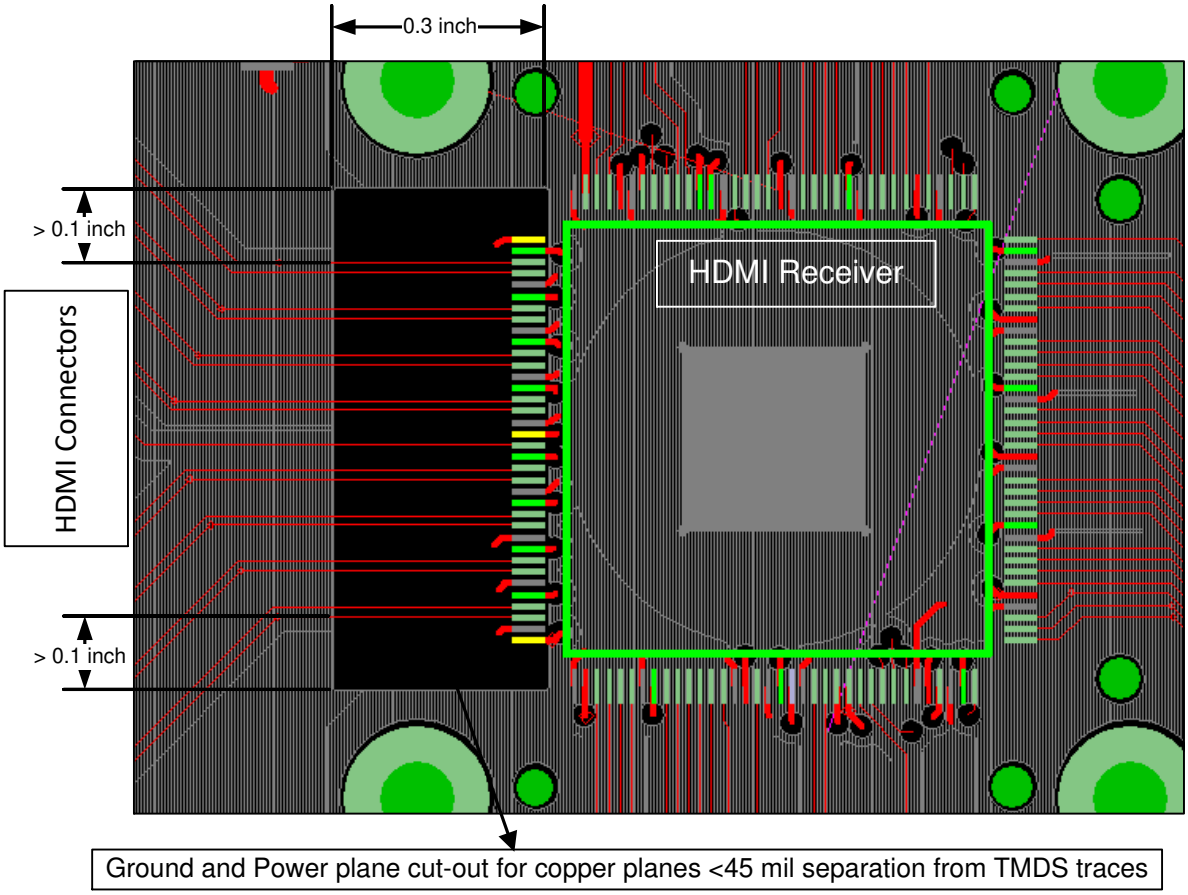


Figure 9.2. Cut-out Reference Plane Dimensions

In Figure 9.3, which is a representation of a PCB containing HDMI connectors and the receiver, the sixteen TMDS traces are connected directly from the HDMI connectors (shown on the left in the figure) to the pins on the SiI9127A/SiI1127A receiver (shown on the right). Trace differential impedance should be 100 Ω for each pair and 50 Ω single-ended if possible. Trace width and pitch depends on the PCB construction. Not all connections are shown; the drawing demonstrates routing of TMDS lines without crossovers, vias, or ESD protection. Refer also to Figure 9.9.

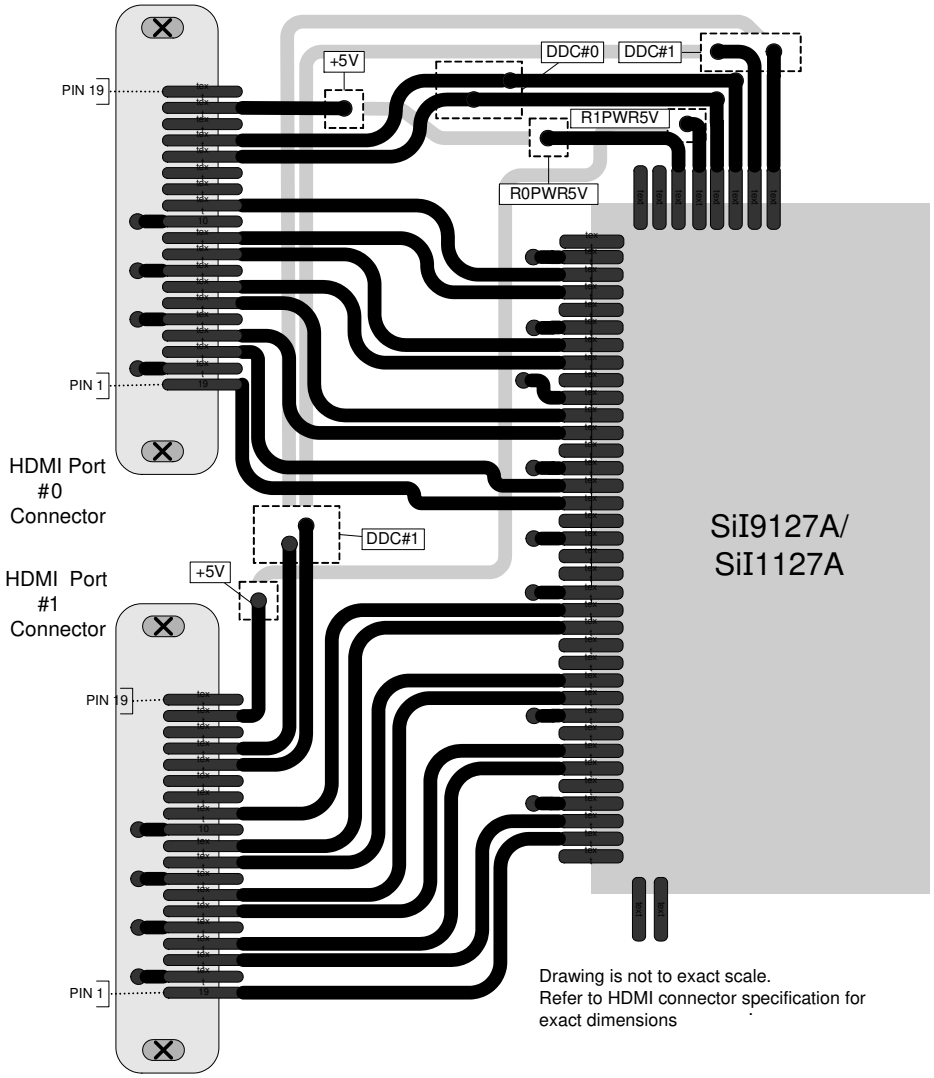


Figure 9.3. HDMI to Receiver Routing – Top View

9.7. EMI Considerations

Electromagnetic interference is a function of the board layout, shielding, receiver component operating voltage, and frequency of operation, among other factors. When attempting to control emissions, do not place any passive components on the differential signal lines other than the essential ESD protection described earlier. The differential signaling used in HDMI is inherently low in EMI as long as the routing recommendations noted in the Receiver Layout section are followed.

The PCB ground plane should extend unbroken under as much of the SiI9127A/SiI1127A chip and associated circuitry as possible, with all ground pins of the chip using a common ground.

9.8. Typical Circuit

Representative circuits for application of the SiI9127A/SiI1127A receiver chip are shown in Figure 9.4 through Figure 9.8. For a detailed review of your intended circuit implementation, contact your Lattice Semiconductor representative.

9.8.1. Power Supply Decoupling

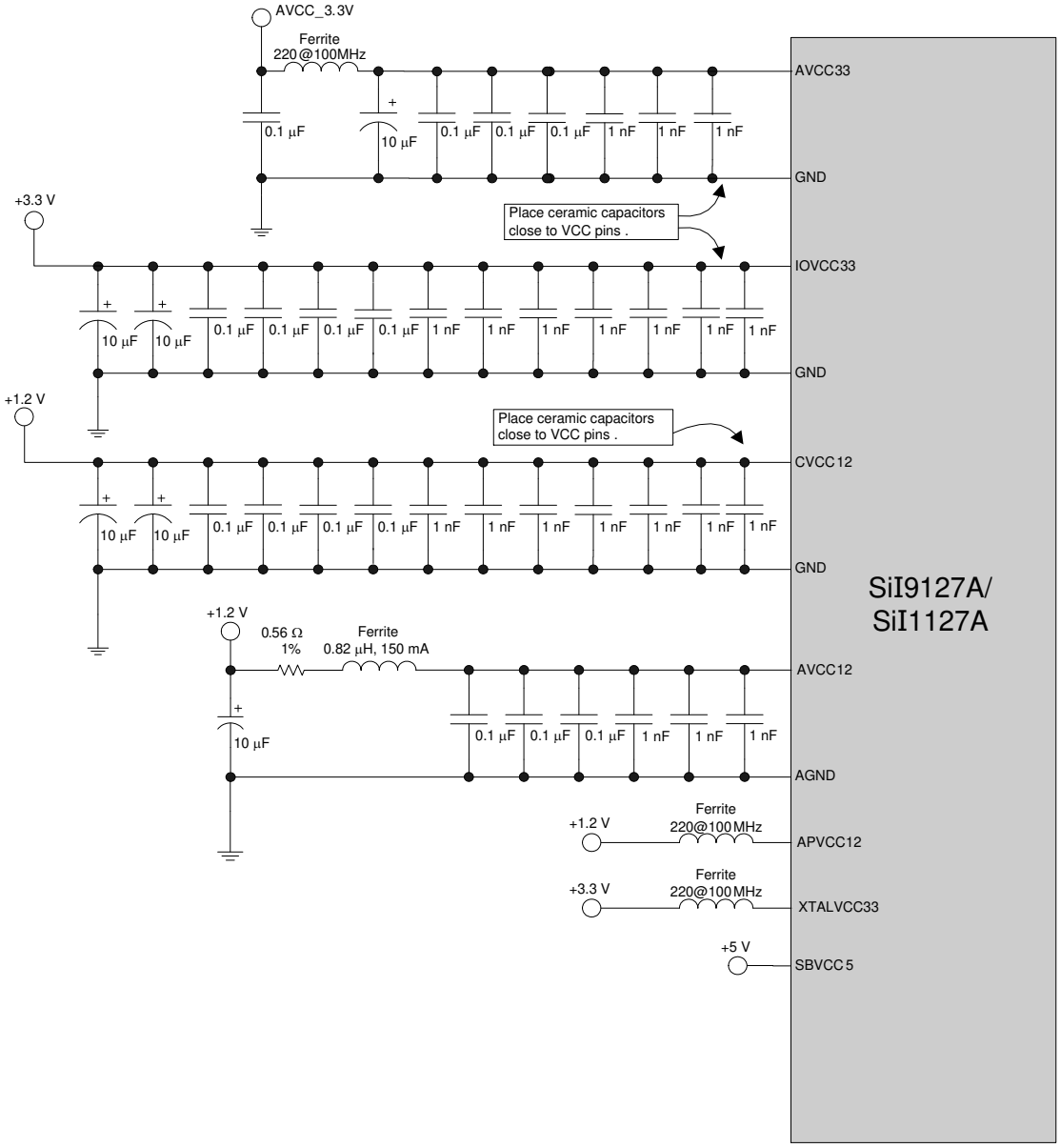


Figure 9.4. Power Supply Decoupling and PLL Filtering Schematic

The ferrite on AVCC33 attenuates noise above 10 kHz. A parasitic resistor helps to minimize the peaking. An example of a surface mount device is the MLF2012 Series SMD inductors from TDK.

9.8.2. HDMI Port Connections

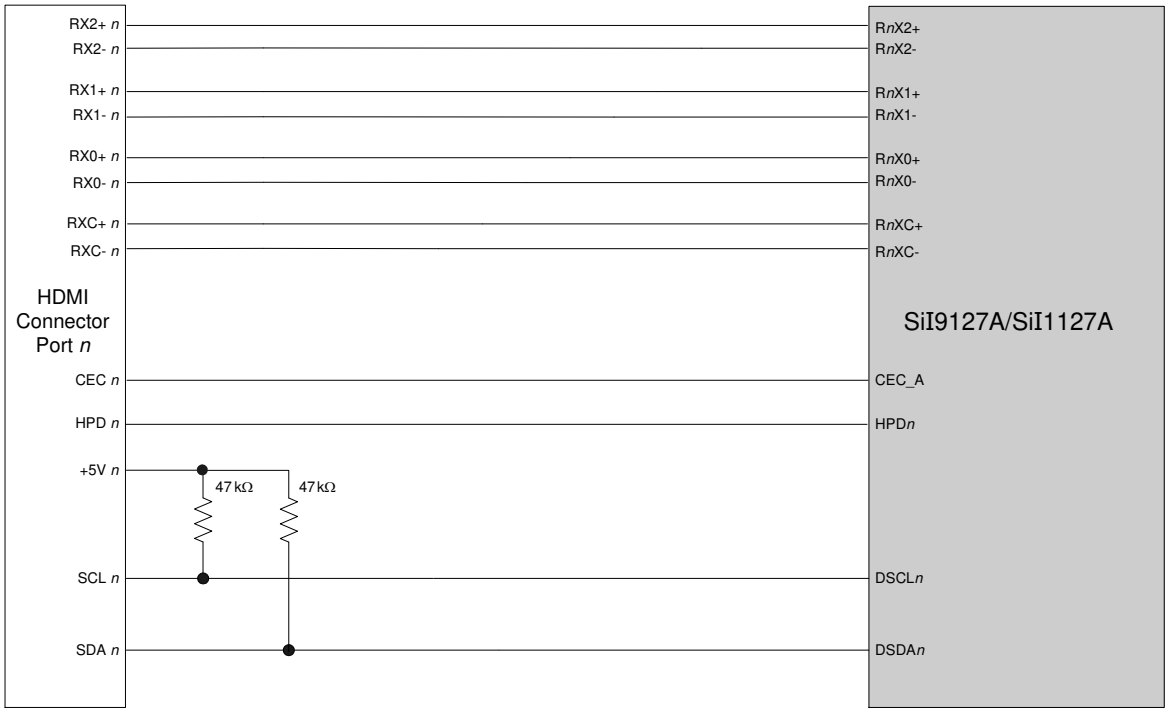


Figure 9.5. HDMI Port Connections Schematic

Note: Repeat the schematic for each HDMI input port on the receiver.

9.8.3. Digital Video Output Connections

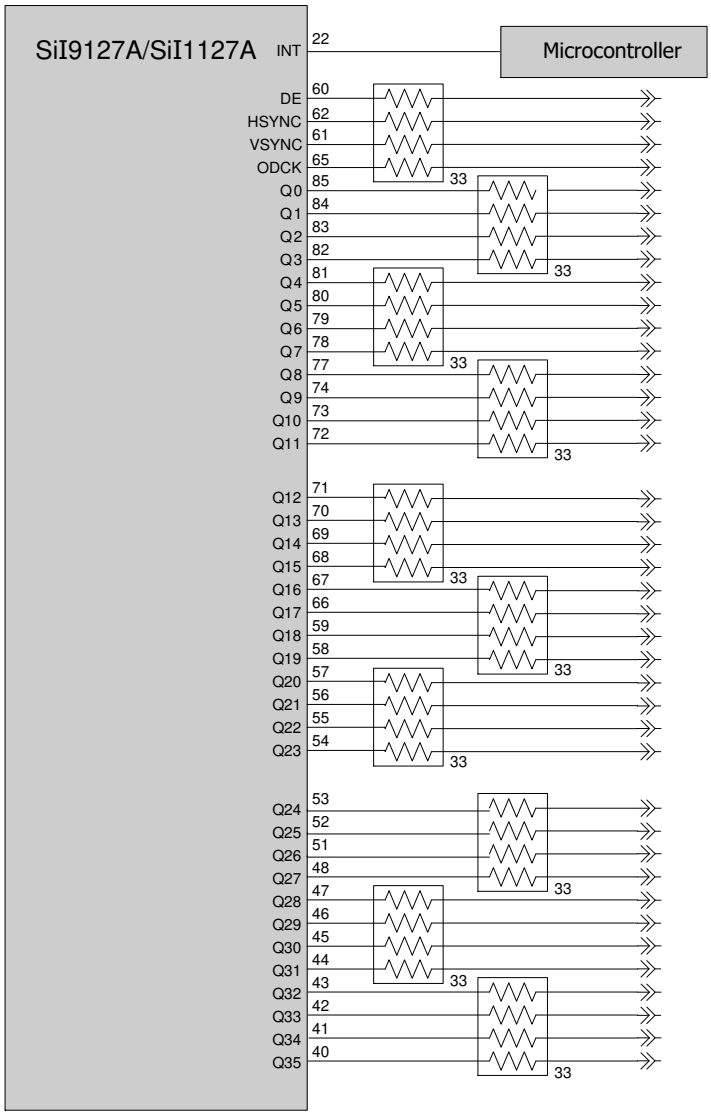


Figure 9.6. Digital Display Schematic

The 3.3 V to the level-shifters and pull-up resistors should be powered-down whenever the 3.3 V is powered-down on the receiver itself.

The receiver INT output can be connected as an interrupt to the microcontroller, or the microcontroller can poll register 0x70 (INTR_STATE) to determine if any of the enabled interrupts have occurred. Refer to the SiI-PR-1033 Programmer Reference for details. The receiver VSYNC output can be connected to the microcontroller if it is necessary to monitor the vertical refresh rate of the incoming video.

9.8.4. Digital Audio Output Connections

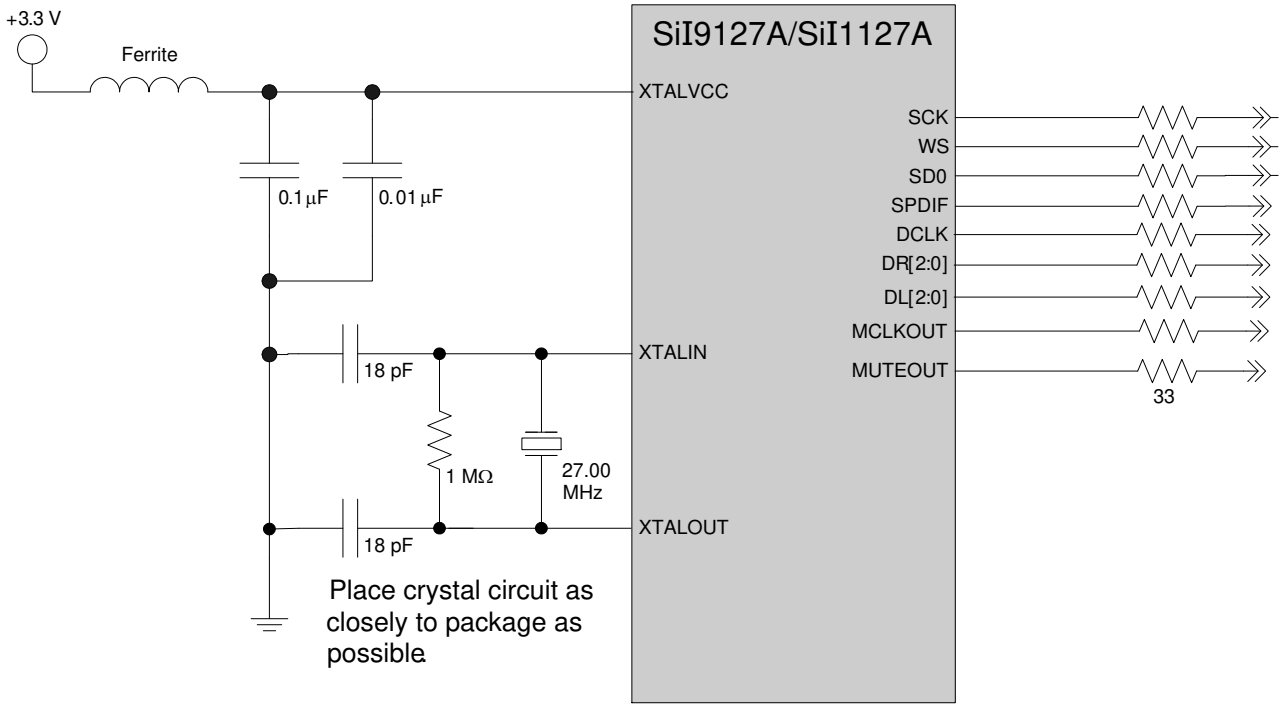


Figure 9.7. Audio Output Schematic

9.8.5. Control Signal Connections

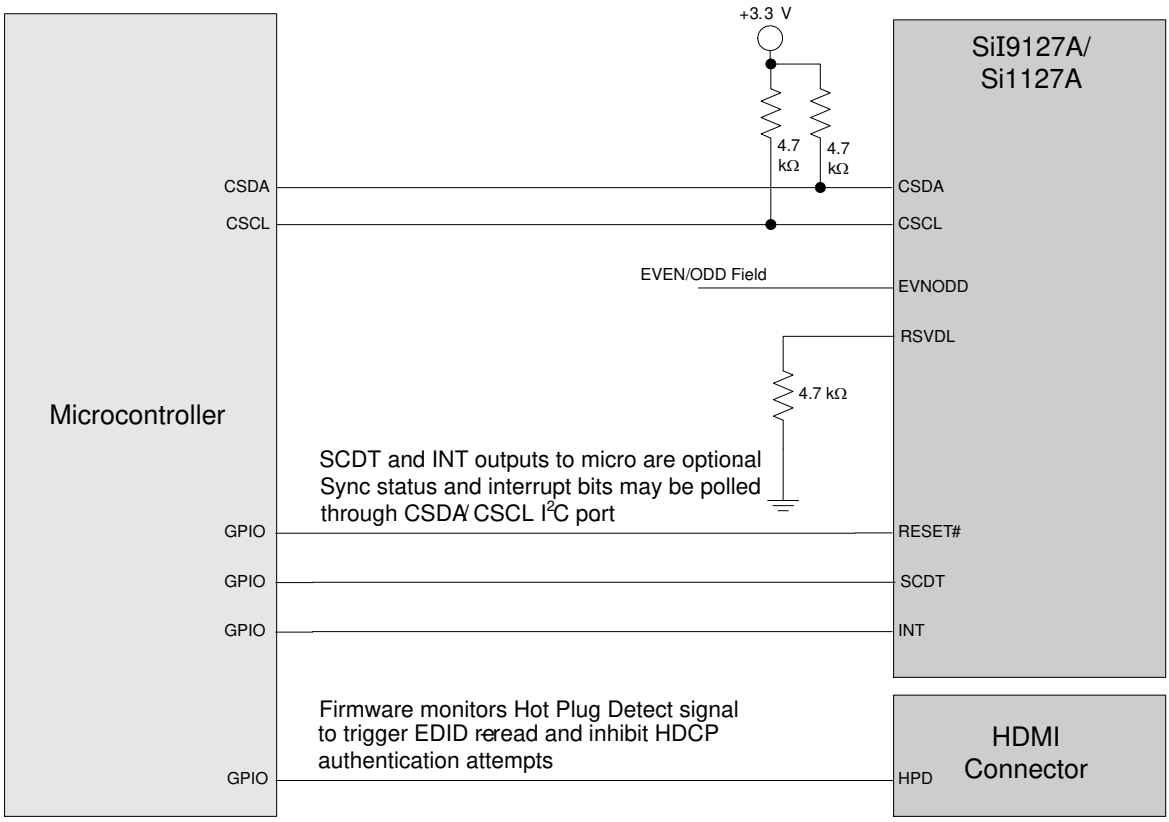


Figure 9.8. Controller Connections Schematic

9.9. Layout

Figure 9.9 shows an example of routing TMDS lines between the SiI9127A/SiI1127A device and the HDMI connector.

9.9.1. TMDS Input Port Connections

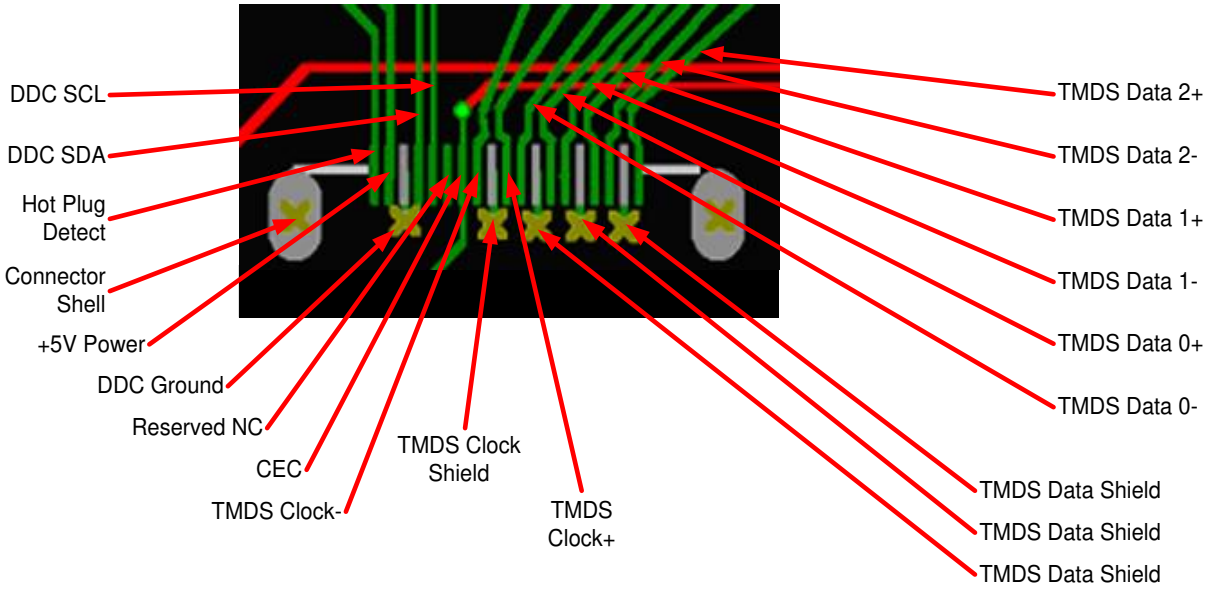


Figure 9.9. TMDS Input Signal Assignments

10. Package Information

10.1. ePad Requirements

The SiI9127A/SiI1127A receiver is packaged in a 128-pin, 14 mm x 14 mm TQFP package with an ePad that is used for the electrical ground of the device and for improved thermal transfer characteristics. The ePad dimensions are 4.445 mm x 4.0604 mm ±0.15 mm. Soldering the ePad to the ground plane of the PCB is ***required*** to meet package power dissipation requirements at full speed operation, and to correctly connect the chip circuitry to electrical ground. A clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical shorts.

The thermal land area on the PCB may use thermal vias to improve heat removal from the package. These thermal vias also double as the ground connections of the chip and must attach internally in the PCB to the ground plane. An array of vias should be designed into the PCB beneath the package. For optimum thermal performance, the via diameter should be 12 mils to 13 mils (0.30 mm to 0.33 mm) and the via barrel should be plated with 1-ounce copper to plug the via. This design helps to avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be tented with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

Package stand-off when mounting the device also needs to be considered. For a nominal stand-off of approximately 0.1 mm the stencil thickness of 5 mils to 8 mils should provide a good solder joint between the ePad and the thermal land.

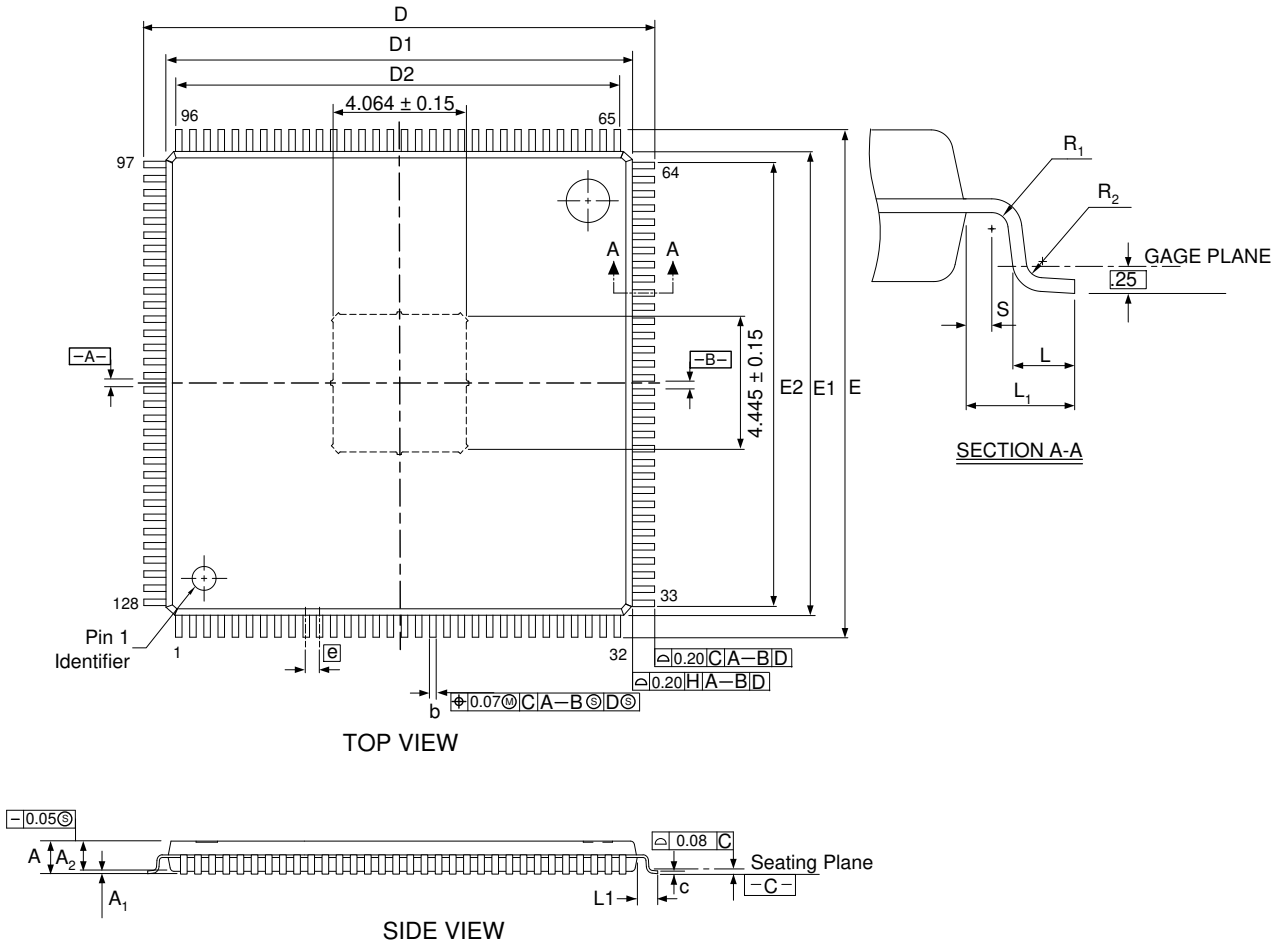
Figure 10.1 on the next page shows the package dimensions of the SiI9127A/SiI1127A receiver.

10.2. PCB Layout Guidelines

Refer to Lattice Semiconductor application note *PCB Layout Guidelines: Designing with Exposed Pads* (see Lattice Semiconductor Documents on page 74) for basic PCB design guidelines when designing with thermally enhanced packages using the exposed pad. This application note is intended for use by PCB layout designers.

10.3. Package Dimensions

Figure 10.1 shows the layout and dimensions of the 128-pin TQFP package. Package drawings are not to scale.



JEDEC Package Code MS-026-AFB

Item	Description	Typ	Max
A	Thickness	1.10	1.20
A1	Stand-off	0.10	0.15
A2	Body thickness	1.00	1.05
D	Footprint	16.00	
E	Footprint	16.00	
D1	Body size	14.00	
E1	Body size	14.00	
D2	Lead Row Width	12.40	
E2	Lead Row Width	12.40	

Item	Description	Typ	Max
b	Lead width	0.16	0.23
c	Lead thickness	—	0.20
e	Lead pitch	0.40	
L	Lead foot length	0.60	0.75
L1	Lead length	1.00	

Dimensions are in millimeters.

Overall thickness A = A1 + A2.

Figure 10.1. 128-Pin TQFP Package Diagram

10.4. Marking Specification

Figure 10.2 shows the markings of the SiI9127A package. This drawing is not to scale. Refer to the specifics in Figure 10.1 on the previous page. Figure 10.3 shows the alternate marking diagram for SiI9127A/SiI1127A.

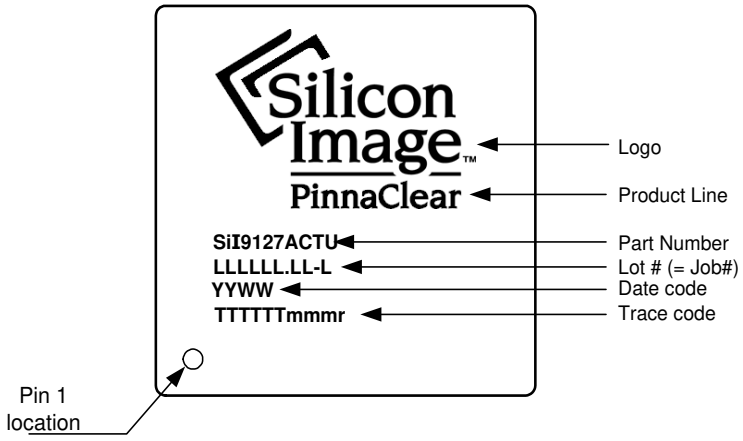


Figure 10.2. Marking Diagram of SiI9127A

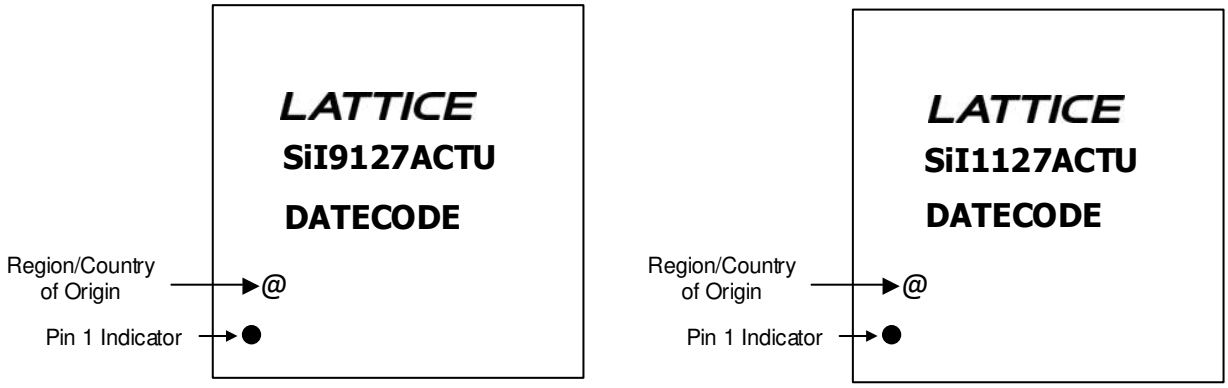


Figure 10.3. Alternate Marking Diagram

10.5. Ordering Information

Production Part Numbers:

TMDS Input Clock Range	Part Number
25 MHz–225 MHz	SiI9127ACTU
25 MHz–225 MHz	SiI1127ACTU

The universal package may be used in lead-free and ordinary process lines.

References

Standards Documents

This is a list of standards abbreviations appearing in this document, and references to their respective specifications documents.

Abbreviation	Standards publication, organization, and date
HDMI	*High-Definition Multimedia Interface*, Revision 1.4b, HDMI Consortium; October 2011 *High-Definition Multimedia Interface*, Revision 1.4a, HDMI Consortium; March 2010
	High Definition Multimedia Interface, Revision 1.3, HDMI Consortium; June 2006
HCTS	*HDMI Compliance Test Specification,* Revision 1.2a, HDMI Consortium; December 2005
HDCP	*High-bandwidth Digital Content Protection,* Revision 1.3, Digital Content Protection, LLC; December 2006
E-EDID	*Enhanced Extended Display Identification Data Standard,* Release A Revision 1, VESA; Feb. 2000
E-DID IG	*VESA EDID Implementation Guide*, VESA; June 2001
CEA-861	*A DTV Profile for Uncompressed High Speed Digital Interfaces,* EIA/CEA; January 2001
CEA-861-B	*A DTV Profile for Uncompressed High Speed Digital Interfaces*, Draft 020328, EIA/CEA; March 2002
CEA-861-D	*A DTV Profile for Uncompressed High Speed Digital Interfaces,* EIA/CEA; July 2006
EDDC	*Enhanced Display Data Channel Standard,* Version 1.1, VESA; March 2004

Standards Groups

For information on the specifications that apply to this document, contact the responsible standards groups appearing on this list.

Standards Group	Web URL
ANSI/EIA/CEA	http://global.ihs.com
VESA	http://www.vesa.org
DVI	http://www.ddwg.org
HDCP	http://www.digital-cp.com
HDMI	http://www.hdmi.org

Lattice Semiconductor Documents

This is a list of the related documents that are available from your Lattice Semiconductor sales representative. *The Programmer's Reference requires an NDA with Lattice Semiconductor.*

Document	Title
SiI-PR-1033	*SiI9127A/SiI1127A HDMI Receiver with Deep Color Outputs Programmer Reference*
SiI-PR-0041	*CEC Programming Interface (CPI) Programmer Reference*
SiI-AN-0129	*PCB Layout Guidelines: Designing with Exposed Pads Application Note*

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

Revision History

Revision D, May 2017

Figure 10.3. Alternate Marking Diagram added per PCN13A16.

Revision C, February 2016

Added SiI1127A receiver support. Updated to latest template.

Revision B, December 2012

Added local I^2C device addresses and 3D video format support.

Revision A03, September 2010

Removed Patent information from DB, rolled the revision for DS.

Revision A02, May 2010

Rewrite page 1; minor content corrections; light copyedit; update package drawing; prepare Data Brief.

Revision A01, April 2009

Removed audio downsampling, output delay control, video output pull-down information; updated specifications and layout.

Revision A, October 2008

First production release.

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