RSL15 Evaluation and Development Board User's Manual

EVBUM2757/D

INTRODUCTION

Purpose

This manual provides information on the hardware configuration and use of the RSL15 Evaluation and Development Board.

The Evaluation and Development Board (referred to as the EVB) is designed to be used with the RSL15 Software development kit. It is intended for evaluating the performance and capabilities of RSL15, and for developing software applications for this device. The Software Development Kit is available at www.onsemi.com/rsl15.

Conventions

In this manual, component and pin names are shown in a `CAPITALIZED MONOSPACE` font.

Manual Organization

The RSL15 Evaluation & Development Board User Guide contains the following sections:

- "Introduction" describes the purpose of this manual, explains how the manual is organized, and provides a list of suggested reading for more information.
- "Board Design and Overview" provides an overview of the Evaluation and Development Board as described in this manual.
- "Configuration" provides detailed information about the Evaluation and Development Board. This chapter contains information on the following topics:
  - Automatic switching power supply
  - SEGGER® J–Link® on–board Debug Port
  - RF Outputs
  - General Purpose Input/Output (GPIO)
  - Test Points
  - Indicator LEDs

Further Reading

For any technical information not covered in this manual, refer to the following documents:

- The searchable HTML documentation
- RSL15 Evaluation and Development Board Schematics
- RSL15 Evaluation and Development Board 3D Model

The above documentation can be found at www.onsemi.com/rsl15.

(Top Side)

(Bottom Side)

Figure 1. RSL15 Evaluation and Development Board Overview

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BOARD DESIGN & OVERVIEW

Introduction

The RSL15 Evaluation and Development Board is designed for simplicity of use when evaluating capabilities and developing applications for the RSL15 Bluetooth Low Energy Wireless MCU. For more information about the RSL15 System on Chip, please visit www.onsemi.com/rsl15. Note that the board features the RSL15 variant with 512 kB of Flash. For information on how to get the board connected and programmed quickly, see the RSL15 Getting Started Guide.

The EVB provides configuration options available and features that are intended to provide an easy−to−use development experience. Some of these features include an automatic switching power supply between USB and battery power, and a DIP switch for quickly disconnecting the J−Link OB MCU from the RSL15, usually for accurate power measurements.

The RSL15 EVB includes SEGGER J−Link on−board technology that supports easy development and debugging through a single USB cable. The RSL15 Evaluation and Development Board main functional blocks are presented in Figure 1.

RSL15 Evaluation and Development Board Features

The RSL15 Evaluation and Development Board enables developers to evaluate the performance and capabilities of RSL15, and to develop, demonstrate, and debug applications. Key features of the EVB include:

- Easy code download and debugging with SEGGER J−Link on−board technology
- JTAG debug port accessible via 10−pin header
- Automatic power supply switching between battery and USB
- Access to all RSL15 interfaces and GPIOs via standard 0.1 inch headers
- 2 push button switches
  - 1 dedicated to resetting the device via the NRESET pin
  - 1 connected to GPIO0
- Test points and GND hooks for easy probing
- CR2032 Battery Holder
- Simple configuration for power measurements
- Integrated PCB antenna with matching and filtering network
- UFL connector used for conducted RF connections

CONFIGURATION

Power Supply

The RSL15 Evaluation and Development Board is equipped with an easy−to−use power supply. The Board can be powered from three sources:

- A CR2032 standard 3.0 V battery inserted into the battery holder
- Power from the USB connection, 5 V, regulated down to 3.0 V by an on−board regulator
- An external power source connected to headers on board

In the default configuration out of the box, the board sources VBAT from VOUT, and VDDO is shorted to VBAT. VOUT is the output of the automatic switching power supply, sourced from the CR2032 battery or USB connection.

The on−board LEDs are guaranteed to work at the default 3.0 V level for VDDO. Below the 3.0 V level, the BLUE LED might not illuminate. The green LED illuminates at a voltage level of 1.7 V or above.

The NRESET pad of the device has an internal pull−up resistor to VDDO. If VDDO is left unpowered, the NRESET pad will be left floating, possibly resulting in unintended resets. For this reason, it is recommended to always have VDDO powered.

WARNING: The absolute maximum safe voltage for this product is 3.6 V. Any overvoltage conditions are likely to damage the device. 4.3 V Li−Ion CR2032 batteries cannot be used directly in the battery holder.

Configuration of the power supply is achieved with the following configuration headers shown in Table 1:

Table 1. POWER SUPPLY CONFIGURATION HEADERS

Designator	Function
VBAT−SEL	– Main configuration header, selects the source for VBAT – Short pins 3 & 2 (labeled VOUT and VBAT) for sourcing power from the battery or USB connection. **DEFAULT POSITION** – Remove the jumper and connect an external power source to pin 2 (labeled VBAT) and a GND connection to power the board from an external power source. – Short pins 1 & 2 (labeled VBAT and 3V0) to bypass the load switch devices and power the RSL15 from the on−board regulator directly.
VDDO−EN	Short this header to connect VBAT and VDDO together. Pin 1, labelled VDDO, can be used to connect an external power source. This header is shorted by **DEFAULT**.

VBAT and VDDO can additionally be powered from the GPIO headers, with a couple of standard 0.1 inch pins available for such purposes.

Table 2. MINIMUM AND MAXIMUM VOLTAGES

Power Supply	Input Voltage		
	Min	Typ	Max
VBAT	1.2		3.6
VDDO	1.2		3.6
Regulated voltage (VOUT)		3.0	

For a visual representation of the power supply system's logical layout, see the RSL15 Evaluation and Development Board Schematic.

Automatic Switching Power Supply

The RSL15 Evaluation and Development Board is designed to automatically switch over to USB power if both the battery and the USB cable are connected. This is intended to save battery life without the user having to remove and re−insert the battery.

J−Link OB Microcontroller Power Supply

The J−Link On−board MCU is powered by a 3.0 V LDO regulator, which is in turn powered by a 5 V rail supplied by the USB connection.

Taking Power Measurements

The RSL15 Evaluation and Development Board has been designed in a way that facilitates an ease of transition between taking power measurements and downloading new firmware. The Board is designed so that all external devices that could cause leakage, causing increased currents in power measurements, can be isolated from the RSL15. This is accomplished using the 8−pin DIP switch, labelled DEBUG−EN. In the off position, the J−Link On−board MCU is isolated from the RSL15.

Power Measurement Setup

This section details the hardware configuration required in order to take accurate power measurements after loading a firmware application onto the board and covers potential power supply options. There are various methods of providing power to the RSL15 Evaluation and Development Board while taking power measurements. The default power configuration consists of a USB connector plugged into the board which provides 5 V at VBUS which is regulated down to 3 V to power the device. The board can also be powered via a battery holder located on its backside. The circuit is configured in such a way that if the battery is inserted at the same time as the USB cable, all power will come from the USB connector. This connects to the two header pins on the board, namely, VBAT−SEL and VDDO−EN. When measuring for power consumption, it is recommended to power and measure the board using a power analyzer or use an ammeter to measure power consumption if the board is being supplied power through other means.

The setup procedure for obtaining accurate power measurements is as follows:

1. Move all of the switches on the DEBUG−EN switch to the **OFF** position.
2. Remove the shorting jumper from the VBAT−SEL header.
3. If using an ammeter and if VBAT and VDDO are the same current, connect it in series across the VOUT and VBAT pins on the VBAT−SEL header.
   OR
   If using an ammeter and if VBAT and VDDO have separate current supplies, connect an ammeter in series across both VBAT−SEL and VDDO−EN for a total of 2 ammeters. Subtracting the power consumption value measured by the ammeter on VDDO−EN (power consumption of VDDO) from the value measured at VBAT−SEL (power consumption of VOUT) will result in the power consumption of VBAT.
   OR
   If using a power analyzer, connect it in parallel, using any VBAT pin and any ground pin.
4. In order to upload new code, leave the power source on, ensuring VBAT and VDDO are powered. Flip the DIP switches to the **ON** position and ensure that the USB−C cable is connected. This is all that is required in order to download new firmware.

Replicate Sleep Mode Sample Application Power Consumption Values

This section will detail how to configure the RSL15 Evaluation and Development Board and take low power consumption measurements while the device is in Sleep Mode with the RTC timer enabled, using the XTAL32K clock or the RC32K clock as the STANDBYCLK with no RAM retained or various levels of RAM retention to replicate datasheet values with a power analyzer. To understand the Sleep Mode sample code, refer to the readme file in the project folder.

The procedure detailed here will allow for the replication of datasheet values for the Sleep Mode sample application. This procedure is specific to this sample application and not for general use. However, following this procedure is a simple way to learn the power consumption measurement procedure.

NOTE: Many SDK samples do not provide the absolute lowest power consumption values.

Before measuring power consumption, load the Sleep Mode sample application onto the RSL15 Evaluation and Development Board with the desired settings:

1. Disable the usage of GPIOs for lowest consumption.
2. Configure either the 32 kHz crystal (XTAL32) or the 32 kHz RC oscillator (RCOSC32) as the source for STANDBYCLK.
3. Configure the DCDC regulator for either buck mode or LDO mode.
4. Configure the RTC clock wakeup duration. This determines the time between device wakeup states. When measuring power consumption, ensure a large enough time difference between wakeup pulses. There is a capacitor on VCC which is a part of the DC/DC regulator that powers the device and the wakeup period should allow for this capacitor to fully discharge, thus resulting in accurate values. A longer wakeup period is recommended since the measurement values in the datasheet were taken after the VCC capacitor had discharged. Power consumption values will be an average value taken over 4 seconds. Therefore a wakeup period of at least 8 seconds is ideal.
5. In order to change the amount of RAM that is kept in retention, the #defines in the code as well as the linker script will need to be modified.

Take the power consumption measurements:

6. Follow the hardware setup steps in section Power Measurement Setup.
7. Turn on the measurement instrument.
8. Set the output voltage. This will depend on the mode the DCDC is in. If in LDO mode, the output voltage should be 1.25 V or 1.5 V. If in buck mode, the output voltage should be 1.8 V or 3 V.
9. Set the output current range to the lowest setting that permits accurate measurements. Note that selection of an appropriate measurement range when measuring low currents, especially in the nA range, is extremely important for generating accurate results.
10. Enable the power supply such that power consumption measurements can be taken.
11. On the RSL15 Evaluation and Development Board, press the RESET button to restart the sample application on the board. As a best practice, this should be done in between all measurements.
12. Measure the power consumption over a period of 4 seconds, preferably right before a wakeup pulse to ensure that the VCC capacitor has discharged completely. Take a minimum of 3 measurements and average these values to obtain the most accurate results.

Communication

There are two ways of achieving communication with the RSL15 Evaluation and Development Board.

The USB−C 2.0 connection (J6) is connected to a J−Link onboard solution that provides an SWJ−DP for debugging the RSL15 at up to 4 MHz. The TC2050−IDC connector (J8 header) is used to program the Arm® Cortex®−M4 processor with J−Link firmware. The EVB is configured for this use case by default. See Figure 2. Standard USB connection.

In order for the USB connection to work, the shorting jumpers must be in their default position. The first jumper must be placed across VBAT and VOUT on the VBAT−SEL header. The second jumper must be placed on VDDO−EN, shorting VDDO and VBAT.

It is also possible to connect and debug the RSL15 via the 10−pin JTAG (JTAG header) connector. This connector is compatible with J−Link debugging devices when paired with an adapter: https://www.olimex.com/Products/ARM/JTAG/ARM−JTAG−20−10/. See Figure 3.

The simplest method for configuring the device to be programmed or debugged is by using the standard USB connection.

UART over J−Link On−board

When the RSL15 EVB is connected to a host Windows PC via the USB−C cable, a UART is available between the PC and the RSL15 via the J−Link On−board. If J−Link drivers are installed, the device shows up in Windows Device Manager under *Ports* as a *JLink CDC UART Port*. Standard software or libraries that are commonly used for serial monitor purposes work with this serial port. GPIO5 is connected to the TXD line of the J−Link OB UART, and GPIO6 is connected to RXD. Therefore, in firmware on the RSL15, GPIO6 and GPIO5 need to be configured in the same manner, where the RSL15 GPIO6 is configured as the UART TXD pin and GPIO5 is configured as the RXD pin. The UART supports up to 115200 baud.

The UART can be enabled or disabled mechanically on the EVB, using the DIP switch labelled DEBUG−EN. If position 7 and 8 on the DIP switch are placed in the OFF position, then the UART is disabled. Placing both position 7 and 8 back to the ON position re−enables the UART. Position 3 of the DIP switch must be in the ON position as well, as this enables the level shifters between the J−Link OB and the RSL15.

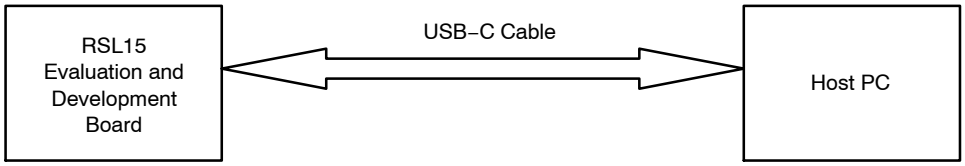

Figure 2. Standard USB Connection

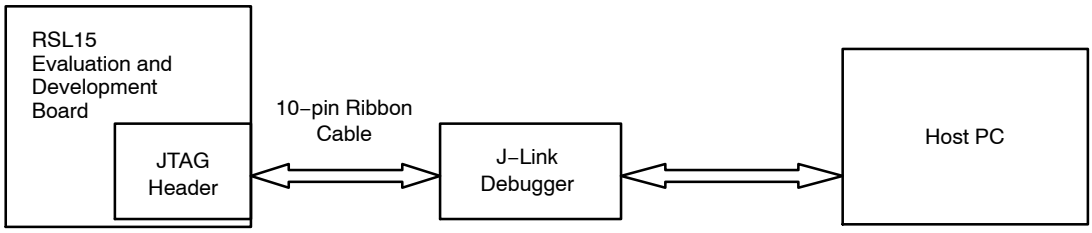

Figure 3. J−Link Connection

General Purpose Input/Output (GPIO)

The RSL15 Evaluation and Development Board contains 15 GPIO signals available on several inline headers. The headers provide access to all GPIO signals, which in turn provide access to a wide variety of interfaces (GPIO, SPI, UART, etc.). See Table 3 for pinouts. VDDO, VBAT and GND are present on the end of each header.

Table 3. GPIO REFERENCE

GPIOs	GPIO Header Pin	Header	Alternate Function On Board
0	5	GPIO−A	Wakeup source, SW1
1	7	GPIO−A	Wakeup source, RTC clock input
2	9	GPIO−A	JTAG TDO*, Wakeup source
3	11	GPIO−A	JTAG TDI*, Wakeup source,
4	12	GPIO−A	JTAG TRST*,
5	10	GPIO−A	UART RXD (from RSL15)
6	8	GPIO−A	UART TXD (from RSL15)
7	6	GPIO−A	
8	5	GPIO−B	GREEN LED
9	7	GPIO−B	
10	9	GPIO−B	BLUE LED
11	11	GPIO−B	
12	12	GPIO−B	
13	10	GPIO−B	
14	8	GPIO−B	
15	6	GPIO−B	

*Assigning a function to these GPIOs other than JTAG pins means they cannot be used for the JTAG connection.

The RSL15 Evaluation and Development Board also has one momentary switch that can be used as a momentary hard pull−down on GPIO0 (SW1). The RESET switch can be used to reset the RSL15.

For more information on the GPIOs, refer to the RSL15 Hardware Reference Manual.

Jumper Wires Female to Female 6.00 in (152.40 mm) 28 AWG can be used to connect GPIOs to external peripherals or instruments. Such cables can be procured from SparkFun Electronics PN: PRT−12796.

RF

The RSL15 Evaluation and Development Board contains two features that assist with evaluating the capabilities of the RSL15 and assist in developing Bluetooth applications. These two features are the on−board antenna and the UFL connector. The functions are switched between via a 0 Ω resistor soldered onto part footprint R4.

Integrated PCB Antenna

The integrated PCB antenna is the default option for radiating the RF output of the RSL15. If it is desired to use the on−board antenna, no changes need to be made out of the box.

UFL Connector

Placed on the PCB is a UFL connector that can be used to connect to the conducted RF output of the RSL15. By default, the UFL connector is disconnected from the RF output. In order to connect the UFL connector to the RF output, R4 must be uninstalled and R5 populated. To switch back to the integrated antenna, R4 must be populated and R5 uninstalled. Note that R4 and R5 share a pad.

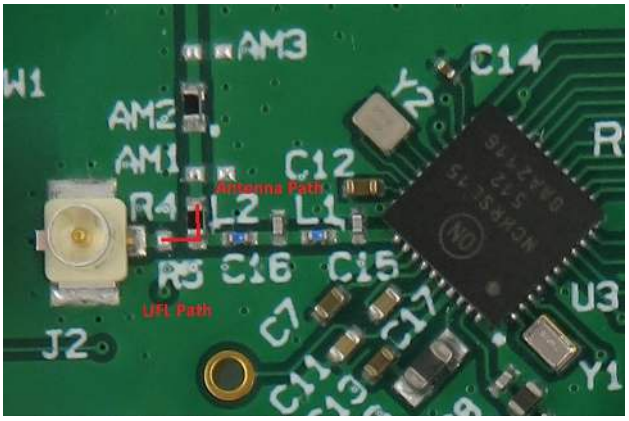

Figure 4. Selection of RF Path Through R4, R5 (0 Ω Resistors)

To connect any RF instrument to the RSL15 RF output, an SMA to UFL adapter cable can be used. Such cables are available from Taoglas Limited PN: CAB.721.

DIP Switch

Present on the RSL15 Evaluation and Development Board is an 8−pin DIP switch that is mainly used for isolating the J−Link OB MCU from the RSL15. However, some alternate configurations are possible, given the flexible nature of the 8 individual switches. Connected to the switch are VDDO, NRESET, JTAG signals, and UART TXD/RXD. Each of these signal lines can be individually connected or disconnected via the DIP Switch. The positions of the signals are outlined in Table 4. Pins 1 and 2 are closest to the ON marking on the switch.

Table 4. DIP SWITCH PINOUT

Pin Numbers	Signal Description
1 & 2	JTMS
3 & 4	JTCK
5 & 6	VDDO (When turned off, disables level translators)
7 & 8	NRESET/JRST
9 & 10	GPIO3/TDI
11 & 12	GPIO2/TDO
12 & 13	GPIO5/J−Link OB TXD
14 & 15	GPIO6/J−Link OB RXD

Test Point Headers

Table 5 shows a list of headers or test points that can be used to measure various nodes on the board.

Table 5. MEASUREMENT TEST POINTS

Designator	Measurement Location
GND−TP	A ground hook is available in the bottom left of the board, on the opposite side of the board from the USB port.
VDDA	A testpoint for measuring VDDA is located close to the antenna.
VBAT−SEL	– Located on top of the board, below the DIP switch – Pin 1: 3.0 V linear regulator output – Pin 2: VBAT for RSL15 – Pin 3: VOUT, output of load switches
VDDO−EN	– Located on top of the board, below the VBAT−SEL header – Pin 1: VDDO rail – Pin 2: VBAT rail
GPIO−A, GPIO−B	– Located on the top right side of the board – Pin 1: VBAT rail – Pin 3: VDDO rail – Pin 2 & 4: GND

Indicator LEDs

There are three LEDs present on the RSL15 Evaluation and Development Board. The first LED is an indicator of communication for the J−Link on−board debug probe, and is found on the backside of the Board. The LED stays a solid green or flicker slightly if communication is normal. If there are communication issues, the LED noticeably flashes on and off.

The other two LEDs on the board are connected to GPIOs and are intended to be used for indication in applications. Sample applications available in the RSL15 SDK use these LEDs. Specifically, the GREEN LED is connected to GPIO8, and the BLUE LED is connected to GPIO10.

The on−board LEDs are guaranteed to work at the default 3.0 V level for VDDO. Any voltage level below this results in lowered brightness or failure to operate correctly.

Export Control Classification Number (ECCN)

The ECCN designation for RSL15 is 5A991.g.

APPENDIX A

Headers & Connectors

This section contains a list and description of all headers present on the RSL15 Evaluation and Development Board, shown in Table 6.

Table 6. LIST OF ALL HEADERS PRESENT

Designator	Description
J1	CR2032 battery holder. Li−Ion CR2032 batteries must not be used, as their voltage is typically > 4 V. Use standard 3 V CR2032 batteries.
VBAT−SEL	Used for selecting the source of VBAT, or for connecting an external source to VBAT directly. Connects VOUT (Output of on−board power supply) to VBAT by default. (Pins 2 & 3 are shorted.)
GND−TP	Ground test point, useful for attaching probes
VDDO−EN	Used for connecting VDDO to VBAT. Shorted by default.
J3	Used for connecting an external JTAG debug probe. Uses the standard 10−pin ARM JTAG connector.
GPIO−A	Contains pins for GPIOs 0−7, as well as VDDO, VBAT and ground.
GPIO−B	Contains pins for GPIOs 8−15, as well as VDDO, VBAT and ground.
VDDA	VDDA test point, used for measuring VDDA
J2	UFL type connector for connecting the RF output in a conducted manner to an external circuit (i.e., external antenna or measurement device). To enable this conducted path, 0 Ω resistor R4 must be de−soldered from its initial position and re−soldered after being rotated 90 degrees.
J6	USB−C 2.0 connector. This USB connector provides 5 V power to the device, as well as enabling programming and debug functionality through the J−Link OB solution.
J8	Header used for programming J−Link OB firmware onto the MCU. J−Link OB firmware comes pre−programmed from the factory. Users can ignore this header.
DEBUG−EN	Enables/disables the connection between the J−Link OB and the RSL15. Disconnecting the two devices allows for accurate power consumption measurements.

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