

Descriptions

LC5710S is a high efficiency LED driver in which a power MOSFET and a control IC are highly integrated.

The IC achieves buck/ boost/ buck-boost LED drive circuit.

Having a rich set of protection features, the IC can provide more cost-effective power supply systems with fewer external components.

Features

- Buck/ boost/ buck-boost
- High Efficiency $\eta > 90\%$ (typ.)
- $I_{LED} = 1.0 \text{ A (max.)}$
- $f_{OSC} = 100 \text{ kHz to } 500 \text{ kHz}$ (Externally Adjustabe)
- Current Setting with High Accuracy
- $V_{CS} = 100 \text{ mV} \pm 3\%$
- Dimming Control with High Accuracy PWM: 20 kHz DC: 0.2 V to 2 V
- Protections
 - Overcurrent Protection (OCP): Pulse-by-pulse Overvoltage Protection (OVP): Auto-restart Thermal Shutdown (TSD): Auto-restart LED Incorrect Connection Protection

Package

SOP8



Not to scale

Specifications

- Power Supply Voltage Range: 5 V to 58 V
- On-resistance $R_{DS(ON)}$: 550 m Ω (typ.)

Applications

- LED Lighting
- LCD Bulbs

Typical Application (Buck Converter)



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Contents

Descriptions	1
Contents	2
1. Absolute Maximum Ratings	-3
2. Recommended Operating Conditions	3
3. Electrical Characteristics	4
4. Block Diagram	-5
5. Pin Configuration Definitions	-5
6. Typical Application	6
7. Physical Dimensions	8
8. Marking Diagram	.9
9 Operational Description	10
91 PWM Current Control	0
9.2 LED Dimming	0
9.2.1 Analog Dimming	0
9.2.2 Digital Dimming 1	1
9.3 LED On/Off Function1	2
9.4 Overcurrent Protection (OCP) 1	2
9.5 Overvoltage Protection (OVP)	2
9.6 LED Incorrect Connection Protection1	3
9.7 Thermal Shutdown	4
9.8 Converter Type Selection	4
9.9 External Inductor Setting	5
9.10 Calculation of Power Dissination, Pp	17
9.10.1 Control Circuit Loss, PCONT	7
9 10 2 Switching Time of Power MOSFET	7
9 10 3 Switching Loss Psw of Power MOSFET	8
9.10.4 On-resistance Loss, Pox, of Power MOSFET	8
10. Design Notes 1	9
10.1 Thermal Derating Curve	9
10.2 External Components1	9
10.2.1 Inductor (L1)	9
10.2.2 Diode (Ds)1	9
10.2.3 Current Detection Resistor (Rcs)	9
10.2.4 Input Capacitor (C _{IN})	9
10.2.5 Output Capacitor (Cour) 1	9
10.2.6 Phase Compensation Circuit (Rs, Cs, Cp)	9
10.2.7 Frequency Setting Resistor (R _{RT})	9
10.3 Phase Compensation (COMP Pin)2	20
10.4 PCB Layout	21
11. Pattern Layout Example 2	24
12. Typical Characteristics2	26
Important Notes 3	32

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (–). Unless specifically noted, $T_A = 25$ °C.

Parameter	Symbol	Pins	Conditions	Rating	Unit
VIN Pin Voltage	V _{IN}	5–3		-0.3 to 60.0	V
SW Pin Voltage	V _{SW}	4–3		-0.3 to 60.0	V
CSP Pin Voltage	V _{CSP}	6–3		-0.3 to 60.0	V
CSN Pin Voltage	V _{CSN}	7–3		-0.3 to 60.0	V
CSP/CSN Pin Differential Voltage	V _{CSP_CSN}	6–7		-0.3 to 3.3	V
COMP Pin Voltage	V _{COMP}	1 –3		-0.3 to 3.3	V
DIM Pin Voltage	V _{DIM}	8–3		-0.3 to 3.3	V
RT Pin Voltage	V _{RT}	2–3		-0.3 to 3.3	V
Allowable Power Dissipation ⁽¹⁾	PD	_	(2)	1.2	W
Junction-to-GND Pin Thermal Resistance	$\theta_{J\text{-}L}$	_		59.0	°C/W
Junction-to-Ambient Thermal Resistance	$\theta_{J\text{-}A}$	—		82.8	°C/W
Junction Temperature ⁽³⁾	TJ	—	× ×	125	°C
Operating Ambient Temperature	T _{OP}	_		-40 to 125	°C
Storage Temperature	T _{STG}	-		-40 to 150	°C

2. Recommended Operating Conditions

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (-). Unless specifically noted $T_A = 25 \,^{\circ}C$

Parameter	Symbol	Min.	Max.	Unit	Remarks
Input Voltage Range	V _{IN}	5	58	V	
Output Cumont Danca(4)	Т	0	1	А	Buck ⁽⁵⁾
Output Current Range	lo	0	0.5	А	Boost/ Buck-boost ⁽⁶⁾
DIM Pin Voltage	V _{DIM}	V _{DIM(OFF)}	2.5	V	Analog Dimming
DIM Pin Dimming Frequency	\mathbf{f}_{DIM}	100	20000	Hz	PWM Digital Dimming
Inductor Ripple Current.	ΔI_L	0.1	0.4	А	
Operating Ambient Temperature Range	T _{OP}	-40	85	°C	

⁽¹⁾ Limited by junction temperature.

⁽²⁾ The IC is mounted on the glass-epoxy board (40 mm \times 40 mm) with copper area (25 mm \times 25 mm).

 $^{^{(3)}}$ The temperature detection of thermal shutdown is about 150 °C.

⁽⁴⁾ The IC should be used within the limited range as shown in Figure 10-1.

 $^{^{(5)}}$ In buck mode, the IC should be used in the range of $I_0 \le 1$ A and $\Delta I_L \le 0.4$ A.

 $^{^{(6)}}$ In boost/ buck-boost mode, the IC should be used in the range of $I_{O} \le 0.5$ A, $\Delta I_{L} \le 0.4$ A.

3. **Electrical Characteristics**

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (–). Unless specifically noted, $T_A = 25$ °C, $V_{IN} = 15$ V.

	/						
Parameter	Symbol	Pins	Conditions	Min.	Тур.	Max.	Unit
Operation Start Voltage	V _{IN(ON)}	5–3		3.8	4.1	4.5	V
Operation Stop Voltage	V _{IN(OFF)}	5–3		3.4	3.7	4.2	V
Operation Voltage Hysteresis	V _{IN(HYS)}	5–3		0.25	0.37	0.50	V
Circuit Current in Operation*	I _{IN(ON)}	5–3		_	1.6	_	mA
Circuit Current in Non- operation*	I _{IN(OFF)}	5–3	$V_{IN} = 3 V$	_	0.24	A.	mA
Switching Frequency 1	f _{OSC1}	—	$Rrt = 110 k\Omega$	80	100	135	kHz
Switching Frequency 2	f _{OSC2}	—	$Rrt = 18 k\Omega$	350	500	650	kHz
Minimum On-time	t _{ON(MIN)}	—	$V_{\text{COMP}} = 0 \text{ V}$	100	200	300	ns
Maximum Duty Cycle	D _{MAX}	_	$V_{\text{COMP}} = 2.8 \text{ V}$	84	90	95	%
Current Detection Threshold Voltage	V _{CS}	6–7		97	100	103	mV
SW Pin Limit Current	I _{SW(LIM)}	4–3		1.4	1.8	2.2	А
CSP Pin Current	I _{CSP}	6–3	A Y	22	35	50	μA
CSN Pin Current	I _{CSN}	7–3	607	5	9.5	15	μA
COMP Pin Source Current	I _{COMP(SO)}	1–3	$V_{CS} = 20 \text{ mV}$ $V_{COMP} = 2 \text{ V}$	-65	-50	-35	μA
COMP Pin Sink Current	I _{COMP(SI)}	1–3	$V_{CS} = 180 \text{ mV}$ $V_{COMP} = 2 \text{ V}$	35	50	65	μA
Error Amplifier Conductance*	G _M		$V_{CS} = 50 \text{ mV}$ to 150 mV	—	4.8	_	ms
Overvoltage Protection Threshold Voltage	V _{CS(OVP)}	6–7		140	150	160	mV
Watchdog Timer Setting Time*	twDT	—	$V_{CS} = 0 V$ $V_{COMP} > 2.1 V$	_	30	_	ms
DIM Pin Voltage at LED Turn-on	V _{DIM(ON)}	8–3		0.17	0.20	0.23	V
DIM Pin Voltage at LED Turn-off	V _{DIM(OFF)}	8–3		0.12	0.15	0.18	V
DIM Pin Hysteresis Voltage	V _{DIM(HYS)}	8–3		10	50	100	mV
TSD Operating Temperature*	T _{SD}	_			165		°C
Thermal Shutdown Temperature Hysteresis*	T _{SD(HYS)}	_			22		°C

* Guaranteed by design.

5.

4. Block Diagram





Pin Number	Pin Name	Description
1	COMP	Phase compensation pin. A resistor and a capacitor are connected in series between the COMP GND pins for compensation of the regulation control loop. A capacitor should be connected in parallel as needed.
2	RT	Frequency variable pin. An oscillation frequency adjustment resistor, R_{RT} , is connected between the RT pin and the GND pin.
3	GND	Ground pin
4	SW	Output pin
5	VIN	Power supply input pin. Recommended input voltage range is 5 V to 58 V. To supply the switching current to the IC, connect a capacitor between the VIN and GND pins.
6	CSP	Reference pin for current detection input. A current detection resistor, R _{CS} , is connected.
7	CSN	Current detection negative input pin. The detection resistor, R_{CS} , is connected to the anode side of the LED string via the overvoltage protection resistor, R_{OVP} .
8	DIM	Dimming signal input pin. The DC voltage or the PWM signal is input. Recommended input range of DC voltage is $V_{DIM(OFF)}$ to 2.5 V. Recommended frequency range of PWM signal is 100 Hz to 20 kHz. When the DIM pin voltage is lower than $V_{DIM(OFF)}$, the SW pin turns off.

6. Typical Application







7. Physical Dimensions

• SOP8 Packgae



8. Marking Diagram



9. Operational Description

For concise descriptions, this section employs notation systems that denote the electrical characteristics symbols listed in Section 3 and the electronic symbol names of the typical applications in Section 6. All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum.

9.1 PWM Current Control

The IC achieves the constant current control of the power supply output by using the PWM control of the peak current-mode method that enhances the response speed and provides stable operation. The oscillation frequency, f_{OSC} , is set within the range of 100 kHz to 500 kHz by a resistor, R_{RT} , that is connected between the RT and GND pins (see Figure 9-1). The oscillation frequency, f_{OSC} , is calculated by the following equation.





The current is controlled to be constant by detecting the current flowing to the power MOSFET, I_D , and the current flowing to the LED, I_{LED} . I_D is detected inside the IC. I_{LED} is detected by a current detection resistor, R_{CS} .

The IC controls the on-time of the internal power MOSFET so that the peak of the value generated from I_D approaches the target value generated from the voltage across R_{CS} , resulting in keeping I_{LED} constant.

ILED is calculated by the following equation.

$$I_{OUT} = \frac{V_{CS} - I_{CSN} \times (R_{CS} + R_{OVP})}{R_{CS}}$$
(2)

Where:

 I_{CSN} is the SW pin input current (9.5 μ A), V_{CS} is the current detection threshold voltage (100 mV),

 R_{CS} is a current detection resistor, and R_{OVP} is a overvoltage protection resistor.

When $I_{CSN} \times (R_{CS} + R_{OVP})$ is considered negligibly small compared with V_{CS} , I_{LED} can be calculated by the following equation.

$$I_{\text{LED}} = \frac{V_{\text{CS}}}{R_{\text{CS}}}$$
(3)

 R_{OVP} should be set so that I_{LED} is within the allowable accuracy range (see Section 9.5).



Figure 9-2 Control Circuit Diagram

9.2 LED Dimming

The IC supports analog dimming that inputs an analog signal (DC voltage) and digital dimming that inputs a PWM signal. Each dimming method is described below.

9.2.1 Analog Dimming

Figure 9-3 shows the DIM pin peripheral circuit when the analog dimming method is used. DIM pin voltage is determined by a resistor, R_{DIM} , connected to the DIM pin. Figure 9-4 shows the relationship between the DIM pin voltage and R_{DIM} . Figure 9-5 shows the relationship between the DIM pin voltage and the LED current, I_{LED} .

When the DIM pin voltage is 2 V or higher, the LED current becomes maximum, i.e., the LED dimming becomes to 100%. When a low-level signal (i.e., $< V_{\text{DIM(OFF)}}$ of 0.15 V) is input to the DIM pin from a

microcontroller port, the internal power MOSFET stops oscillating and the LED also turns off.



Figure 9-3 DIM Pin Peripheral Circuit



Figure 9-4 DIM Pin Voltage vs. R_{DIM}



Figure 9-5 LED Current vs. DIM Pin Voltage

9.2.2 Digital Dimming

The digital dimming of the IC inputs the PWM signal between the DIM and the GND pins, resulting in controlling the current flowing to the LED by the duty of the PWM signal. The DIM pin input signal including surge voltage should be within the DIM pin absolute maximum rating of -0.3 V to 3.3 V.

As shown in Figure 9-6, while the DIM pin is high level (i.e., $\geq V_{\text{DIM}(\text{ON})}$ of 0.2 V), the internal power MOSFET oscillates and current flows to the LED. While the DIM pin is low level (i.e., $\leq V_{\text{DIM}(\text{OFF})}$ of 0.15 V), the internal power MOSFET stops oscillating and the LED also turns off. When the duty cycle is 100%, the LED current becomes maximum, i.e., the LED dimming becomes to 100%.





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9.3 LED On/Off Function

When a low level signal (i.e., $< V_{DIM(OFF)}$ of 0.15 V) is input to the DIM pin from a microcontroller port, the internal power MOSFET stops oscillating and the LED turns off. To invert the logic, connect a transistor as shown in Figure 9-7.



Figure 9-7 DIM Pin Peripheral Circuit

9.4 Overcurrent Protection (OCP)

The IC has Overcurrent Protection (OCP) that limits the current flowing into the SW pin (see Figure 9-8). When the the current flowing into the SW pin increases to $I_{SW(LIM)} = 1.8$ A or more, the internal power MOSFET is turned off on a pulse-by-pulse basis. This protects the IC from an overcurrent flows due to a fault in constant current detection or an output short circuit.





9.5 Overvoltage Protection (OVP)

If the LED suddenly turns to be open from the normal operation state, the voltage between the CSP and CSN pins rises rapidly, which may result in critical damage to the IC. In order to protect the IC from overvoltage between the CSP and CSN pins, connect a resistor, R_{OVP}, and a Zener diode, DZ_{OVP}, as shown in Figure 9-9.

When the LED is open and the voltage between the CSP and CSN pins exceeds the value of the equation (4) due to the flowing of the current, I_{DZ} , as shown in Figure 9-10, the Overvoltage Protection (OVP) operates and the IC stops oscillating. When the voltage between the CSP

and CSN pins falls below the value of Equation (4), the OVP automatically restarts the normal operation.

$$V_{OUT(OVP)} = V_{Z(OVP)} + V_{CS(OVP)}$$
(4)

 $V_{OUT(OVP)}$ is the output voltage when LED is open $V_{Z(OVP)}$ is the Zener voltage of DZ_{OVP} $V_{CS(OVP)}$ is the OVP threshold voltage (150 mV)



Figure 9-10 LED Open

Set a resistor, $R_{\text{OVP}},$ and a Zener diode, $\text{DZ}_{\text{OVP}},$ as follows:

• Rovp

When the overvoltage protection operates, set the R_{OVP} resistance so that DZ_{OVP} is less than the allowable power dissipation and I_{LED} is within the allowable variation in your application.

When the power dissipation of DZ_{OVP} is P_{DZ} and the Zener voltage is V_{DZ} , the allowable current of the Zener diode, I_{DZ} , is in the range of the following equation.

$$I_{DZ} \le \frac{P_{DZ}}{V_{DZ}} \tag{5}$$

The value of R_{OVP} for keeping DZ_{OVP} below the allowable power dissipation is in the range of the following equation.

$$R_{OVP} \ge \frac{V_{CS(OVP)}}{I_{DZ} + I_{CSN}} - R_{CS}$$
(6)

Where:

 $V_{CS(OVP)}$ is the OVP threshold voltage (150 mV), I_{CSN} is the CSN pin input current, and R_{CS} is the LED current detection resistance.

In the equation (6), when $I_{CSN} \leq I_{DZ}$, the value of R_{OVP} is in the range of the following equation.

$$R_{OVP} \ge \frac{V_{CS(OVP)}}{I_{DZ}} - R_{CS}$$
(7)

Here is an example: when $V_{CS(OVP)} = 150 \text{ mV}$, $I_{CSN} = 9.5 \ \mu\text{A}$, $I_{DZ} = 5 \text{ mA}$, and $R_{CS} = 0.33 \ \Omega$, as $I_{CSN} << I_{DZ}$, $R_{OVP} = 29.67 \ \Omega \ (\approx 30 \ \Omega)$ from the equation (7).

• DZOVP

Set the Zener voltage, V_{DZ} , to be higher than the maximum voltage that is applied to the LED string so that DZ_{OVP} does not conduct in normal operation.

9.6 LED Incorrect Connection Protection



Figure 9-11 Correct Connection



Figure 9-12 Incorrect Connection

For applications using multiple LC5710S and driving multiple LED strings, care should be taken in connecting the LED strings.

If the LED string is connected between the outputs of different ICs as shown in Figure 9-12, the overcurrent protection, the thermal shutdown, or the LED incorrect connection protection is activated, resulting in IC unstable operation.

The LED incorrect connection protection is a function that protects the IC when the LED string is incorrectly connected. If the state where the voltage between CSP and CSN pins, $V_{CS} < 5$ mV and COMP pin voltage, V_{COMP} > 2.1 V continues for the watchdog timer setting time, $t_{WDT} = 30$ ms, or longer, the LED incorrect connection protection is activated and the IC operates in intermittent oscillation. This suppresses the heat generation of the IC, preventing critical damage to the IC.

This function is a simple protection in case of incorrect connection. In actual application, connect the LED strings correctly as shown in Figure 9-11.

9.7 Thermal Shutdown

When the junction temperature of the IC increases to the thermal shutdown operation temperature, $T_{SD} = 165$ °C, or more, the thermal shutdown (TSD) operates, and the IC stops the oscillation. TSD has the temperature hysteresis, $T_{SD_{.}HYS} = 22$ °C. When the junction temperature of the IC decreases to be $T_{SD} - T_{SD(HYS)}$ or lower, the TSD automatically restarts the normal operation.

9.8 Converter Type Selection

The converter type is determined by the input voltage, $V_{\rm IN}$, and the total forward voltage drop of the connected LEDs (see Table 9-1).

Table 9-1 Input Voltage, V_{IN} vs. LED String Voltage

Buck	$V_{IN} > (n \times V_{FLED}) + V_{CS}$
Boost	$V_{IN} \leq (n \times V_{FLED}) + V_{CS}$
Buck-	$V_{\text{pr}}(\min) \leq (n \times V_{\text{pr},\text{pr}}) + V_{\text{pr}} \leq V_{\text{pr}}(\max)$
boost	\mathbf{v}_{IN} (IIIIII.) \mathbf{v}_{FLED} + \mathbf{v}_{CS} \mathbf{v}_{IN} (IIIII.)
Where:	

 V_{FLED} is LED forward voltage drop (3.5 V for white LED for lighting),

n is the number of LEDs in series, and

 V_{CS} is the current detection threshold voltage (100 mV).

Table 9-2 shows the number of lights in series of LED depending on the circuit type. The unsupported (—) in Table 9-2 corresponds to one of the following conditions, therefore, the operation is limited.

- The input voltage is less than 5 V
- V_{IN(MAX)} or V_{SW(MAX)} is higher than 48 V (80% of absolute maximum rating, 60 V)
- Duty cycle, D, is outside the range of $0.15 \le D \le 0.84$
- Inductor peak current, I_{LP}, is 1.4 A or more (SW pin limit current, I_{SW (LIM)} = 1.4 A or more)

Table 9-2	Number of LEE	Os in Series
-----------	---------------	--------------

Conditions: V_{IN} (or V_{SW}) \leq 48 V (60 V × 0.8), 0.15 < D < 0.84

		V _{IN} Range (V)					
Number	V _{OUT} / LED	В	uck	В	oost	Buck	x-boost
in Series	Voltage (V)	$I_{LED} = 1.0 A,$	$\Delta I_L = 0.4 \text{ A}$	$I_{LED} = 0.5 A,$	$\Delta I_L = 0.4 \text{ A}$	$I_{LED} = 0.5 A,$	$\Delta I_L = 0.4 \text{ A}$
in Series	() onuge ()	Min.	Max.	Min.	Max.	Min.	Max.
1	3.6	5.00	24.00			5	20.4
2	7.1	8.45	47.33	5.00	6.04	5.1	39.9
3	10.6	12.62	48.00	5.00	9.01	7.6	37.4
4	14.1	16.79	48.00	6.60	11.99	10.1	33.9
5	17.6	20.95	48.00	8.30	14.96	12.7	30.4
6	21.1	25.12	48.00	9.90	17.94	15.1	26.9
7	24.6	29.29	48.00	11.60	20.91	17.6	23.4
8	28.1	33.45	48.00	13.20	23.89		
9	31.6	37.62	48.00	14.90	26.86		
10	35.1	41.79	48.00	16.50	29.84	_	
11	38.6	45.95	48.00	18.20	32.81		
12	42.1			19.80	35.79		
13	45.6	_		21.50	38.76	_	

- : unsupported

The graphs based on Table 9-2 are shown in Figure 9-13 to Figure 9-15. The values in the graphs are reference. In actual operation, when a large surge occurs on the SW pin or the IC is operating at high temperature, reduce the number of LEDs or the LED current, I_{LED} . Use the IC within the range of the thermal derating curve in Figure 10-1.



Figure 9-13 Number of LEDs in Series vs. Input Voltage Range (Buck)



Figure 9-14 Number of LEDs in Series vs. Input Voltage Range (Boost)



Figure 9-15 Number of LEDs in Series vs. Input Voltage Range (Buck-boost)

9.9 External Inductor Setting

The definitions of the symbols used in this section are as follows:

 V_{OUT} is output voltage, I_L is inductor current, ΔI_L is inductor ripple current, I_{LED} is LED current, and f_{OSC} is oscillation frequency.

When using the IC, set the inductance value so that the inductance current is in the continuous current mode (CCM: Continuous Conduction Mode).

The IC supports buck converter, boost converter, and buck-boost converter. Table 9-3 shows the equation of the inductance in each circuit type.

Duty cycle, D, is set within the range of the following equation.

$$t_{ON(MIN)} \times f_{OSC} < D < D_{MAX}$$
(8)

$$0.15 < D < 0.84$$
 (9)

V_{OUT} is calculated by the following equation.

$$V_{OUT} = n \times V_{FLED} + V_{CS}$$
(10)

Where:

 V_{FLED} is LED forward voltage drop (about 3.5 V for white LED for lighting),

n is the number of LEDs in series, and

V_{CS} is current detection threshold voltage (100 mV).

Parameter	Buck	Boost	Buck-boost
SW Pin Voltage, V _{SW}	V _{IN}	V _{OUT}	$V_{IN} + V_{OUT}$
Duty Cycle, D	$\frac{V_{OUT}}{V_{IN}}$	$\frac{V_{OUT}-V_{IN}}{V_{OUT}}$	$\frac{V_{OUT}}{V_{IN} + V_{OUT}}$
Inductor Average Current, $I_{L(AVG)}$	I _{LED}	$\frac{I_{LED}}{1-D}$	$\frac{I_{LED}}{1-D}$
Inductor Peak Current, ILP	$I_{LED} + \frac{\Delta I_L}{2}$	$\frac{I_{LED}}{1-D} + \frac{\Delta I_L}{2}$	$\frac{I_{LED}}{1-D} + \frac{\Delta I_L}{2}$
Inductance, L	$\frac{V_{OUT} \times (1 - D)}{\Delta I_L \times f_{OSC}}$	$\frac{V_{IN} \times D}{\Delta I_L \times f_{OSC}}$	$\frac{V_{IN} \times D}{\Delta I_L \times f_{OSC}}$

 Table 9-3
 Inductance Calculation

In the buck converter, the drain current, I_D , flowing through the SW pin is equal to I_{LED} . In the boost and buckboost converters, when D = 0.5 and the inductor ripple current, ΔI_L , is the same, I_D twice that of the buck converter flows to the SW pin.

The maximum ΔI_L is 0.4 A. Set the inductor peak current, I_{LP} , to less than 1.4 A (lower limit of $I_{SW (LIM)}$) so that the overcurrent protection does not operate.

Therefore, the maximum current that can be supplied to the LED is as follows.

- Buck: 1.0 A
- Boost and Buck-boost: 0.5 A

Note that the IC should be used within the thermal derating curve in Figure 10-1.

Figure 9-16 to Figure 9-18 show graphs of inductance L and ripple current, ΔI_L . The inductance L and ripple current, ΔI_L are calculated under the condition that V_F of the white LED for lighting is 3.5 V and 5 lights ($V_{OUT} = 17.6$ V) are connected in series.



Figure 9-16 Buck Converter Inductance Calculation Example ($V_{OUT} = 17.6 \text{ V}, V_{IN} = 24 \text{ V}$)



Figure 9-17 Boost Converter Inductance Calculation Example $(V_{OUT} = 17.6 \text{ V}, V_{IN} = 12 \text{ V})$



Figure 9-18 Buck-boost Converter Inductance Calculation Example $(V_{OUT} = 17.6 \text{ V}, V_{IN} = V_{OUT} \pm 20\%)$

When ΔI_L is decreased, the required inductance, L, is increased. Compared with inductors with the same physical dimensions, inductors with a larger L value tend to have a smaller allowable current, I_{DZ} . When the L value is large and the allowable current I_{DZ} is also large, an inductor with a large physical dimension is required.

In general, the value of ΔI_L is set to about 20% to 30% of the output current.

$$\Delta I_{\rm L} = I_{\rm OUT} \times 0.2 \text{ to } 0.3 \tag{11}$$

9.10 Calculation of Power Dissipation, PD

Power dissipation, P_D , is calculated by the following equation.

$$P_{\rm D} = P_{\rm COUT} + P_{\rm SW} + P_{\rm ON} \tag{12}$$

Where:

P_{CONT} is internal control circuit loss,

 P_{SW} is switching loss of internal power MOSFET, and P_{ON} is on-resistance loss of internal power MOSFET.

The calculation for each loss is as follows.

9.10.1 Control Circuit Loss, PCONT

The control circuit loss, P_{CONT} , depends on the input voltage and the frequency. P_{CONT} includes the loss of circuit current inside the IC and the drive loss of the power MOSFET inside the IC. The value of P_{CONT} is read from Figure 9-19.



Figure 9-19 Control Circuit Loss, P_{CONT}

9.10.2 Switching Time of Power MOSFET

Figure 9-20 shows the switching time, t_{SW} , of the internal power MOSFET. t_{SW} is defined, provided that the turn-on time, t_r , and the turn-off time, t_f , are the same value. Figure 9-20 shows the relationship between the SW pin voltage and t_{SW} , assuming that there is almost no effect of parasitic inductance on the main circuit.





The internal power MOSFET is connected to the main circuit of the voltage converter. When the impedance of the main circuit pattern that the switching current flows through is high or the parasitic inductance is included, the switching time may be different from that of Figure 9-20.

9.10.3 Switching Loss, Psw of Power MOSFET

Switching loss, P_{SW} , in the power MOSFET can be calculated by the following equation.

• Buck

$$P_{SW} = 2 \times (V_{IN} \times \frac{I_{LED}}{2} \times t_{SW} \times f_{OSC})$$
(13)

• Boost

$$P_{SW} = 2 \times (V_{OUT} \times \frac{I_{L(AVG)}}{2} \times t_{SW}$$

$$\times f_{OSC})$$
(14)

• Buck-boost

$$P_{SW} = 2 \times \left\{ (V_{IN} + V_{OUT}) \times \frac{I_{L(AVG)}}{2} \\ \times t_{SW} \times f_{OSC} \right\}$$
(15)

Where:

 V_{IN} is input voltage (V), V_{OUT} is output voltage (V), I_{LED} is LED current (A), $I_{L(AVG)}$ is inductor average current (A), t_{SW} is switching time of power MOSFET (s), and f_{OSC} is switching frequency (Hz).

tsw is the value read from Figure 9-20 or measured.

9.10.4 On-resistance Loss, Pon, of Power MOSFET

On-resistance loss, P_{ON} , of power MOSFET is calculated by the following equation.

• Buck

$$P_{\rm ON} = R_{\rm ON} \times I_{\rm LED}^2 \times t_{\rm ON} \times f_{\rm OSC}$$
(16)

Boost and Buck-boost

$$P_{ON} = R_{ON} \times I_{L(AVG)}^{2} \times t_{ON} \times f_{OSC}$$
(17)

Where: R_{ON} is on-resistance of power MOSFET (Ω), I_{LED} is LED current (A), $I_{L(AVG)}$ is inductor average current (A), and t_{ON} is on-time of power MOSFET (s).

$$t_{ON} = \frac{1}{f_{OSC}} \times D$$

D is duty cycle (see Table 9-3). f_{OSC} is switching frequency (Hz).

(14) (15) (15)

10. Design Notes

10.1 Thermal Derating Curve

Figure 10-1 shows the IC derating curve when mounting on the board described in Section 11. When using the IC, ensure enough margins. Thermal derating is calculated at $T_J = 125 \circ C$, $\theta_{J-A} = 82.8 \circ C/W$.



Figure 10-1 Thermal Derating Curve

Allowable power dissipation, P_D , is calculated by the following equation.

$$P_{\rm D} = \frac{\left(T_{\rm J} - T_{\rm A}\right)}{\theta_{\rm I-A}}$$

Where:

T_J is junction temperature (125 °C),

T_A is ambient temperature, and

 θ_{J-A} is junction-to-ambient thermal resistance (82.8 °C/W).

When
$$T_A = 25 \,^{\circ}C$$
, P_D is 1.2077 W

10.2 External Components

Components fit for the use condition should be used.

10.2.1 Inductor (L1)

Inductor (L1) is a choke coil for LED current smoothing.

The larger the inductance is, the smaller the ripple current, ΔI_L , is. The smaller the inductance is, the larger the ripple curren, ΔI_L , is. Reducing ΔI_L reduces LED heat generation due to changes in ΔI_L .

The inductance must be set to prevent the inductor from being magnetically saturated even during overload or short-circuit load condition.

10.2.2 Diode (Ds)

Select a Schottky diode or ultra-fast recovery diode for a freewheeling or boosting diode.

When a diode with a long reverse recovery time, $t_{\rm rr}$, is selected, a large surge current flows through the power MOSFET in turn-on of the power MOSFET, which causes increased noise, malfunction, and decreased efficiency.

10.2.3 Current Detection Resistor (R_{CS})

A high frequency switching current flows through R_{CS} ; therefore, malfunctions may be caused if a resistor with a high internal inductance is used. The resistor with low internal inductance and high surge capability must be selected.

10.2.4 Input Capacitor (CIN)

Input capacitor, C_{IN} , is a capacitor for smoothing the main supply circuit. The larger the capacitance of C_{IN} is, the smaller the ripple voltage is. The larger the output power is, the larger the ripple voltage is. Select C_{IN} according to the output power.

10.2.5 Output Capacitor (COUT)

According to the ripple current, ΔI_L , allowed by the LED string, determine whether C_{OUT} is necessary, and if necessary, determine the capacitance of C_{OUT} .

When the allowable range of ΔI_L is large, reduce the capacitance of C_{OUT} or remove C_{OUT} .

When the allowable range of ΔI_L is small, connect C_{OUT} in parallel with the LED string.

When the LED string is far from the output pin, connect C_{OUT} in parallel with the LED string to reduce ΔI_L and ripple voltage.

10.2.6 Phase Compensation Circuit (Rs, Cs, C_P)

 R_S , C_S , and C_P are components for phase compensation connected to the COMP pin. In order to prevent malfunction due to noise, these components should be connected between the COMP and GND pins with a minimal length of traces.

10.2.7 Frequency Setting Resistor (RRT)

Set the oscillation frequency (100 kHz to 500 kHz) with R_{RT} . To avoid malfunctions, be sure to connect R_{RT} between the RT and GND pins with a minimal length of traces.

10.3 Phase Compensation (COMP Pin)

To operate the IC stably, ensure enough phase margins. The phase margin is determined by the resistor and the capacitors connected to the COMP pin (i.e., R_S , C_S , and C_P).



Figure 10-2 COMP Pin Peripheral Circuit

1) Setting of Target Crossover Frequency, fc

A crossover frequency, f_c , is the frequency when the gain becomes 0 dB (1 time). The higher f_c , the faster the response to load fluctuation, but the operation tends to become unstable due to the influences of ripple and noise. In order to operate the IC stably, set the frequency so that f_c is within the range of the followiong equation.

• Buck

$$f_C \le \frac{f_{OSC}}{50}$$

Where:

f_{OSC} is switching frequency (Hz).

Boost

$$f_{\rm C} \le \frac{f_{\rm Z2}}{50} \tag{20}$$

$$f_{Z2} = \frac{R_{LED} \times (1 - D)^2}{2\pi \times L}$$
(21)

$$R_{LED} = \frac{V_{OUT}}{I_{LED}}$$
(22)

Where:

f_{Z2} is zero frequency (Hz),

 R_{LED} is the resitance when the LED is regarded as a resistive load (Ω), L is inductance (H), D is duty cycle,

 V_{OUT} is output voltage (V), and I_{LED} is LED current (A).

• Buck-boost

When $D \ge 0.5$, f_C is calculated by the equation of boost. When D < 0.5, f_C is calculated by the equation of buck.

If the operation is unstable, set a lower value of f_{C} .

2) Setting of Rs

 R_s is a resistor for phase compensation, which is calculated by the following equation.

$$R_{\rm S} = \frac{2\pi \times C_{\rm OUT} \times f_{\rm C} \times V_{\rm OUT}}{K}$$
(23)

Where:

 C_{OUT} is the output capacitance (F), f_C is the crossover frequency set above (Hz), V_{OUT} is output voltage (V), and K is the constant of the IC (2.497 \times 10⁻⁴).

In buck converter, when $f_C = 10$ kHz, $C_{OUT} = 1 \mu F$, and $V_{OUT} = 3.6$ V, R_S is as follows:

$$R_{S} = \frac{2\pi \times 1 \,\mu\text{F} \times 10 \,\text{kHz} \times 3.6 \,\text{V}}{2.497 \,\times \,10^{-4}} \approx 0.91 \,\text{k}\Omega$$

3) Setting of Cs

 C_S

 C_S is a capacitor for phase compensation. A pole frequency, f_{P1} , and zero frequency, f_{Z1} , are determined by C_S . To ensure enough phase margin (60 deg. or more), f_{Z1} should be set to about a quarter of f_C .

 C_S is calculated by the following equation.

$$=\frac{4}{2\pi \times R_{\rm S} \times f_{\rm C}}$$
(24)

In buck converter, when $f_C = 10$ kHz and $R_S = 0.91$ k Ω , C_S is as follows:

$$C_{\rm S} = \frac{4}{2\pi \times 0.91 \text{ k}\Omega \times 10 \text{ kHz}} \approx 70.3 \text{ nF}$$

4) Setting of C_P

No C_P is required when a ceramic capacitor is used for an output capacitor.

When an aluminum electrolytic capacitor is used for the output capacitor, if ESR is in the range of Equation (25), C_P must be added to offset the effect of zero frequency, f_{Z2} , generated by ESR. In the control using the peak current control method, f_{Z2} makes f_C higher than necessary, which may cause malfunction of the IC. Therefore, to offset the influence of f_{Z2} , add C_P to configure a new pole frequency, f_{P3} .

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$$ESR > \frac{1}{2\pi \times f_{C} \times C_{OUT}}$$
(25)

 C_P is calculated by the following equation.

$$C_{\rm P} = \frac{C_{\rm OUT} \times ESR}{R_{\rm S}}$$
(26)

10.4 PCB Layout

The switching power supply circuit includes high frequency and high voltage current paths that affect the IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing. Thus, to reduce the impedance of the high frequency traces on a PCB (see Figure 10-3), they should be designed as wide trace and small loop as possible.

Care should be taken in thermal design because the power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$.



Figure 10-3 High-frequency Current Loops (Hatched Area)

Figure 10-4 to Figure 10-6 are peripheral circuit examples of the IC.

1) Main Circuit Trace Layout

The switching current flows through these main circuti traces. Therefore, these traces should be as wide and short as possible.

- 2) Logic Ground Trace Layout If a large current flows through a logic ground, electric potential across the logic ground may vary and thus cause the IC to malfunction. Logic ground traces should be designed as close as possible to the GND pin, at a single-point ground (or star ground) that is separated from the main circuit. Therefore, it is recommended to separate the dimming signal ground traces from the main circuit trace.
- 3) R_{CS} Trace Layout

In order to reduce noise at current detection, R_{OVP} must be separated, and be connected between the CSP and CSN pins with a minimal length of traces. When the noise between the CSP and CSN pins is large, connect a filter capacitor, C_f (see Section 6).

- COMP Pin Peripheral Circuit The phase compensation circuit components (Rs, Cs, Cp) should be connected between the COMP and GND pins with a minimal length of traces.
- 5) RT Pin Peripheral Circuit

Frequency setting resistor, R_{RT} , should be connected between the RT and GND pins with a minimal length of traces.

6) C_{OUT} is placed close to the LED string.







Figure 10-5 Peripheral Circuit Example around the IC: Boost



Figure 10-6 Peripheral Circuit Example around the IC: Buck-boost

11. Pattern Layout Example

This section contains the schematic diagrams of a PCB pattern layout example using the LC5710S. Note that the pattern layout example only uses the parts illustrated in the circuit diagram below. For details on the land pattern example of the IC, see Section 7.



Figure 11-1 Pattern Layout Example for Buck Converter



Figure 11-2 Pattern Layout Example for Boost and Buck-boost Converters







In boost converter, J2 is open and J1 is inserted. In buck-boost converter, J1 is open and J2 is inserted.

Figure 11 Pattern Layout Example for Boost and Buck-boost Converters

12. Typical Characteristics











Figure 12-7 Efficiency (Buck-boost)

Figure 12-8 Efficiency (Buck-boost)



Figure 12-9 Undervoltage Lockout (Boost)





Figure 12-11 PWM Digital Dimming Characteristics (Dimming Fequency = 1 kHz)

Figure 12-12 Analog Dimming Characteristics





Figure 12-18 Waveforms at Digital Dimming (1 kHz, duty cycle 5%)





 $\begin{array}{l} \mbox{Figure 12-20} & \mbox{Normal Oscillation Waveforms} \\ \mbox{(Buck, } V_{IN} = 30 \mbox{ V}, \mbox{ 5LEDs}, \mbox{ } f_{OSC} = 100 \mbox{ kHz}) \end{array}$

 $Figure 12-21 \quad Normal Oscillation Waveforms \\ (Buck, V_{IN} = 30 \ V, \ 5LEDs, \ f_{OSC} = 500 \ kHz)$



Figure 12-22 Normal Oscillation Waveforms (Boost, V_{IN} = 15 V, 5LEDs, f_{OSC} = 100 kHz)





Figure 12-24 Normal Oscillation Waveforms (Buck-boost, $V_{IN} = 20$ V, 5LEDs, $f_{OSC} = 100$ kHz)

AotRecc

Figure 12-25 Normal Oscillation Waveforms (Buck-boost, V_{IN} = 20 V, 5LEDs, f_{OSC} = 500 kHz)

Vsw

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