19-1335; Rev 0a; 2/98

EVALUATION KIT AVAILABLE

Low-Power, 90Msps, 6-Bit ADC

MAX1011

General Description

The MAX1011 is a 6-bit analog-to-digital converter (ADC) that combines high-speed, low-power operation with a user-selectable input range, an internal reference, and a clock oscillator. The ADC converts analog signals into binary-coded digital outputs at sampling rates up to 90Msps. The ability to directly interface with baseband signals makes the MAX1011 ideal for use in a wide range of communications and instrumentation applications.

The MAX1011's input amplifier features a true differential input, a -0.5dB analog bandwidth of 55MHz, and a user-programmable input full-scale range of 125mVp-p, 250mVp-p, or 500mVp-p. With an AC-coupled signal, input offset is typically less than 1/4LSB. Dynamic performance is 5.85 effective number of bits (ENOB) with a 20MHz analog input signal, or 5.7 ENOB with a 50MHz signal.

The MAX1011 operates with +5V analog and +3.3V digital supplies for easy interfacing to +3.3V-logic-compatible digital signal processors and microprocessors. It comes in a 24-pin QSOP package.

Features

- **High Sampling Rate: 90Msps**
- **Low Power Dissipation: 215mW**
- **Excellent Dynamic Performance:**
  5.85 ENOB with 20MHz Analog Input
  5.7 ENOB with 50MHz Analog Input
- **±1/4LSB INL and DNL (typ)**
- **±1/4LSB Input Offset (typ)**
- **Internal Bandgap Voltage Reference**
- **Internal Oscillator with Overdrive Capability**
- **55MHz (-0.5dB) Bandwidth Input Amplifier with True Differential Input**
- **User-Selectable Full-Scale Range (125mVp-p, 250mVp-p, or 500mVp-p)**
- **Single-Ended or Differential Input Drive**
- **Flexible, 3.3V, CMOS-Compatible Digital Outputs**

Applications

IF Sampling Receivers

VSAT Receivers

Wide Local Area Networks (WLANs)

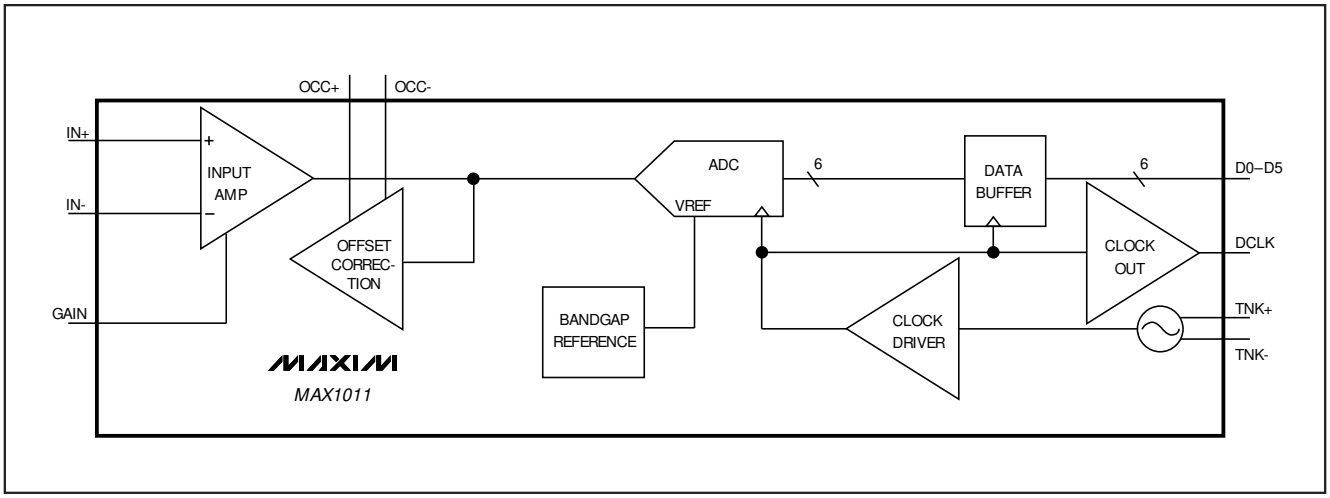
Instrumentation

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1011CEG	0°C to +70°C	24 QSOP

Pin Configuration appears at end of data sheet.

Functional Diagram



Low-Power, 90Msps, 6-Bit ADC

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6.5V
V_{CCO} to OGND.....-0.3V to +6.5V
GND to OGND .....-0.3V to +0.3V
Digital and Clock Output Pins to OGND...-0.3V to V_{CCO} (10sec)
All Other Pins to GND.....-0.3V to V_{CC}

Continuous Power Dissipation (T_A = +70°C)
24-Pin QSOP (derate 10mW/°C above +70°C).....800mW
Operating Temperature Range.....0°C to +70°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, <10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±5%, V_{CCO} = 3.3V ±300mV, **T_A = T_{MIN} to T_{MAX}**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution	RES		6			Bits
Integral Nonlinearity	INL		-0.5	±0.25	0.5	LSB
Differential Nonlinearity	DNL	No missing codes over temperature	-0.5	±0.25	0.5	LSB
Full-Scale Input Range	V_{FSH}	GAIN = V_{CC} (high gain)	118.75	125	131.25	mVp-p
	V_{FSM}	GAIN = open (mid gain)	237.5	250	262.5	
	V_{FSL}	GAIN = GND (low gain)	475	500	525	
INVERTING AND NONINVERTING ANALOG INPUTS						
Input Open-Circuit Voltage	V_{AOC}		2.25	2.35	2.45	V
Input Resistance	R_{IN}		13	20	29	kΩ
Input Capacitance	C_{IN}	Guaranteed by design		1.5	3	pF
Common-Mode Voltage Range	V_{CM}	Other analog input driven with external source (Note 2)	1.75		2.75	V
OSCILLATOR INPUTS						
Oscillator Input Resistance	R_{OSC}	Other oscillator input tied to V_{CC} + 0.3V	4.8	8	12.1	kΩ
DIGITAL OUTPUTS (D0–D5)						
Digital Outputs Logic-High Voltage	V_{OH}	I_{SOURCE} = 50µA	0.7V_{CCO}			V
Digital Outputs Logic-Low Voltage	V_{OL}	I_{SINK} = 400µA			0.5	V
POWER SUPPLY						
Supply Current	I_{CC}			37	63.5	mA
Power-Supply Rejection Ratio	PSRR	V_{CC} = 4.75V to 5.25V (Note 3)		-65	-40	dB
Digital Outputs Supply Current	I_{CCO}	20MHz, full-scale analog inputs, C_L = 15pF (Note 4)		8.5	13.8	mA
Power Dissipation	PD			215		mW

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±5%, V_{CCO} = 3.3V ±300mV, **T_A = +25°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (Gain = open, external 90MHz clock (Figure 7), V_{IN} = 20MHz sine, amplitude -1dB below full scale, unless otherwise noted.)						
Maximum Sample Rate	f_{MAX}		90			Msps
Analog Input -0.5dB Bandwidth	BW	GAIN = GND, open, V_{CC}		55		MHz
Effective Number of Bits	$ENOB_M$	GAIN = open (mid gain)	5.6	5.85		Bits
		GAIN = open (mid gain), f_{IN} = 50MHz, -1dB below full scale		5.7		
	$ENOB_H$	GAIN = V_{CC} (high gain)		5.8		
	$ENOB_L$	GAIN = GND (low gain)		5.85		
Signal-to-Noise Plus Distortion Ratio	SINAD	GAIN = open (mid gain)	35.5	37		dB
Input Offset (Note 5)	OFF	Guaranteed by design	-0.5		0.5	LSB
TIMING CHARACTERISTICS (Data outputs: R_L = 1MΩ, C_L = 15pF)						
Clock to Data Propagation Delay	t_{PD}	(Note 6)		3.0		ns
Data Valid Skew	t_{SKEW}	(Note 6)		1		ns
Input to DCLK Delay	t_{DCLK}	TNK+ to DCLK (Note 6)		4.5		ns
Aperture Delay	t_{AD}	Figure 8		5.5		ns
Pipeline Delay	PD	Figure 8		1		clock cycle

Note 1: Best-fit straight-line linearity method.

Note 2: A typical application will AC couple the analog input to the DC bias level present at the analog inputs (typically 2.35V). However, it is also possible to DC couple the analog input (using differential or single-ended drive) within this common-mode input range (Figures 4 and 5).

Note 3: PSRR is defined as the change in the mid-gain, full-scale range as a function of the variation in V_{CC} supply voltage, expressed in decibels.

Note 4: The current in the V_{CCO} supply is a strong function of the capacitive loading on the digital outputs. To minimize supply transients and achieve optimal dynamic performance, reduce the capacitive-loading effects by keeping line lengths on the digital outputs to a minimum.

Note 5: Offset-correction compensation enabled, 0.22µF at compensation inputs (Figures 2 and 3).

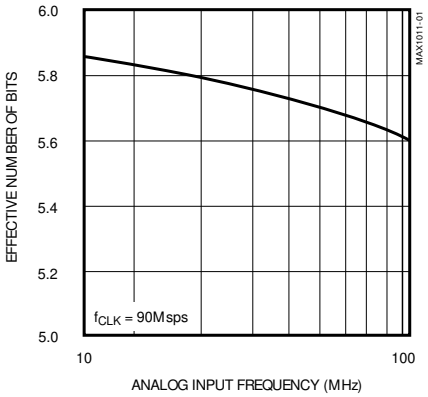
Note 6: t_{PD} and t_{SKEW} are measured from the 1.4V level of the output clock, to the 1.4V level of either the rising or falling edge of a data bit. t_{DCLK} is measured from the 50% level of the clock-overdrive signal on TNK+ to the 1.4V level of DCLK. The capacitive load on the outputs is 15pF.

Low-Power, 90Msps, 6-Bit ADC

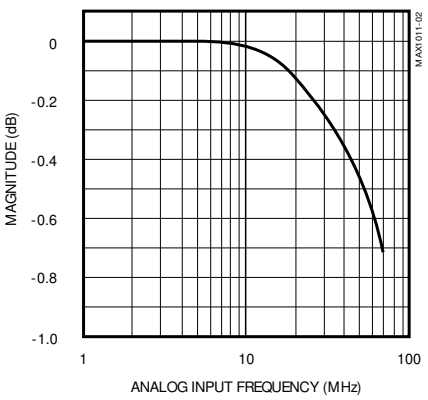
Typical Operating Characteristics

(V_{CC} = +5V ±5%, V_{CCO} = 3.3V ±300mV, f_{CLK} = 90Msps, GAIN = open (midgain) MAX1011 evaluation kit, T_A = +25°C, unless otherwise noted.)

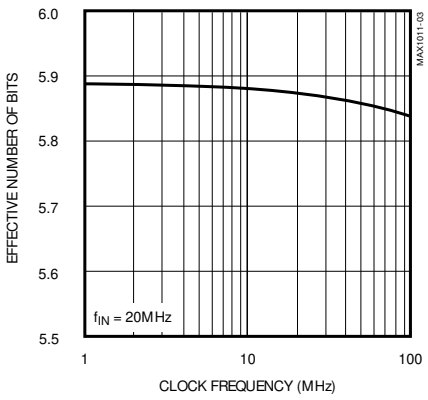
EFFECTIVE NUMBER OF BITS vs. ANALOG INPUT FREQUENCY



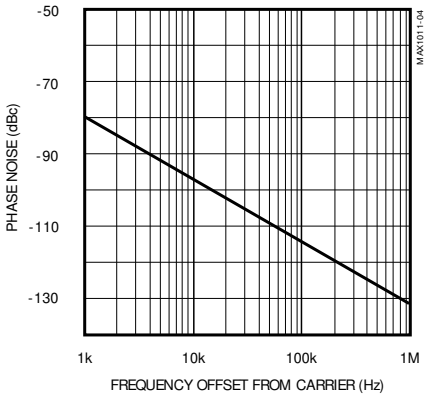
ANALOG INPUT BANDWIDTH



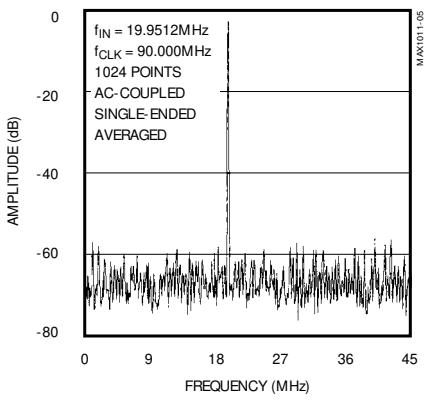
EFFECTIVE NUMBER OF BITS vs. SAMPLING/CLOCK FREQUENCY



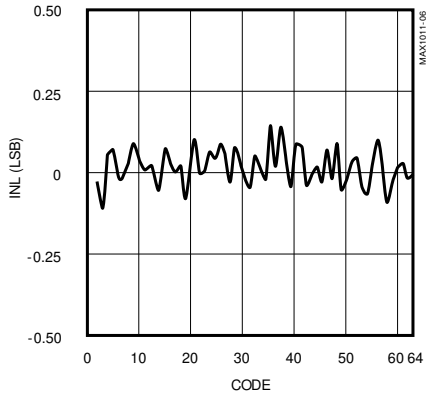
OSCILLATOR OPEN-LOOP PHASE NOISE vs. FREQUENCY OFFSET



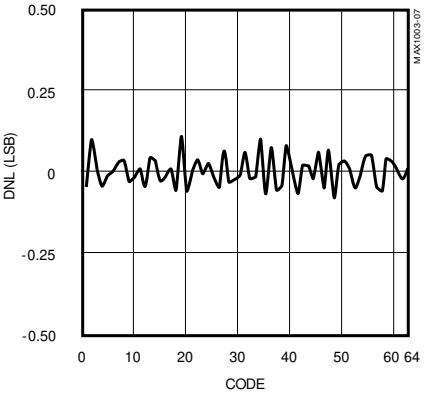
FFT PLOT



INTEGRAL NONLINEARITY vs. CODE



DIFFERENTIAL NONLINEARITY vs. CODE



Pin Description

PIN	NAME	FUNCTION
1	GAIN	Gain-Select Input. Sets input full-scale range: 125/250/500mVp-p (Table 1).
2	OCC+	Positive Offset-Correction Compensation. Connect a 0.22µF capacitor for AC-coupled inputs. Ground pin 2 for DC-coupled inputs.
3	OCC-	Negative Offset-Correction Compensation. Connect a 0.22µF capacitor for AC-coupled inputs. Ground pin 3 for DC-coupled inputs.
4	IN+	Noninverting Analog Input
5	IN-	Inverting Analog Input
6	V_{CC}	+5V ±5% Supply. Bypass with a 0.01µF capacitor to GND (pin 9).
7	TNK+	Positive Oscillator/Clock Input
8	TNK-	Negative Oscillator/Clock Input
9, 10, 12, 13	GND	Analog Ground
11	V_{CC}	+5V ±5% Supply. Bypass with a 0.01µF capacitor to GND (pin 10).
14	V_{CC}	+5V ±5% Supply. Bypass with a 0.01µF capacitor to GND (pin 13).
15	N.C.	No Connection
16	OGND	Digital Output Ground
17	V_{CCO}	Digital Output Supply, +3.3V ±300mV. Bypass with a 47pF capacitor to OGND (pin 16).
18	DCLK	Digital Clock Output. Frames the output data.
19–24	D0–D5	Digital Outputs 0–5. D5 is the most significant bit (MSB).

Detailed Description

Converter Operation

The MAX1011 integrates a 6-bit analog-to-digital converter (ADC), a buffered voltage reference, and oscillator circuitry. The ADC uses a flash conversion technique to convert an analog input signal into a 6-bit parallel digital output code. The MAX1011's unique design includes 63 fully differential comparators and a proprietary encoding scheme that ensures no more than 1LSB dynamic encoding error. The control logic interfaces easily to most digital signal processors (DSPs) and microprocessors (µPs) with +3.3V CMOS-compatible logic interfaces. Figure 1 shows the MAX1011 in a typical application.

Programmable Input Amplifier

The MAX1011 has a programmable-gain input amplifier with a -0.5dB bandwidth of 55MHz and a true differential input. To maximize performance in high-speed systems, the amplifier has less than 3pF of input capacitance. The input amplifier gain is programmed via the GAIN pin to provide three possible input full-scale ranges (FSRs) as shown in Table 1.

Single-ended and differential AC-coupled input circuit examples are shown in Figures 2 and 3. Each of the

Table 1. Input Amplifier Programming

GAIN	INPUT FULL-SCALE RANGE (mVp-p)
GND	500
Open	250
V_{CC}	125

amplifier inputs is internally biased to a 2.35V reference through a 20kΩ resistor, eliminating external DC bias circuits. A series 0.1µF capacitor is required at the amplifier input for AC-coupled signals.

When operating with AC-coupled inputs, the input amplifier's DC offset voltage is nulled to within ±1/2LSB by an on-chip, offset-correction amplifier. An external compensation capacitor is required to set the dominant pole of the offset-correction amplifier's frequency response (Figures 2 and 3). The compensation capacitor will determine the low-frequency corner of the analog input response according to the following formula:

$$f_C = 1 / (0.1 \times C)$$

where C is the value of the compensation capacitor in µF, and f_C is the corner frequency in Hz.

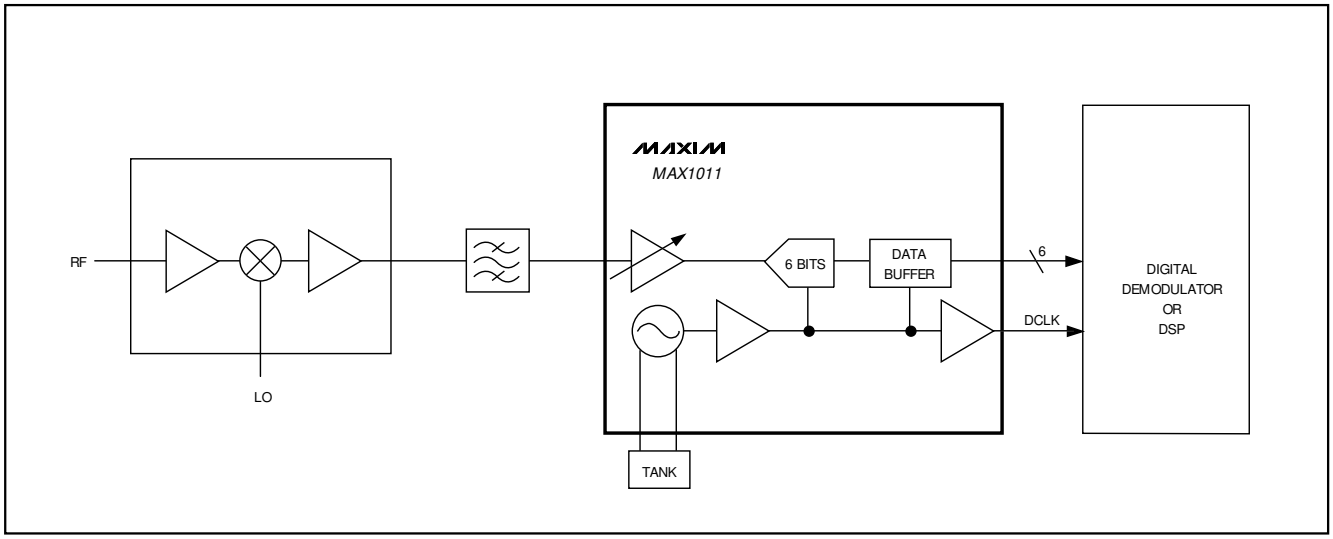


Figure 1. IF Sampling Receiver

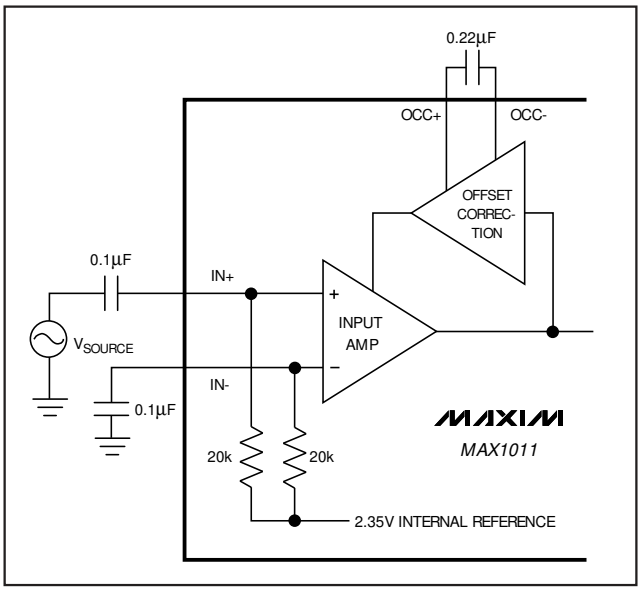


Figure 2. Single-Ended AC-Coupled Input

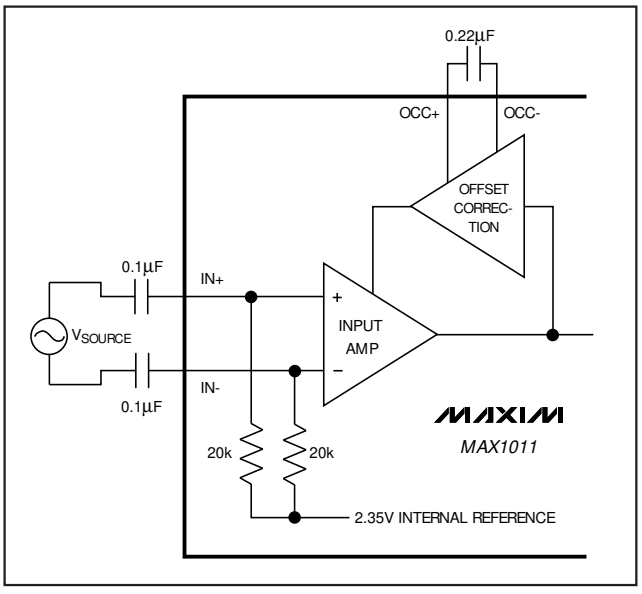


Figure 3. Differential AC-Coupled Input

For applications where a DC component of the input signal is present, Figures 4 and 5 show single-ended and differential DC-coupled input circuits. The amplifier's input common-mode voltage range extends from 1.75V to 2.75V. To prevent attenuation of the input signal's DC component in this mode, disable the offset-correction amplifier by grounding the OCC+ and OCC- pins (Figures 4 and 5).

ADC

The ADC block receives the analog signal from the input amplifier. The ADC uses flash conversion with 63 fully differential comparators to digitize the analog input signal into a 6-bit output in offset binary format.

The MAX1011 features a proprietary encoding scheme that ensures no more than 1LSB dynamic encoding error. Dynamic encoding errors resulting from metastable states may occur when the analog input voltage, at the time the sample is taken, falls close to the decision point for any one of the input comparators. The resulting output code for typical converters can be incorrect, including false full- or zero-scale outputs. The MAX1011's unique design reduces the magnitude of this type of error to 1LSB.

Internal Voltage Reference

An internal buffered-bandgap reference is included on the MAX1011 to drive the ADC's reference ladder. The on-chip reference and buffer eliminate any external (high-impedance) connections to the reference ladder, minimizing the potential for noise coupling from external circuitry while ensuring that the voltage reference, input amplifier, and reference ladder track well with variations of temperature and power supplies.

Oscillator Circuit

The MAX1011 includes a differential oscillator, which is controlled by an external parallel resonant (tank) network as shown in Figure 6. Alternatively, the oscillator may be overdriven with an external clock source as shown in Figure 7.

Internal Clock Operation (Tank)

If the tank circuit is used, the resonant inductor should have a sufficiently high Q and a self-resonant frequency (SRF) of at least twice the intended oscillator frequency. Coilcraft's 1008HS-221, with an SRF of 700MHz and a Q of 45, works well for this application. Generate different clock frequency ranges by adjusting varactor and tank elements.

An internal clock-driver buffer is included to provide sharp clock edges to the internal flash comparators. The buffer ensures that the comparators are simultaneously clocked, maximizing the ADC's effective number of bits (ENOB) performance.

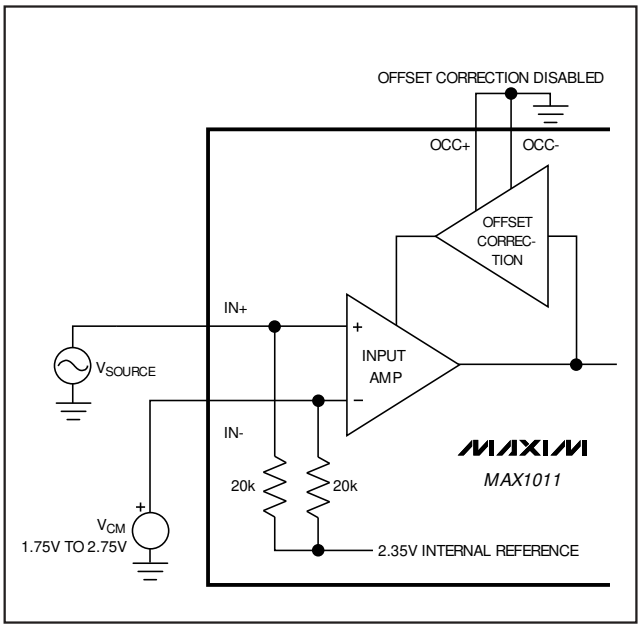


Figure 4. Single-Ended DC-Coupled Input

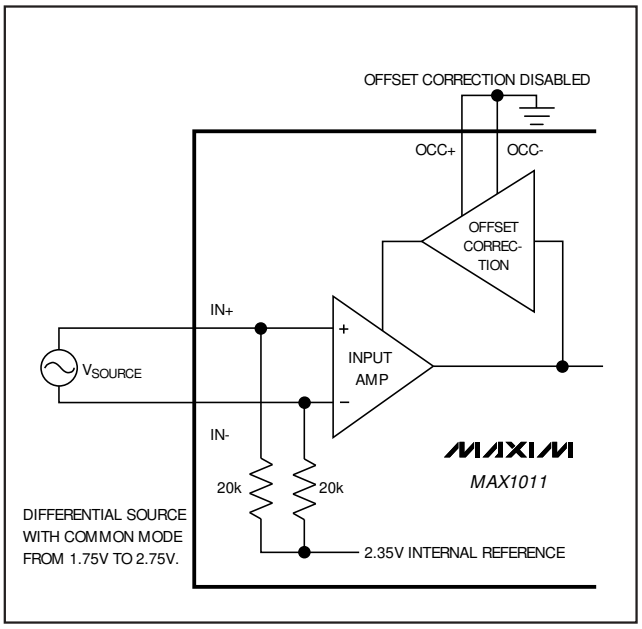


Figure 5. Differential DC-Coupled Input

Low-Power, 90Msps, 6-Bit ADC

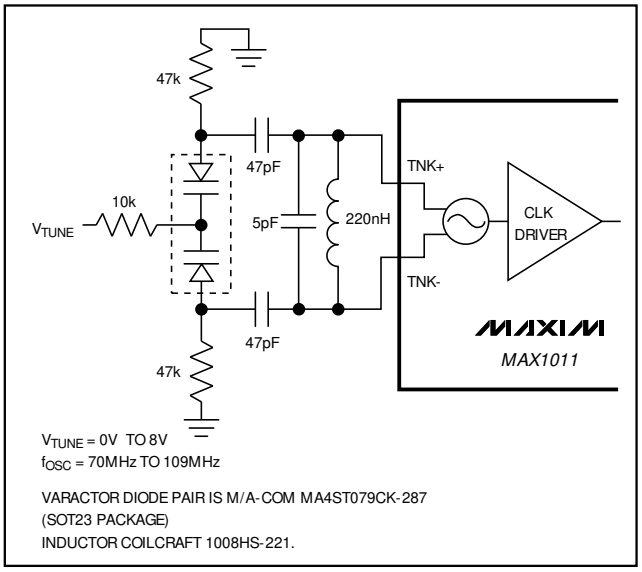


Figure 6. Tank Resonator Oscillator

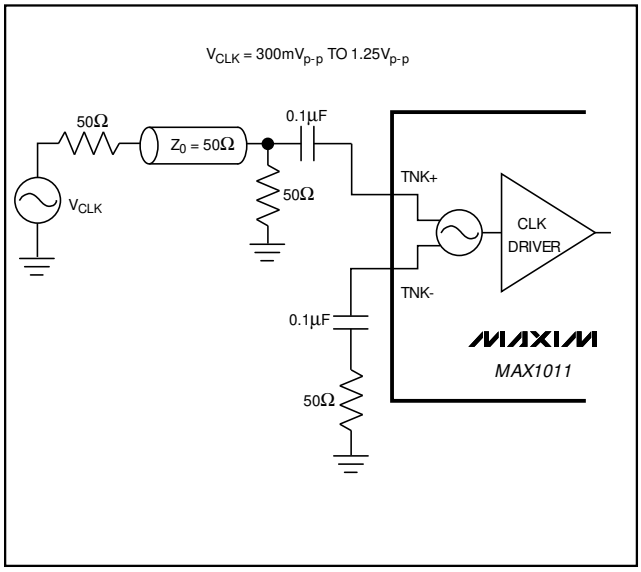


Figure 7. External Clock Drive Circuit

External Clock Operation

To accommodate designs that use an external clock, the MAX1011's internal oscillator can be overdriven by an external clock source (Figure 7). The external clock source should be a sinusoid to minimize clock phase noise and jitter, which can degrade the ADC's ENOB performance. AC couple the clock source (recommended voltage level is approximately 1Vp-p) to the oscillator inputs (Figure 7).

Output Data Format

The conversion results are output on a 6-bit-wide data bus. Data is latched into the ADC output latch following a pipeline delay of one clock cycle (Figure 8). Output data is clocked out of the ADC's data output pins (D0 through D5) on the rising edge of the clock output (DCLK), with a DCLK-to-data propagation delay (t_{PD}) of 3.0ns. The MAX1011 outputs are +3.3V CMOS-logic compatible.

Transfer Function

Figure 9 shows the MAX1011's nominal transfer function. Output coding is offset binary with 1LSB = FSR / 63.

Applications Information

The MAX1011 is designed with separate analog and digital power-supply and ground connections to isolate high-current digital noise spikes from the more sensitive analog circuitry. The high-current digital output ground (OGND) and analog ground (GND) should be at the same DC level, connected at only one location on the board. This will provide best noise immunity and improved conversion accuracy. Use of separate ground planes is strongly recommended.

The entire board needs good DC bypassing for both analog and digital supplies. Place the power-supply bypass capacitors close to where the power is routed onto the board, i.e., close to the connector. 10µF electrolytic capacitors with low-ESR ratings are recommended. For best effective bits performance, minimize capacitive loading at the digital outputs. Keep the digital output traces as short as possible.

The MAX1011 requires a +5V ±5% power supply for the analog supply (V_{CC}) and a +3.3V ±300mV power supply connected to V_{CCO} for the logic outputs. Bypass each of the V_{CC} supply pins to its respective GND with high-quality ceramic capacitors located as close to the package as possible (Table 2). Consult the evaluation kit manual for a suggested layout and bypassing scheme.

Table 2. Bypassing Guide

SUPPLY FUNCTION	V_{CC}/ V_{CCO} (PIN)	BYPASS TO GND/ OGND (PIN)	CAPACITOR VALUE
Analog Inputs	11	10	0.01µF
Oscillator/Clock	6	9	0.01µF
Converter	14	13	0.01µF
Digital Output	17	16	47pF

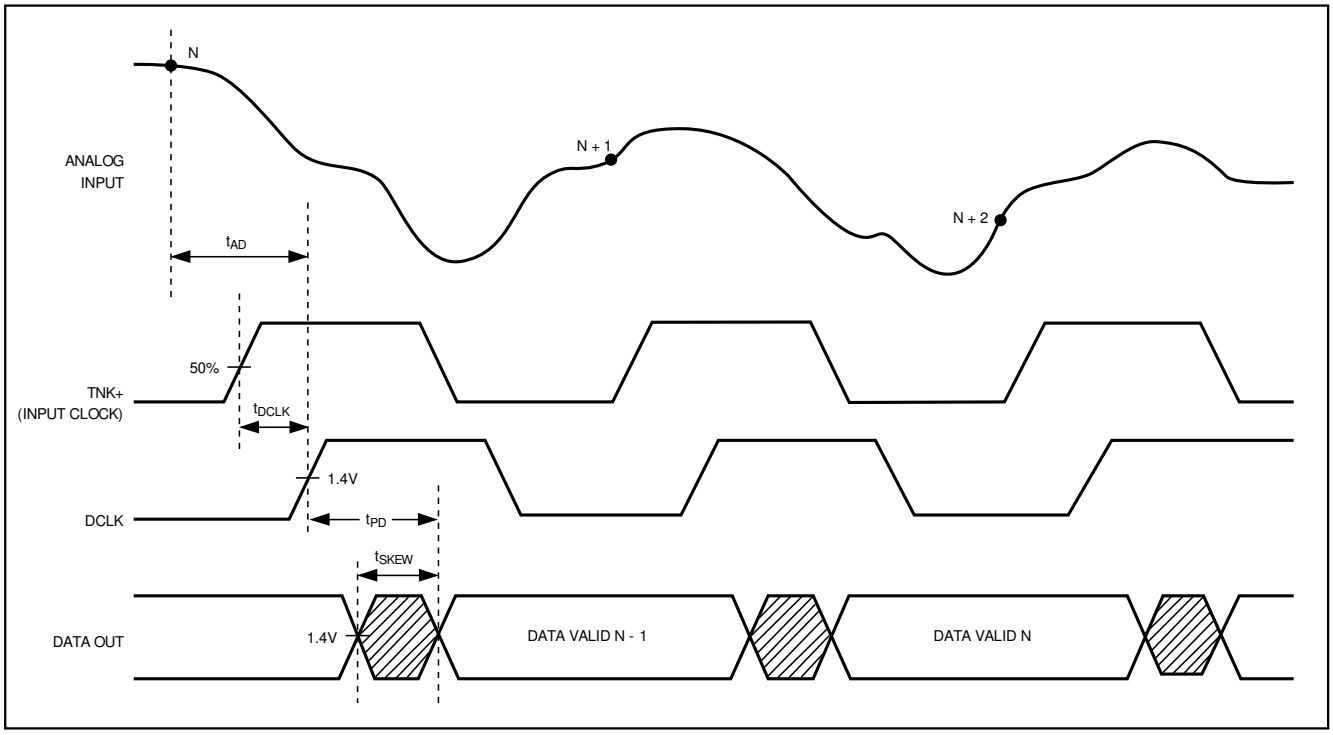


Figure 8. MAX1011 Timing Diagram

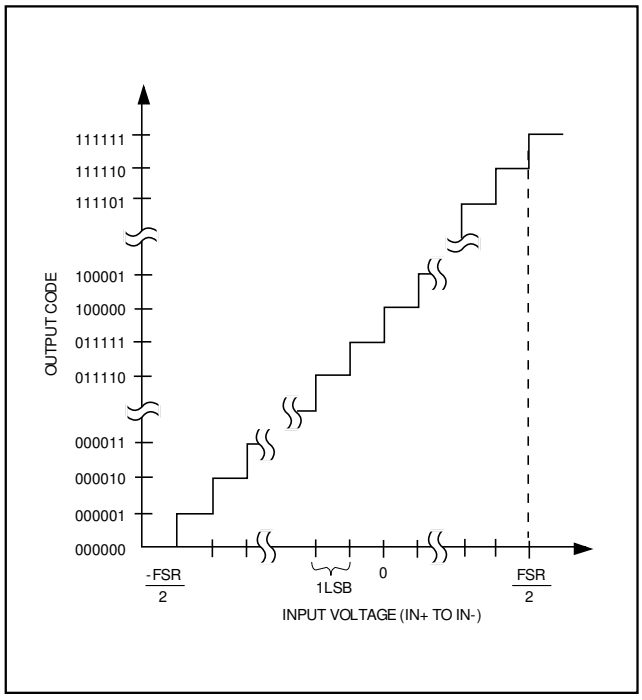


Figure 9. Ideal Transfer Function

Dynamic Performance

Signal-to-noise and distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to all other ADC output signals. The output spectrum is limited to frequencies above DC and below one-half the ADC sample rate.

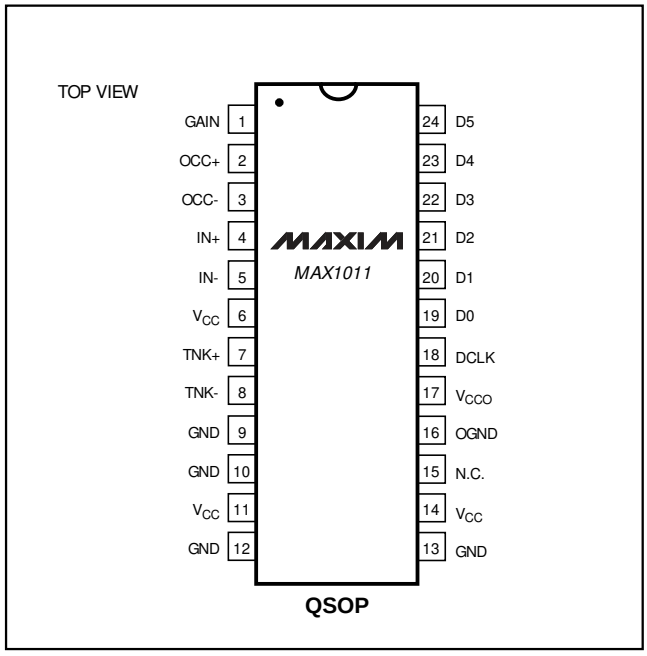
The theoretical minimum analog-to-digital noise is caused by quantization error, and results directly from the ADC's resolution: SNR = (6.02N + 1.76)dB, where N is the number of bits of resolution. Therefore, a perfect 6-bit ADC can do no better than 38dB.

The FFT Plot (see *Typical Operating Characteristics*) shows the result of sampling a pure 20MHz sinusoid at a 90MHz clock rate. This FFT plot of the output shows the output level in various spectral bands. The plot has been averaged to reduce the quantization noise floor and reveal the low-amplitude spurs. This emphasizes the excellent spurious-free dynamic range of the MAX1011.

The effective resolution (or effective number of bits) the ADC provides can be measured by transposing the equation that converts resolution to SINAD: N = (SINAD - 1.76)/ 6.02 (see *Typical Operating Characteristics*).

Low-Power, 90Msps, 6-Bit ADC

Pin Configuration



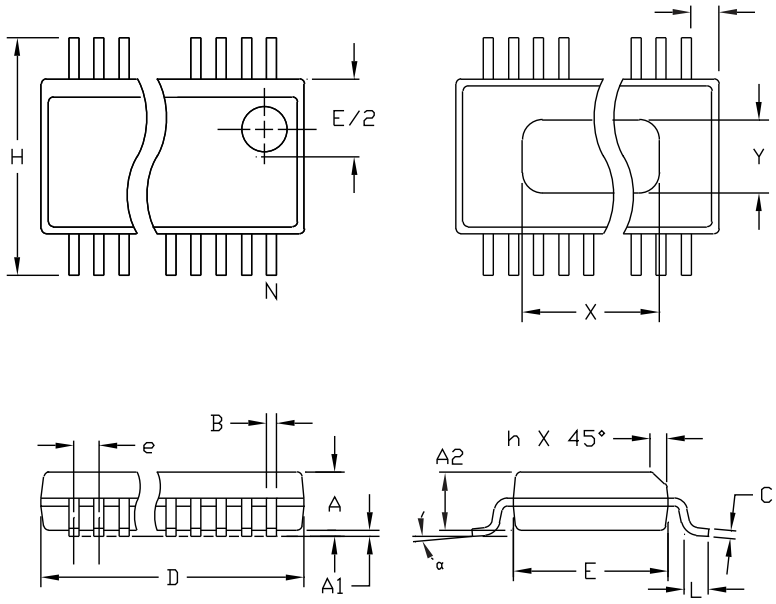
Chip Information

TRANSISTOR COUNT: 2823

SUBSTRATE CONNECTED TO GND

Package Information

QSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	B	1/1

NOTES