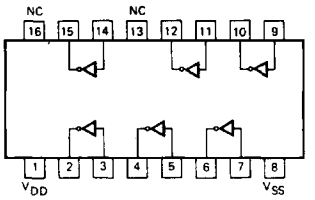
GD4049B • GD4050B

4049B HEX INVERTING BUFFER • 4050B HEX NON-INVERTING BUFFER

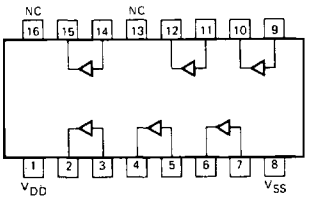
DESCRIPTION – These CMOS buffers provide high current output capability suitable for driving TTL or high capacitance loads. Since input voltages in excess of the buffers' supply voltage are permittad, these buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. The 4049B provides six inverting buffers, the 4050B six non-inverting buffers. Their guaranteed fan out into common bipolar logic elements is shown in Table 1.

4049B
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)

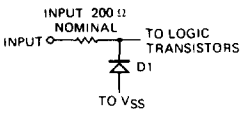


NOTE:
The SO Package has the same pinouts (Connection Diagram) as the Dual In-line Package.

4050B
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



INPUT PROTECTION



NOTE: Typical Breakdown Voltage of Diode D1 is 20 V

TABLE 1
Guaranteed fan out of 4049B, 4050B into common logic families

DRIVEN ELEMENT	GUARANTEED FAN OUT
Standard TTL, DTL	2
9LS, 93L, 74LS	9
74L	16

Conditions: V_{DD} = V_{CC} = 5.0 ± 0.25 V
V_{OL} = 0.5 V, T_A = 0 to 75 °C

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, 4049BXM and 4050BXM (See Note 1)

SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OH}	Output HIGH Current	-1.85 -1.25 -0.9	-2.5								mA	MIN, 25°C MAX	V_{OUT} = 2.5 V for V_{DD} = 5 V Inputs at 0 or V_{DD} per Function
		-0.62 -0.5 -0.35	-1		-1.85 -1.25 -0.9	-2.5		-5.5 -3.75 -2.7	-7.5		mA	MIN, 25°C MAX	V_{OUT} = 4.5 V for V_{DD} = 5 V V_{OUT} = 9.5 V for V_{DD} = 10 V V_{OUT} = 13.5 V for V_{DD} = 15 V Inputs at 0 or V_{DD} per Function
I_{OL}	Output LOW Current	3.75 3 2.1	6		10 8 5.6	16		30 24 16.8	48		mA	MIN, 25°C MAX	V_{OUT} = 0.4 V for V_{DD} = 5 V V_{OUT} = 0.5 V for V_{DD} = 10 V V_{OUT} = 1.5 V for V_{DD} = 15 V Inputs at 0 or V_{DD} per Function
		3.3 2.6 1.8	5.2								mA	MIN, 25°C MAX	V_{OUT} = 0.4 V for V_{DD} = 4.5 V Inputs at 0 V or V_{DD} per Function
I_{DD}	Quiescent Power Supply Current			1 30			2 60			4 120	μA	MIN, 25°C MAX	All Inputs at 0 V or V_{DD}

Notes on the following page.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, 4049BXC and 4050BXC (Cont'd) (See Note 1)

SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OH}	Output HIGH Current	-1.5									mA	MIN	V_{OUT} = 2.5 V for V_{DD} = 5 V
		-1.25	-2.5								mA	25°C	Inputs at 0 or V_{DD}
		-1.0									mA	MAX	per Function
		-0.6			-1.5			-4.5			mA	MIN	V_{OUT} = 4.5 V for V_{DD} = 5 V V_{OUT} = 9.5 V for V_{DD} = 10 V
		-0.5	-1		-1.25	-2.5		-3.75	-7.5		mA	25°C	V_{OUT} = 13.5 V for V_{DD} = 15 V
		-0.4			-1.0			-3			mA	MAX	Inputs at 0 or V_{DD} per Function
I_{OL}	Output LOW Current	3.6			9.6			28			mA	MIN	V_{OUT} = 0.4 V for V_{DD} = 5 V V_{OUT} = 0.5 V for V_{DD} = 10 V
		3.0	6		8	16		24	48		mA	25°C	V_{OUT} = 1.5 V for V_{DD} = 15 V
		2.5			6.6			19			mA	MAX	Inputs at 0 or V_{DD} per Function
		3.1									mA	MIN	V_{OUT} = 0.4 V for V_{DD} = 4.5 V
		2.6	5.2								mA	25°C	Inputs at 0 V or V_{DD}
		2.1									mA	MAX	per Function
I_{DD}	Quiescent Power Supply Current			4			8			16	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
				30			60			120		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 4049B only (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		65	130		30	65		29	52	ns	C_L = 50 pF,
t_{PHL}			50	105		25	50		17	40		R_L = 200 kΩ
t_{TLH}	Output Transition Time		73	145		40	80		30	60	ns	Input Transition
t_{THL}			33	65		13	25		9	20		Times ≤ 20 ns

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

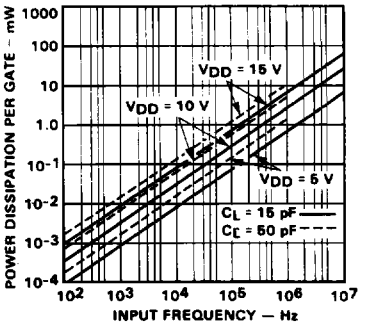
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 4050B only (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		65	130		30	65		24	52	ns	C_L = 50 pF,
t_{PHL}			43	95		23	45		17	36		R_L = 200 kΩ
t_{TLH}	Output Transition Time		73	145		90	80		30	60	ns	Input Transition
t_{THL}			33	65		13	25		9	20		Times ≤ 20 ns

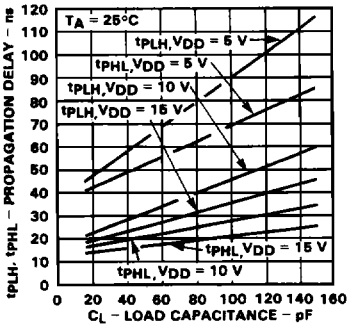
Notes on preceeding page.

TYPICAL ELECTRICAL CHARACTERISTICS

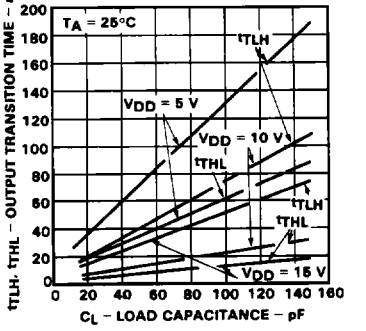
TYPICAL POWER DISSIPATION VERSUS FREQUENCY



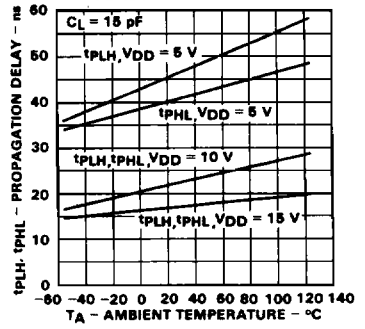
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



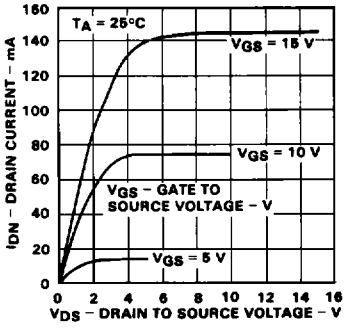
OUTPUT TRANSITION TIME VERSUS LOAD CAPACITANCE



PROPAGATION DELAY VERSUS TEMPERATURE



N-CHANNEL DRAIN CHARACTERISTICS



P-CHANNEL DRAIN CHARACTERISTICS