

#### Dual Hall Effect Latch with Speed & Direction Detection

#### **Features and Benefits**

- Operating Voltage from 2.7V to 24V
- Two Integrated Hall plates for Direction Detection
- Latching Magnetic Characteristics
- Speed & Direction Open-Drain Outputs
- Direction Output updated prior Speed Output
- Excellent Temperature Stability
- Reverse Supply Voltage Protection
- Output Current Limitation and Auto-Shutoff
- Under-Voltage Lockout Protection

### **Ordering information**

### Applications

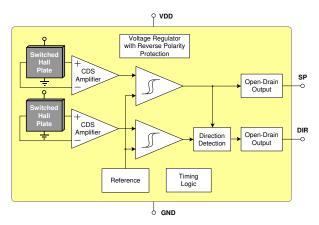
- Windows lifter with Anti-Pinch feature
- Rotation speed & direction detection
- Linear speed & direction detection
- Angular position detection
- Power closures with Anti-Pinch features

Part No.	Temperature Code	Sensitivity	Package Code	Packing Form
MLX92251LSE-AAA-000-RE	L (-40°C to 150°C)	± 7.5 mT	SE (TSOT-5L)	RE (Tape & Reel)
MLX92251LSE-ABA-000-RE	L (-40°C to 150°C)	± 2.5 mT	SE (TSOT-5L)	RE (Tape & Reel)

#### Legend:

Temperature Code:	L for Temperature Range -40°C to 150°C
Package Code:	SE for TSOT,
Packing Form:	RE for Reel
Ordering example:	MLX92251LSE-AAA-000-RE

## **1. Functional Diagram**



## 2. General Description

The Melexis MLX92251 is a second generation Hall-effect dual latch designed in mixed signal CMOS technology. The device integrates a voltage regulator, two Hall sensors with advanced offset cancellation system and two open-drain output drivers, all in a single package. Two Hall plates are integrated on the same piece of silicon, thus using the high precision of the wafer fabrication process to ensure a fixed

spacing of 1.45mm between the sensing elements. The first Hall plate signal is used to provide the speed signal output. The combination of both the first and second Hall plate signals is then internally processed to directly deliver a direction signal output.

The MLX92251 shares the MLX922xx-based platform, synonym of high performance in terms of electrical specification, magnetic specification and protection level.

With latching magnetic characteristics, the speed (SP) output is turned low or high respectively with a sufficiently strong South or North pole facing the package top side. When removing the magnetic field, the device keeps its previous state.

The direction (DIR) output is latched in Low or High state depending on the movement direction of the applied magnetic field, as a result of certain magnetic pulse sequence on both Hall sensors.

The MLX92251 is delivered in a Green compliant 5-pin Thin Small Outline Transistor (TSOT) for surface-mount process.



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## 3. Glossary of Terms

MilliTesla (mT), Gauss	Units of magnetic flux density: 1mT = 10 Gauss
RoHS	Restriction of Hazardous Substances
TSOT	Thin Small Outline Transistor – also referred with the Melexis package code "SE"
ESD	Electro-Static Discharge

## 4. Pin Definitions and Descriptions



Pin #	Name	Description
1	SPEED	Open-Drain Output
2	DIRECTION	Open-Drain Output
3	VDD	Power Supply
4	GND	Ground pin
5	GND	Ground pin

Note: Both GND pins should be connected (pin 4 and pin 5)

## 5. Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Supply Voltage	$V_{\text{DD}}$	+27	V
Supply Current	IDD	+20	mA
Reverse Supply Voltage	V <sub>DDREV</sub>	-27	V
Reverse Supply Current	Iddrev	-20	mA
Output Voltage	Vout	+27	V
Output Current	Іоит	+20	mA
Reverse Output Voltage	VOUTREV	-0.5	V
Reverse Output Current	IOUTREV	-50	mA
Operating Temperature Range	T <sub>A</sub>	-40 to +150	°C
Storage Temperature Range	Ts	-55 to +165	°C
Maximum Junction Temperature	ΤJ	+165	°C
ESD Sensitivity – HBM <sup>(1)</sup>	-	2500	V
ESD Sensitivity – CDM <sup>(2)</sup>	-	1000	V
Magnetic Flux Density	В	Unlimited	mT

Exceeding the absolute maximum ratings may cause permanent damage.

Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>&</sup>lt;sup>1</sup> Human Body Model according AEC-Q100-002 standard.

<sup>&</sup>lt;sup>2</sup> Charged Device Model according AEC-Q100-011 standard. REVISION 005 – DECEMBER 2022

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### 6. General Electrical Specifications

#### DC Operating Parameters T<sub>A</sub> = -40°C to 150°C, V<sub>DD</sub> = 2.7V to 24V (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Units
Supply Voltage	V <sub>DD</sub>	Operating	2.7	-	24	V
Supply Current	I <sub>DD</sub>	$V_{DD} = 12V$	3	4.5	7	mA
Reverse Supply Current	IDDREV	V <sub>DD</sub> = -18V			1	mA
Output Leakage Current	IOFF	$V_{OUT}$ = 12V, $V_{DD}$ = 12V, $B < B_{RP}$		0.1	10	μΑ
Output Saturation Voltage	Vouts	B > Bop, Iout = 10mA		0.2	0.5	V
Output Rise/Fall Time (2,3)	t <sub>R</sub> / t <sub>F</sub>	$V_{DD} = 12V, V_{PU}$ <sup>(4)</sup> = 5V, $R_{PU} = 1k\Omega, C_L = 50pF$	0.1	0.3	1	μs
Output Current Limit	I <sub>CL</sub>	$B > B_{OP}$ , $V_{OUT} = 12V$	14	25	44	mA
Output ON Time under Current Limit conditions <sup>(5)</sup>	t <sub>clon</sub>	B > B <sub>OP</sub> , V <sub>PU</sub> = 12V, R <sub>PU</sub> = 100Ω	150	230		μs
Output OFF Time under Current Limit conditions <sup>(5)</sup>	tcloff	B > B <sub>OP</sub> , V <sub>PU</sub> = 12V, R <sub>PU</sub> = 100Ω		3.5		ms
Chopping Frequency	<b>f</b> CHOP			400		kHz
Speed Signal Delay <sup>(2,6)</sup>	tspd		0.4	0.85	1.6	μs
Output Refresh Period	t <sub>PER</sub>		3.2	5	8.4	μs
Output Jitter (p-p value) <sup>(2)</sup>	t <sub>JITTER</sub>	Over 1000 successive output switching events @1kHz square wave, B <sub>PEAK</sub> = 50mT, t <sub>RISE</sub> =t <sub>FALL</sub> ≤100μs		±2.6		μs
Maximum Switching Frequency <sup>(2,7)</sup>	fsw	≥30mT square wave magnetic field	40	66		kHz
Power-On Time <sup>(8)</sup>	<b>t</b> PON	$V_{DD}$ = 5V, $dV_{DD}/dt > 2V/\mu s$		16	35	μs
Under-voltage Lockout Threshold	VUVL		2.2	2.4	2.7	V
Under-voltage Lockout Reaction time <sup>(2)</sup>	tuvl			1		μs
SE Package Thermal Resistance	Rтн	Single layer (1S) JEDEC board		300		°C/W

8 The Power-On Time represents the time from reaching  $V_{DD} = 2.7V$  to the first refresh of the SP output REVISION 005 – DECEMBER 2022

<sup>1</sup> Typical values are defined at  $T_A = +25$  °C and  $V_{DD} = 12V$ 

<sup>2</sup> Based on device characterization results, not subject to production test

<sup>3</sup> Measured between  $0.1*V_{PU}$  and  $0.9*V_{PU}$ 

<sup>4</sup> *R*<sub>PU</sub> and *V*<sub>PU</sub> are respectively the external pull-up resistor and pull-up power supply

<sup>5</sup> If the Output is in Current Limitation longer than t<sub>CLON</sub> the Output is switched off in high-impedance state. The Output returns back in active state at next reaching of B<sub>OP</sub> or after t<sub>CLOFF</sub> time interval

<sup>6</sup> Controlled delay between direction (DIR) signal update and speed (SP) signal update

<sup>7</sup> Maximum switching frequency corresponds to the max frequency of the applied magnetic field which is detected without loss of pulses

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## 7. Magnetic Specifications

### 7.1. MLX92251LSE-AAA-000

#### DC Operating Parameters $V_{DD}$ = 2.7V to 24V and $T_A$ =-40°C to 150°C (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Units
Operating Point	B <sub>OP</sub>		5	7.5	10	mT
Release Point	B <sub>RP</sub>		-10	-7.5	-5	mT
Magnetic Matching	D	$B_{OP1} - B_{OP2} \text{ or } B_{RP1} - B_{RP2}, T_A = 25^{\circ}C$	-2		2	mT
	B <sub>MATCH</sub>	BOP1 – BOP2 OF BRP1 – BRP2	-3		3	mT
Magnetic Offset	B <sub>OFF</sub>	(B <sub>OP1</sub> + B <sub>RP1</sub> ) / 2, (B <sub>OP2</sub> + B <sub>RP2</sub> ) / 2	-2		2	mT
Temperature Coefficient	тс			0		ppm/°C
Hall Plates Spacing	-			1.45		mm

### 7.2. MLX92251LSE-ABA-000

DC Operating Parameters  $V_{DD}$  = 2.7V to 24V and  $T_A$  =-40°C to 150°C (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Units
Operating Point	B <sub>OP</sub>		0.6	2.5	4.5	mT
Release Point	B <sub>RP</sub>		-4.5	-2.5	-0.6	mT
Magnetic Matching		$B_{OP1} - B_{OP2} \text{ or } B_{RP1} - B_{RP2}, T_A = 25^{\circ}C$	-2		2	mT
	B <sub>MATCH</sub>	$B_{OP1} - B_{OP2} \text{ or } B_{RP1} - B_{RP2}$	-3		3	mT
Magnetic Offset	BOFF	(B <sub>OP1</sub> + B <sub>RP1</sub> ) / 2, (B <sub>OP2</sub> + B <sub>RP2</sub> ) / 2	-2		2	mT
Temperature Coefficient	TC			-1100		ppm/°C
Hall Plates Spacing	-			1.45		mm

**Note:** Temperature coefficient value is guaranteed by design and verified by characterization and is calculated using the following formula:

$$TC = \frac{B_{T2} - B_{T1}}{B_{25^{\circ}C} \times (T_2 - T_1)} * 10^{6}, ppm/^{\circ}C; \quad T_1 = -40^{\circ}C; \quad T_2 = 150^{\circ}C$$

Dual Hall Effect Latch with Speed & Direction

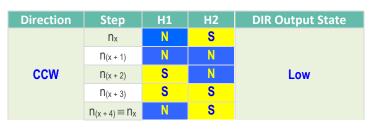


### 8. Output Behavior versus Magnetic Pole

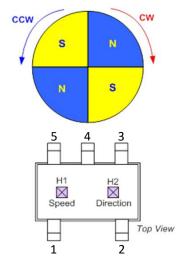
#### DC Operating Parameters $T_A = -40^{\circ}$ C to 150°C, $V_{DD} = 2.7$ V to 24V (unless otherwise specified)

Parameter	Test Conditions	SP Output State
South pole	B > B <sub>OP</sub>	Low
North pole	B < B <sub>RP</sub>	High <sup>(1)</sup>

Output behavior versus magnetic pole<sup>(2)</sup>



Direction	Step	H1	H2	DIR Output State
cw	n <sub>x</sub>	N	S	High <sup>(3)</sup>
	N(x + 1)	S	S	
	N(x + 2)	S	N	
	N(x + 3)	N	N	
	$n_{(x+4)} \equiv n_x$	N	S	



<sup>&</sup>lt;sup>1</sup> Default SP output state during power-up

<sup>&</sup>lt;sup>2</sup> Magnetic pole applied perpendicularly to Hall plate "H1", facing the branded/top side of the package

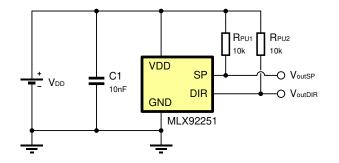
<sup>&</sup>lt;sup>3</sup> Default magnetic and DIR output state during power-up REVISION 005 – DECEMBER 2022

Dual Hall Effect Latch with Speed & Direction

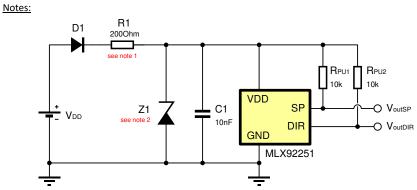


### 9. Application Information

### 9.1. Default Application Schematic



### 9.2. Recommended Application Schematic for ISO7637-2 (pulses 5a and 5b)

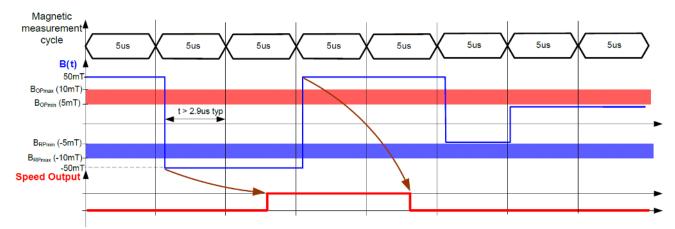


1. Recommended for conducted transients on supply line above 32V with duration above 500ms.

 $\ \ 2. \ \ Recommended \ \ for \ \ conducted \ \ transients \ \ on \ \ supply \ \ line \ \ above \ \ 36V.$ 

3. Recommended zener diode Z1 is BZX55C27 or equivalent.

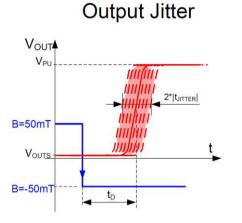
#### 9.3. Speed (SP) Output Behavior vs. BOP/BRP



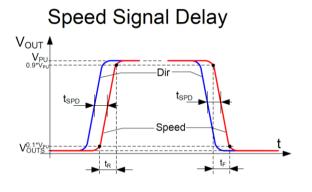
Note: The decision for output update is taken at the end of each magnetic measurement cycle



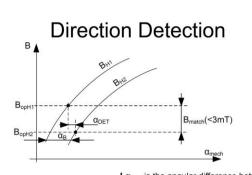
### 9.4. Output Jitter, Speed Signal Delay and Direction Detection

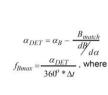


Note: t<sub>D</sub>=8us typ for DIR output and t<sub>D</sub>=8.85us typ for SP output, based on simulation



### 9.5. UV lockout and POR behaviour



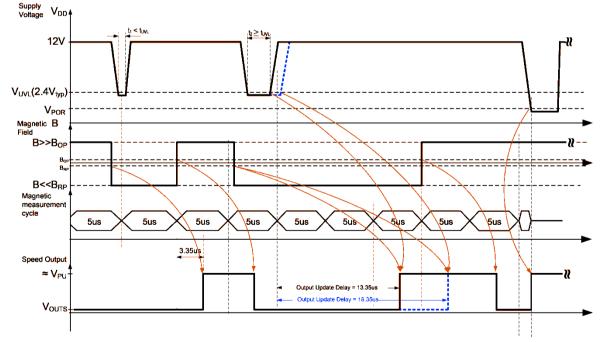


 $\begin{array}{l} \alpha_{\text{DET}} \text{ is the angular difference between H1} \\ \text{and H2 magnetic threshold crossing points;} \\ \textbf{B}_{\text{H1}} \left(\textbf{B}_{\text{H2}}\right) \text{ is the magnetic field facing Hall plate} \\ \text{H1(H2) as a function of the mechanical angle } \alpha_{\text{mech}}\text{;} \\ \alpha_{\text{B}} \text{ is the angular difference between B}_{\text{H1}} \text{ and B}_{\text{H2}}\text{;} \\ \textbf{B}_{\text{match}}\text{-} 3\text{mT} \text{ is the magnetic matching (see Magnetic Specifications section)} \end{array}$ 

 $\begin{array}{l} dB/d\alpha \text{ is the magnetic field gradient} \\ f_{Bmax} \text{ is the maximum magnetic field frequency at} \\ \text{which the direction will be detected without error} \\ \Delta t \text{ is the time difference between H1 and H2} \\ \text{magnetic threshold crossing points;} \end{array}$ 

For example, if  $\alpha_B = 5^\circ$  and dB/d $\alpha > 1$ mT/ $^\circ$ ;

for MLX92251  $\Delta t$  = 10us (definitely > 2\*|t<sub>JITTER</sub>|) could be assumed; The calculated f<sub>Bmax</sub> = 555Hz.



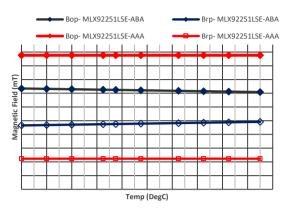
NOTE: Start-up behaviour feature does not occur after under-voltage lockout. V<sub>POR</sub>≤ 2V (based on device characterization results).

Dual Hall Effect Latch with Speed & Direction

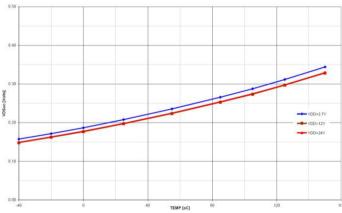


## **10. Performance Graphs**

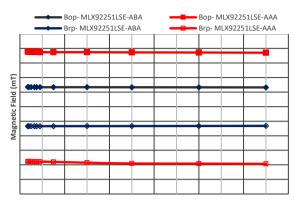
### 10.1. Magnetic parameters vs. T<sub>A</sub>



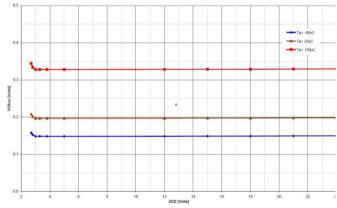




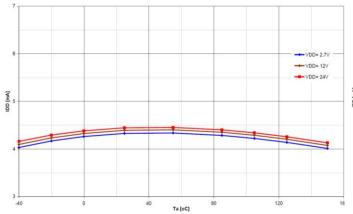
## 10.2. Magnetic parameters vs. V<sub>DD</sub>



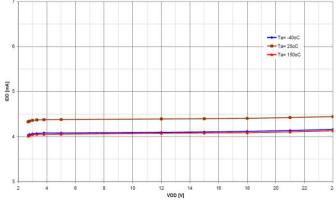








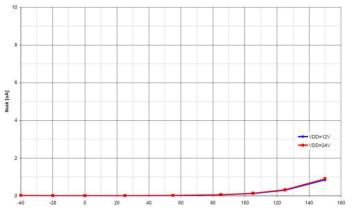
### 10.6. $I_{DD}$ vs. $V_{DD}$

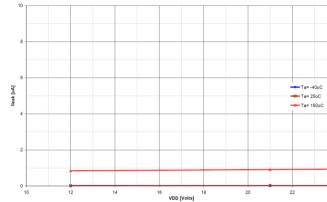


Dual Hall Effect Latch with Speed & Direction



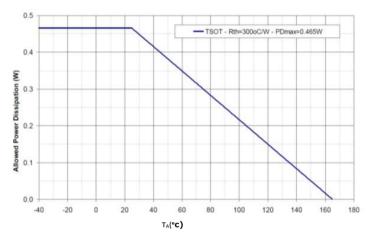
### 10.7. Ileak vs. Ta





10.8. ILEAK VS. VDD

### 10.9. Power Derating vs. T<sub>A</sub>





## **11. Standard information**

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

#### Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020 Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
   Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing (reflow profiles according to table 2)

#### Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
- Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15 Resistance to soldering temperature for through-hole mounted devices

#### Iron Soldering THD's (Through Hole Devices)

• EN60749-15 Resistance to soldering temperature for through-hole mounted devices

#### Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

• EIA/JEDEC JESD22-B102 and EN60749-21 Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis recommends reviewing on our web site the General Guidelines <u>soldering recommendation</u> (<u>http://www.melexis.com/Quality\_soldering.aspx</u>) as well as <u>trim&form recommendations</u> (<u>http://www.melexis.com/Assets/Trim-and-form-recommendations-5565.aspx</u>).

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: <u>http://www.melexis.com/quality.aspx</u>

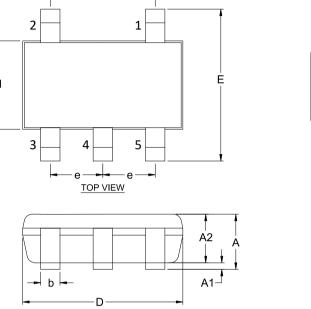
### **12. ESD Precautions**

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD). Always observe Electro Static Discharge control procedures whenever handling semiconductor products. Dual Hall Effect Latch with Speed & Direction

## 13. TSOT-5L (SE) Package Information

## 13.1. TSOT-5L – Package dimensions

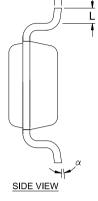
e1



S Y M BO L	MINIMUM	MAXIMUM	
A		1.00	
A1	0.025	0.10	
A2	0.85	0.90	
D	2.80	3.00	
E	2.60	3.00	
E1	1.50	1.70	
L	0.30	0.50	
b	0.30	0.45	
С	0.10	0.20	
е	0.95 BSC		
e1	1.90 BSC		
α	0°	8°	



NOTE :





# 6. FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITH 0.076 mm SEATING PLANE.

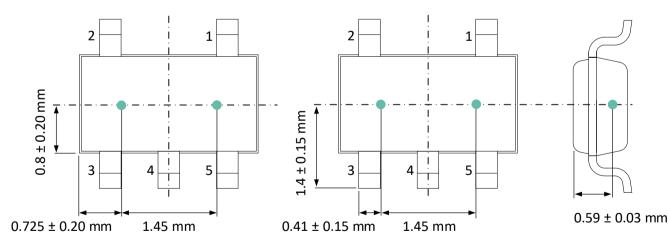
SIDE VIEW

1. ALL DIMENSIONS IN MILLIMETERS (mm) UNLESS OTHERWISE STATED.

4. DIMENSION & DOES NOT INCLUDE DAMBAR PROTRUSION OF MAX 0.07 mm. 5. DIMENSION L IS THE LENGTH OF THE TERMINAL FOR SOLDERING TO A SUBTRATE.

2. DIMENSION D DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS OF MAX 0.15 mm PER SIDE. 3. DIMENSION E DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS OF MAX 0.25 mm PER SIDE.

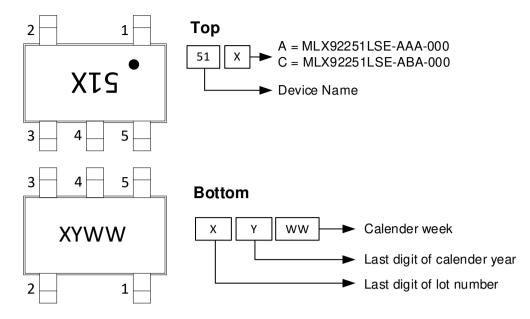
## 13.2. TSOT-5L – Sensitive spots



Dual Hall Effect Latch with Speed & Direction



## 13.3. TSOT-5L – Package marking





## 14. Contact

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### **15. Disclaimer**

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