Dual MOSFET Gate Driver, High Performance

NCP81080

The NCP81080 is a high performance dual MOSFET gate driver optimized to drive half bridge N−Channel MOSFETs. The NCP81080 uses a bootstrap technique to ensure a proper drive of the high−side power switch. A high floating top driver design can accommodate HB voltage as high as 180 V. The NCP81080 has an internal anti−cross conduction circuit with a 135 ns fixed internal dead−time to prevent current shoot−through. The NCP81080 is available in 2x2mm DFN and SOIC packages.

Features

- Drives Two N−Channel MOSFETs in High−Side and Low−Side Configuration
- Floating Top Driver Accommodates Boost Voltage up to 180 V
- Switching Frequency up to 500 Khz
- Current Shoot−Through Protection
- 135 ns Fixed internal Dead−Time
- 44 ns Rising and 30 ns Falling Propagation Delay Times
- 0.5 A peak Source Current with 0.8 A Peak Sink Current
- 19 ns Rise/17 ns Fall Times with 1000−pF Load
- High−Side & Low−Side UVLO Protection

Applications

- Telecom and Datacom
- Isolated Non−Isolated Power Supply Architectures
- Class−D Audio Amplifiers
- Two Switch and Active Clamp Forward Converters
- Motor Drives

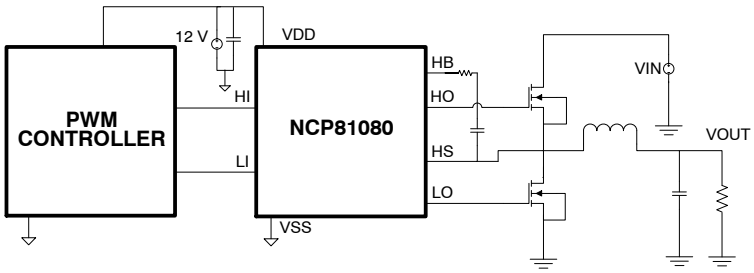

Figure 1. Typical Application Circuit

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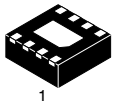
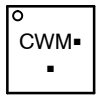
MARKING DIAGRAMS

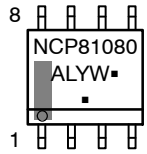


DFN8
MN SUFFIX
CASE 506AA



CW = Specific Device Code
M = Date Code
▪ = Pb−Free Device
(Note: Microdot may be in either location)

SOIC−8
CASE 751



NCP81080 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

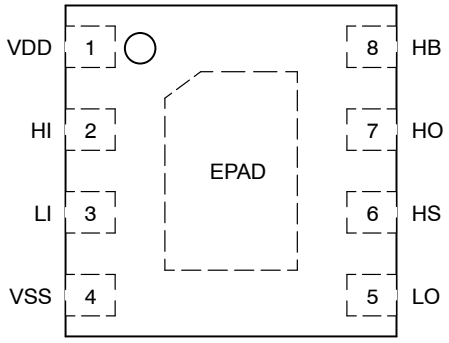
ORDERING INFORMATION†

Device	Package	Shipping
NCP81080MNTBG	DFN8 (Pb−Free)	3000 / Tape & Reel
NCP81080DR2G	SOIC8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 1. PIN DESCRIPTION TABLE

Pin No.	Symbol	Description
1	VDD	Positive supply for the low−side driver
2	HI	High−Side Input
3	LI	Low−Side Input
4	VSS	Negative Supply Return
5	LO	Low−Side Output
6	HS	High−Side Source
7	HO	High−Side Output
8	HB	High−Side Bootstrap
9	EPAD	Connect EPAD to VSS



(Top View)

Table 2. MAXIMUM RATINGS

Parameter		Value	Unit
VDD		−0.3 to 24	V
$V_{HB} - V_{SS}$		−0.3 to 200	V
$V_{HO} - V_{HS}$	DC	−0.3 to V_{HB} + 0.3	V
	Repetitive Pulse < 100 ns	−2 to V_{HB} + 0.3, ($V_{HB} - V_{HS}$ <20)	
$V_{HS} - V_{SS}$	DC	−20 to 200 − VDD	V
$V_{LO} - V_{SS}$	DC	−0.3 to VDD + 0.3	V
	Repetitive pulse < 100 ns	−2 to VDD + 0.3	
V_{HI}, V_{LI}		−10 to 24	V
$V_{HB} - V_{HS}$		−0.3 to 24	V
I_{Diode}	AC (Peak current)	8	A
Operating virtual Junction Temp Range, T_J		−40 to 170	°C
Storage Temperature, T_{STG}		−65 to 150	°C
Lead Temperature (Soldering, 10 sec)		+300	°C
HBM		800	V
CDM		2000	V

Table 3. RECOMMENDED OPERATING CONDITIONS

Parameter		Min	Nom	Max	Unit
V_{DD}	Supply Voltage Range	5.5	12	20	V
V_{HS}	Voltage on HS (DC)	−10		180	
V_{HB}	Voltage on HB	V_{HS} + 5.5		V_{HS} + 20	
	Voltage Slew Rate on HS			30	V / ns
T_J	Operating Junction Temperature Range	−40		+140	°C

Table 4. ABSOLUTE MAXIMUM RATINGS

Thermal Characteristic	DFN	SOIC	Unit
θ_{JA} Junction to Ambient thermal resistance	97	146	°C/W
θ_{JCT} Junction to case (Top) thermal resistance	181	72	
θ_{JCB} Junction to case (Bottom) thermal resistance	1.9	67	
ψ_{JT} Junction to top characterization parameter	2.2	7.2	
ψ_{JB} Junction to board characterization parameter	2.0	64	
Moisture Sensitivity Level – QFN Package	MSL	1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*The maximum package power dissipation must be observed.
2) JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM
3) JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM
*All signals referenced to VSS unless otherwise noted.

Table 5. ELECTRICAL CHARACTERISTICS
Unless otherwise stated: $T_A = T_J = -40°C$ to 140°C; VDD = VHB = 12 V, VHS = VSS = 0 V, No load on LO or HO

Parameter		Test Condition	Min	Typ	Max	Units
SUPPLY CURRENTS						
I_{DD}	VDD quiescent current	$V_{LI} = V_{HI} = 0$		0.85	1.6	mA
I_{DDO}	VDD operating current	f = 500 kHz, C_{LOAD} = 0		5.1	9.0	
		f = 300 kHz, C_{LOAD} = 0		3.5	6.5	
I_{HB}	Boot voltage quiescent current	$V_{LI} = V_{HI}$ = 0 V		0.65	1.6	
I_{HBO}	Boot voltage operating current	f = 500 kHz, C_{LOAD} = 0		4.8	9.0	
		f = 300 kHz, C_{LOAD} = 0		3.4	6.5	
I_{HBS}	HB to Vss quiescent current	$V_{HS} = V_{HB}$ = 110 V		8.0	100	μA
I_{HBSO}	HB to Vss operating current	f = 500 kHz, C_{LOAD} = 0		0.2		mA
INPUT						
V_{HIH}, V_{LIH}	Input voltage high		2.0			V
V_{HIL}, V_{LIL}	Input voltage low				0.8	
R_{IN}	Input Pulldown Resistance		100	175	350	kΩ
UNDERVOLTAGE PROTECTION (UVLO)						
VDD	VDD rising threshold		3.4	4.4	5.4	V
VDD	VDD Threshold hysteresis			0.4		
VHB	VHB rising threshold		3.4	4.4	5.4	
VHB	VHB Threshold hysteresis			0.35		
BOOTSTRAP DIODE						
V_F	Low−current forward voltage	I_{VDD} − HB = 100 μA		0.61	0.85	V
V_{FI}	High−current forward voltage	I_{VDD} − HB = 100 mA		0.93	1.1	
R_D	Dynamic resistance, ΔVF/ΔI	I_{VDD} − HB = 100 mA and 80 mA		2.1	3.5	Ω
LO GATE DRIVER						
V_{LOL}	Low level output voltage	I_{LO} = 100 mA		0.31	1.2	V
V_{LOH}	High level output voltage	I_{LO} = −100 mA, $V_{LOH} = V_{DD} - V_{LO}$		0.75	1.6	
	Peak Pull−Up Current	V_{LO} = 0 V		0.55		A
	Peak Pull−Down Current	V_{LO} = 12 V		0.8		
$R_{O, Unbiased}$		VCC = VSS		20k		Ω

Table 5. ELECTRICAL CHARACTERISTICS
Unless otherwise stated: $T_A = T_J = -40°C$ to 140°C; VDD = VHB = 12 V, VHS = VSS = 0 V, No load on LO or HO

Parameter		Test Condition	Min	Typ	Max	Units
HO GATE DRIVER						
V_{HOL}	Low level output voltage	I_{HO} = 100 mA		0.3	1.2	V
V_{HOH}	High level output voltage	I_{HO} = −100 mA, $V_{HOH} = V_{HB}-V_{HO}$		0.71	1.6	
	Peak Pull−Up Current	V_{HO} = 0 V		0.55		A
	Peak Pull−Down Current	V_{HO} = 12 V		0.8		
$R_{O, Unbiased}$		HB − HS = 0 V		20k		Ω
PROPAGATION DELAYS						
t_{DLFF}	PWM falling to V_{LO} falling	C_{LOAD} = 0		30		ns
t_{DHFF}	PWM falling to V_{HO} falling	C_{LOAD} = 0		30		
t_{DLRR}	PWM rising to V_{LO} rising	C_{LOAD} = 0		44		
t_{DHRR}	PWM rising to V_{HO} rising	C_{LOAD} = 0		44		
DEAD−TIME						
Fixed Deadtime	Internal Fixed Dead−Time			135		ns
DEAD−TIME MATCHING						
t_{DTM}	LI OFF, HI ON			10		ns
OUTPUT RISE AND FALL TIME						
t_R	LO, HO	C_{LOAD} = 1000 pF		19		ns
t_F	LO, HO	C_{LOAD} = 1000 pF		17		
MISCELLANEOUS						
	Minimum input pulse width that changes the output			30		ns
	Bootstrap diode turn−off time	I_F = 20 mA, I_{REV} = 0.5 A (Notes 1, 2)		50		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
1. Typical values for T_A = 25°C
2. I_F: Forward current applied to bootstrap diode, I_{REV}: Reverse current applied to bootstrap diode.

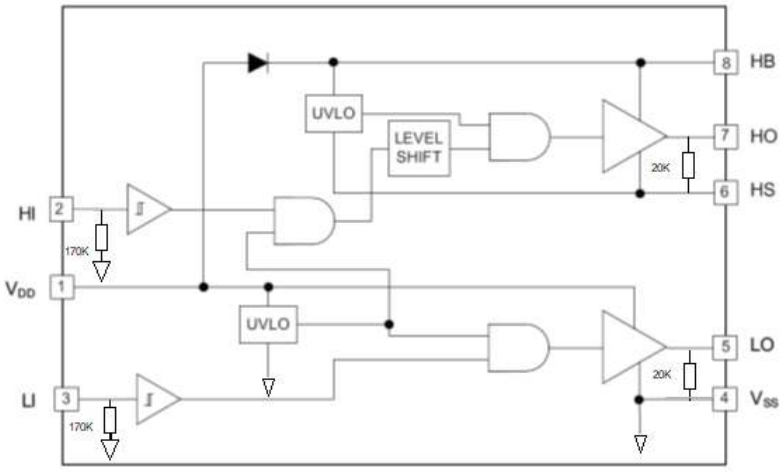


Figure 2. Internal Block Diagram

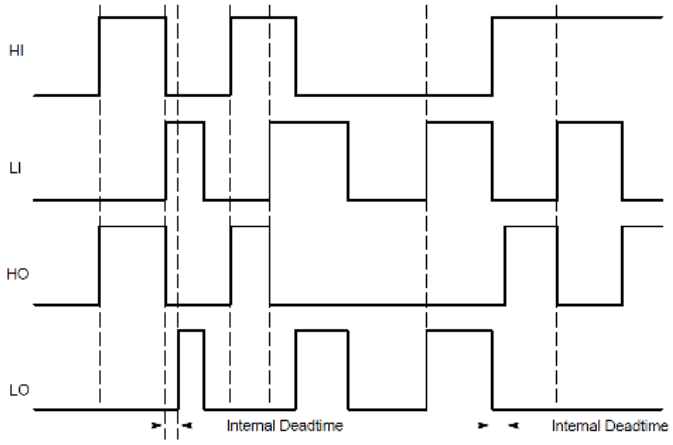


Figure 3. Timing Diagram

NOTE: The NCP81080 has a fixed internal dead−time of 135 ns.

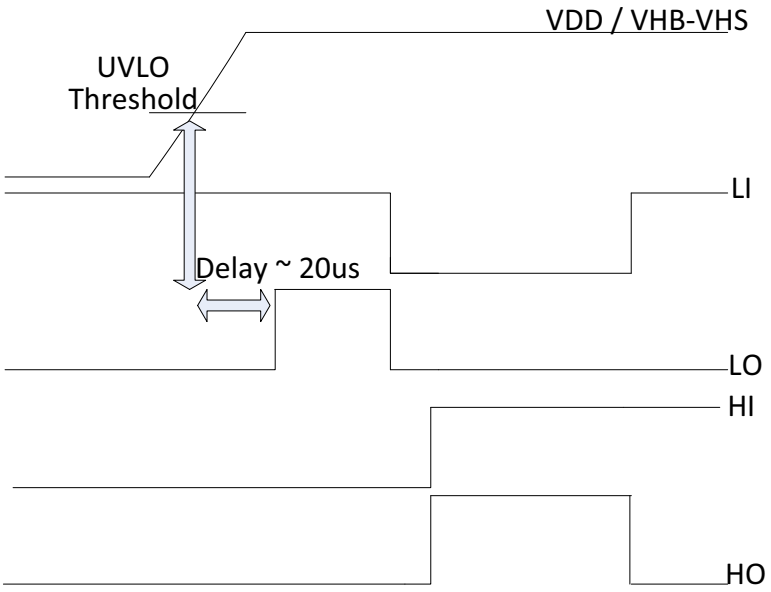


Figure 4. Output Logic at UVLO Crossing

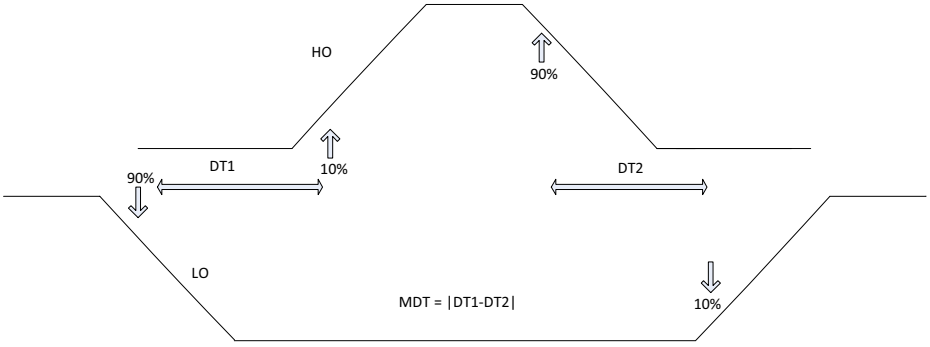


Figure 5. Dead−Time Matching

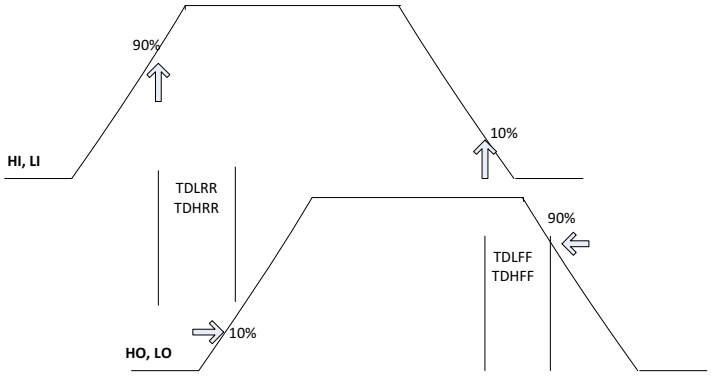


Figure 6. Propagation Delays

TYPICAL CHARACTERISTICS

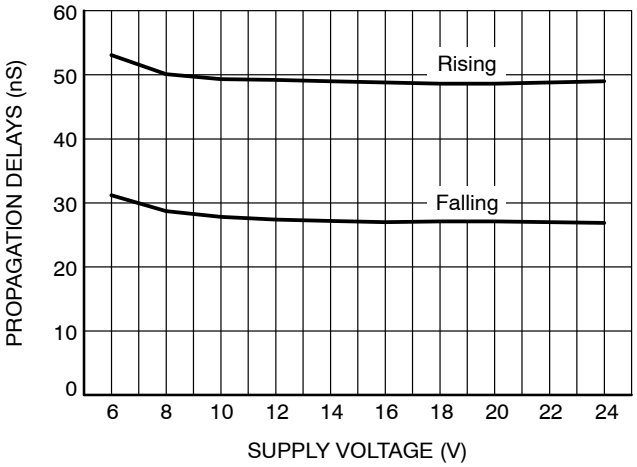


Figure 7. Propagation Delays vs. Supply Voltage

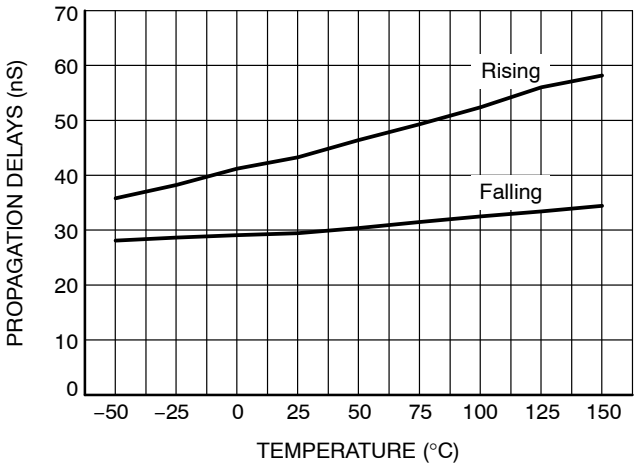


Figure 8. Propagation Delays vs. Temperature

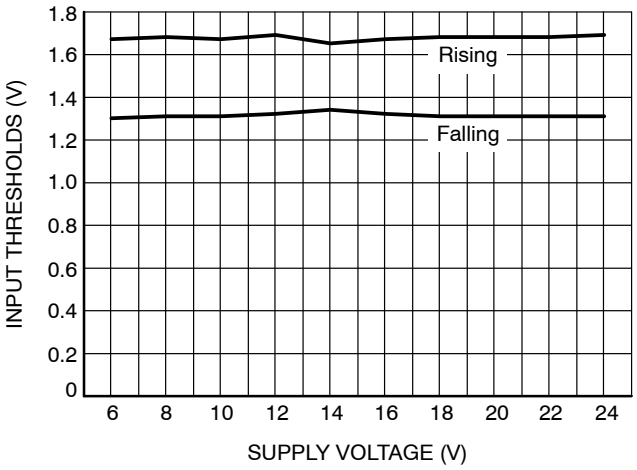


Figure 9. Input Thresholds vs. Supply Voltage

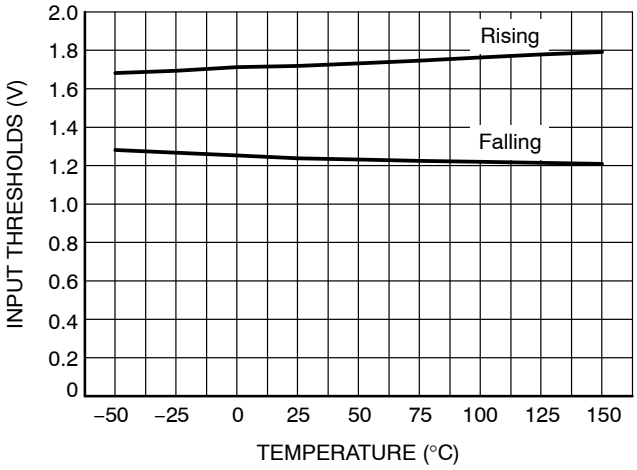


Figure 10. Input Thresholds vs. Temperature

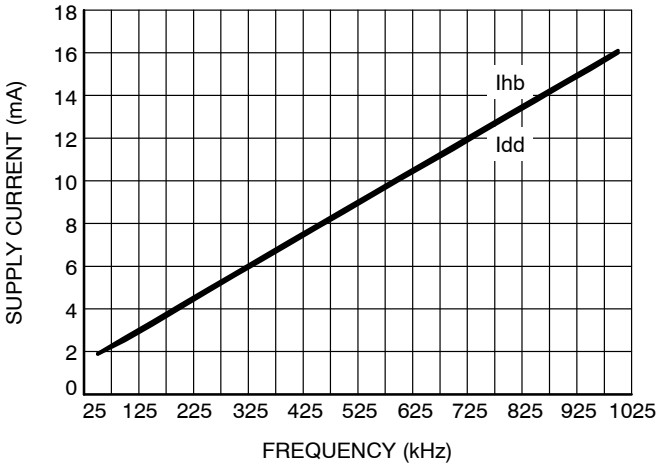


Figure 11. Supply Current vs. Frequency

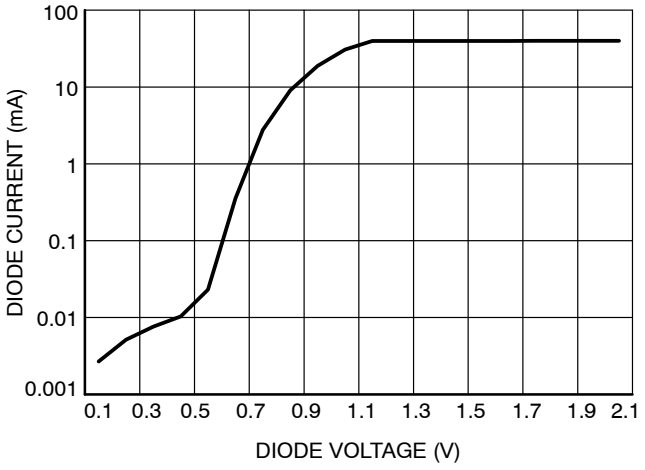


Figure 12. Diode Current vs. Diode Voltage

TYPICAL CHARACTERISTICS

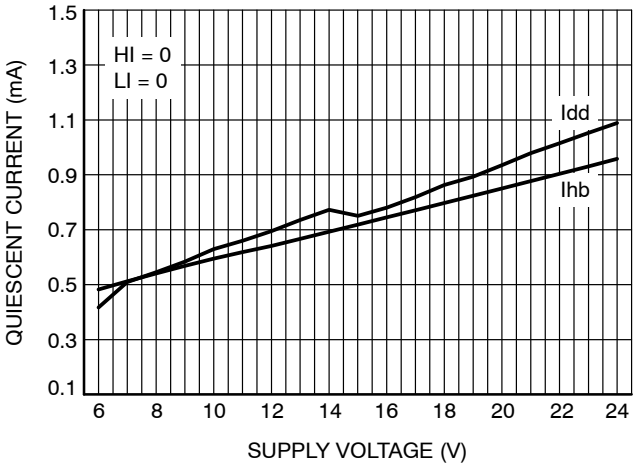


Figure 13. Quiescent Current vs. Supply Voltage

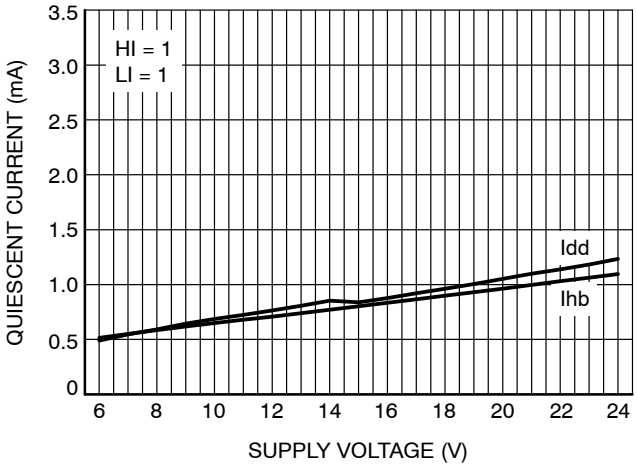


Figure 14. Quiescent Current vs. Supply Voltage

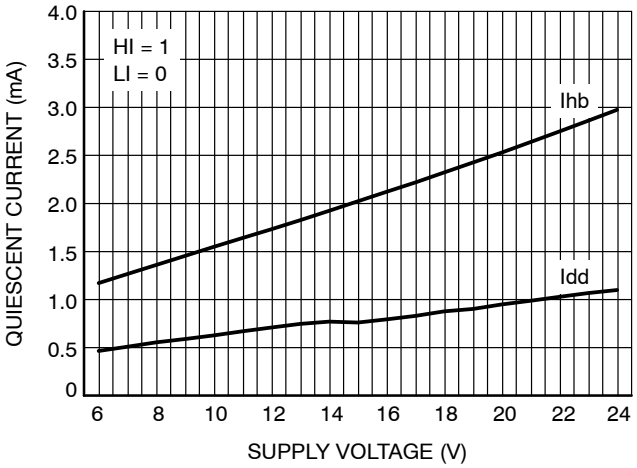


Figure 15. Quiescent Current vs. Supply Voltage

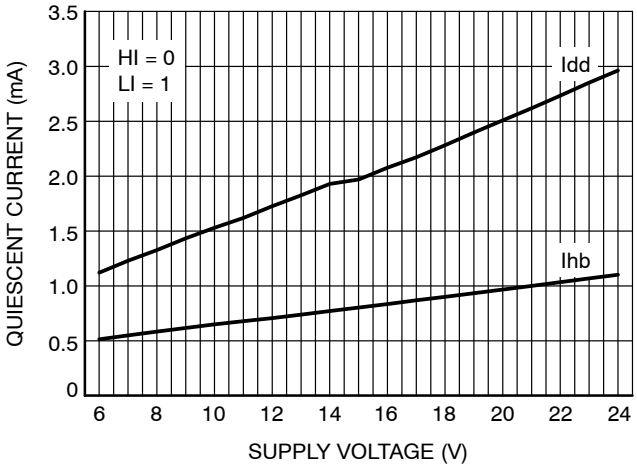


Figure 16. Quiescent Current vs. Supply Voltage

APPLICATION INFORMATION

The NCP81080 is a high performance dual MOSFET gate driver optimized to drive half bridge N−Channel MOSFETs. A high and a Low input signals are all that is required to properly drive the power stage. The input signals are independently controlled and monitored by an anti−cross conduction circuit in order to prevent current shoot through. The NCP81080 has UVLO protections for the high−side and low−side drivers forcing the outputs low if the bias supplies drop below the specified UVLO thresholds. The NCP81080 also features an on−chip high voltage bootstrap diode which reduces the external component count. The NCP81080 has a fixed internal dead−time of 135 ns.

Driver Supply Voltage

As a general rule of thumb the local bypass should be 20 times the bootstrap capacitor. It is recommended to use a 4.7 μF bypass capacitor on VDD to VSS. The bootstrap capacitor is recharged on a cycle by cycle basis through the bootstrap diode from the VDD bypass capacitor. The charging cycle involves bursts in peak currents that require careful considerations by keeping a tight layout and short loops to avoid reliability issues.

If for any reason the application requires the VDD voltage to discharge to ground at rapid rates (3 + V/μs) the user is required to add an external diode between the supply voltage and the bypass capacitor.

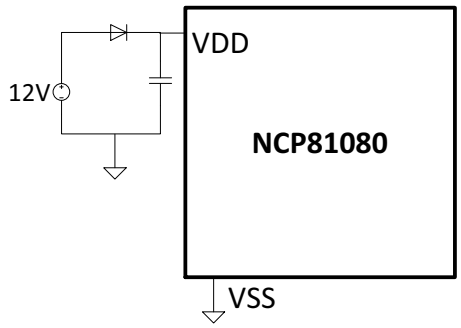


Figure 17. VDD Diode

Low−Side Driver

The low side driver is designed to drive low RDS_{ON} N−channel MOSFETs. The typical output resistances for the driver are 7.5 ohms for sourcing and 3.1 ohms for sinking gate current. The bias to the low side driver is internally connected to the VDD supply and VSS. When the driver is enabled, the driver's output is in phase with LI. When the NCP81080 is disabled, the low side gate is held low.

High−Side Driver

The high side driver is designed to drive a floating low RDS_{ON} N−channel MOSFET. The output resistances for the driver are 7.1 ohms for sourcing and 3.1 ohms for sinking gate current. The bias voltage for the high side driver is realized by an external bootstrap supply circuit which is connected between the HB and HS Pins.

The peak diode current that the part can handle is 8 A. It is required to add an external limiting resistor in series with the bootstrap capacitor to prevent damaging the internal diode.

At power−up, the HS Pin is at ground, the bootstrap capacitor will charge up to VDD through the internal diode. The designer must factor in at least 3 time constants (RC) plus the internal UVLO delays (20 μs typical) before the output can react to a logic input (Refer to Figure 4). If for any reason the voltage across the bootstrap capacitor drops below UVLO, it is required to charge the capacitor back up to VDD while accounting for 3 time constants and the 20 μs UVLO delay before the High−Side channel can react to an HI input.

When the HI pin goes high, the high side driver will begin to turn the high side MOSFET ON by pulling charge out of the bootstrap capacitor. As the external MOSFET turns ON, the HS Pin will rise up to VIN, forcing the HB Pin to VIN + V_{BstCap} which is enough gate to source voltage to hold the switch On. To complete the cycle, the MOSFET is switched OFF by pulling the gate down to the voltage at the HS Pin. When the low side MOSFET turns On, the HS Pin is pulled to ground. This allows the bootstrap capacitor to charge back up to VDD. The high−side driver's output is in phase with the HI input. When the driver is disabled, the high side gate is held low.

Table 6. TYPICAL EXTERNAL CURRENT LIMITING RESISTOR VALUES

VDD (V)	Bootstrap Capacitor (μF)	External Resistor (ohms)
12	0.1	2
12	1	3
18	0.1	3

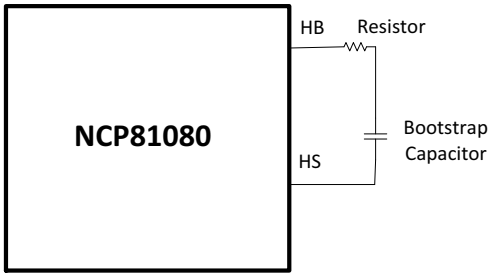


Figure 18. External Current Limiting Resistor

UVLO (Under Voltage Lockout)

The bias supplies of the high−side and low−side drivers have UVLO protection. The VDD UVLO disables both drivers when the VDD voltage crosses the specified threshold. The typical rising threshold is 4.4 V with 0.4 V hysteresis. The VHB UVLO disables only the high−side driver when the VHB to VHS is below the specified

threshold. The typical VHB UVLO rising threshold is 4.4 V with 0.35 V hysteresis.

At power up, when the supply voltage ramps up to set VDD and crosses the UVLO thresholds, **users must take into account a 20 µs delay** before the output drivers can react to a logic input. The 20 µs delay applies to both High−side and Low−side drivers. Figure 4 only shows the delay for the low−side channel.

Input Stage

The input stage of the NCP81080 is TTL compatible. The logic rising threshold level is 2.0 V and the logic falling threshold is 0.8 V.

Cross−Conduction Protection

The NCP81080's inputs HI & LI are controlled independently. In order to prevent the power stage MOSFETs from turning on at the same time an internal logic circuit is implemented to monitor the state of HI & LI. If both input signals are high at the same time, the output signals HO & LO are forced low. (See Timing Diagram)

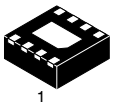
UVLO Crossing

When VDD & VHB cross their respective UVLO thresholds if HI and LI were already set the NCP81080 will keep HO pulled Low until it detects a rising edge on HI, however LO will follow LI allowing the Low−Side FET to turn on. (Refer to Figure 4)

Layout Guidelines

Gate drivers experience high di/dt during the switching transitions. So, the inductance at the gate drive traces must be minimized to avoid excessive ringing on the switch node. Gate drive traces should be kept as short and wide (>20 mil) as practical. The input capacitor must be placed as close as possible to the IC. Connect the VSS pin of the NCP81080 as close as possible to the source of the lower MOSFET. The use of vias is highly desirable to maximize thermal conduction away from driver.

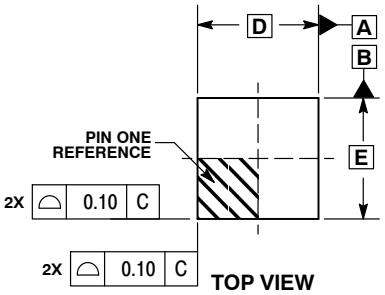
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

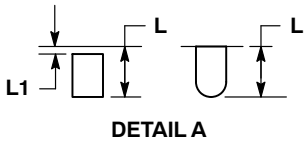


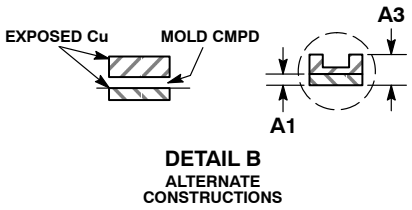
SCALE 4:1

DFN8 2x2, 0.5P
CASE 506AA
ISSUE F

DATE 04 MAY 2016

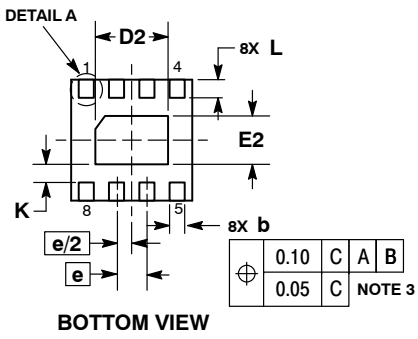




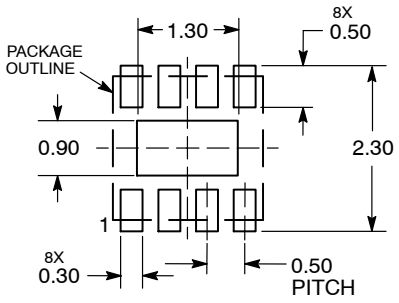


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.30 REF	
L	0.25	0.35
L1	---	0.10



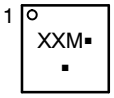
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Device

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

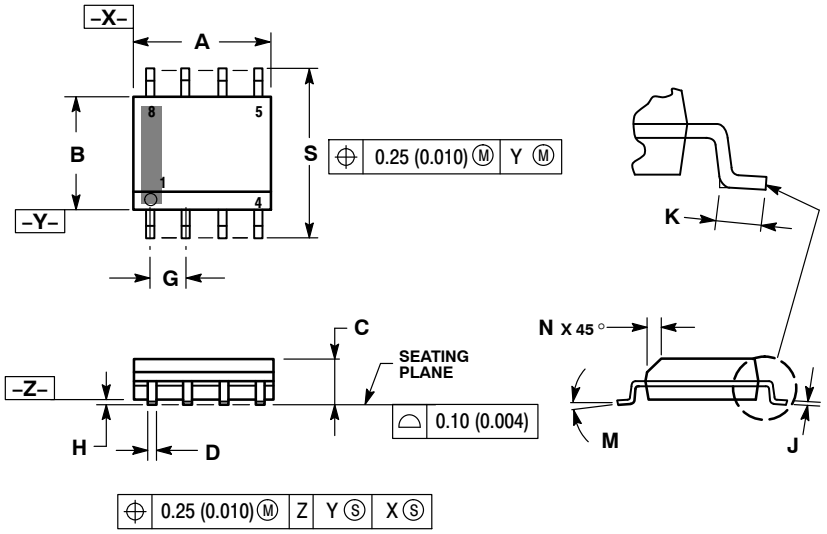
DOCUMENT NUMBER:	**98AON18658D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DFN8, 2.0X2.0, 0.5MM PITCH**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

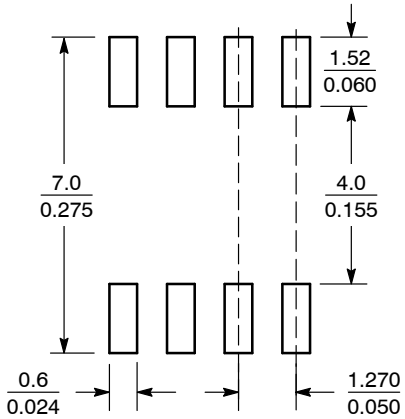
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

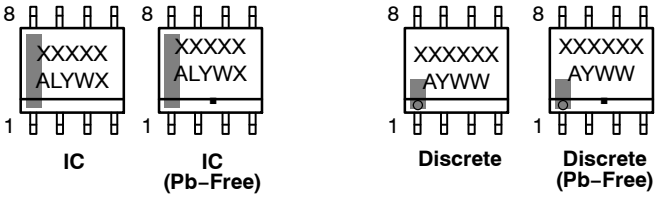
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | **IC (Pb−Free)** | **Discrete** | **Discrete (Pb−Free)**

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

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