19-3707; Rev 3; 11/10

Low-Cost, 308MHz, 315MHz, and 433.92MHz FSK Transceiver with Fractional-N PLL

General Description

The MAX7031 crystal-based, fractional-N transceiver is designed to transmit and receive FSK data at factory-preset carrier frequencies of 308MHz†, 315MHz, or 433.92MHz with data rates up to 33kbps (Manchester encoded) or 66kbps (NRZ encoded). This device generates a typical output power of +10dBm into a 50Ω load, and exhibits typical sensitivity of -110dBm. The MAX7031 features separate transmit and receive pins (PAOUT and LNAIN) and provides an internal RF switch that can be used to connect the transmit and receive pins to a common antenna.

The MAX7031 transmit frequency is generated by a 16-bit, fractional-N, phase-locked loop (PLL), while the receiver's local oscillator (LO) is generated by an integer-N PLL. This hybrid architecture eliminates the need for separate transmit and receive crystal reference oscillators because the fractional-N PLL is preset to be 10.7MHz above the receive LO. Retaining the fixed-N PLL for the receiver avoids the higher current-drain requirements of a fractional-N PLL and keeps the receiver current drain as low as possible.

The fractional-N architecture of the MAX7031 transmit PLL allows the transmit FSK signal to be preset for exact frequency deviations, and completely eliminates the problems associated with oscillator-pulling FSK signal generation. All frequency-generation components are integrated on-chip, and only a crystal, a 10.7MHz IF filter, and a few discrete components are required to implement a complete antenna/digital data solution.

The MAX7031 is available in a small, 5mm x 5mm, 32-pin, thin QFN package, and is specified to operate in the automotive -40°C to +125°C temperature range.

†Consult factory for availability.

Applications

- 2-Way Remote Keyless Entry
- Security Systems
- Home Automation
- Remote Controls
- Remote Sensing
- Smoke Alarms
- Garage-Door Openers
- Local Telemetry Systems

Features

- **+2.1V to +3.6V or +4.5V to +5.5V Single-Supply Operation**
- **Single-Crystal Transceiver**
- **Factory-Preset Frequency (No Serial Interface Required)**
- **FSK Modulation**
- **Factory-Preset FSK Frequency Deviation**
- **+10dBm Output Power into 50Ω Load**
- **Integrated TX/RX Switch**
- **Integrated Transmit and Receive PLL, VCO, and Loop Filter**
- **> 45dB Image Rejection**
- **Typical RF Sensitivity*: -110dBm**
- **Selectable IF Bandwidth with External Filter**
- **RSSI Output with High Dynamic Range**
- **< 12.5mA Transmit-Mode Current**
- **< 6.7mA Receive-Mode Current**
- **< 800nA Shutdown Current**
- **Fast-On Startup Feature, < 250μs**
- **Small, 32-Pin, Thin QFN Package**

**0.2% BER, 4kbps Manchester-encoded data, 280kHz IF BW*

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX7031_ATJ__+	-40°C to +125°C	32 Thin QFN-EP**

+Denotes a lead(Pb)-free/RoHS-compliant package.
***EP = Exposed pad.*
***Note:** The MAX7031 is available with factory-preset operating frequencies. See the Selector Guide for complete part numbers.*

Pin Configuration, Selector Guide, Typical Application Circuit, and Functional Diagram appear at end of data sheet.

Low-Cost, 308MHz, 315MHz, and 433.92MHz FSK Transceiver with Fractional-N PLL

ABSOLUTE MAXIMUM RATINGS

HVIN to GND ....-0.3V to +6.0V
PAVDD, AVDD, DVDD to GND.............................-0.3V to +4.0V
ENABLE, T/R̄, DATA, AGC0, AGC1,
AUTOCAL to GND..............................-0.3V to (V_{HVIN} + 0.3)V
All Other Pins to GND ....-0.3V to ($V_{\_VDD}$ + 0.3)V

Continuous Power Dissipation (T_A = +70°C)
32-Pin Thin QFN (derate 21.3mW/°C
above +70°C)..1702mW
Operating Temperature Range ....-40°C to +125°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, 50Ω system impedance, V_{PAVDD} = V_{AVDD} = V_{DVDD} = V_{HVIN} = +2.1V to +3.6V, f_{RF} = 308MHz, 315MHz, or 433.92MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{PAVDD} = V_{AVDD} = V_{DVDD} = V_{HVIN} = +2.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage (3V Mode)	V_{DD}	HVIN, PAVDD, AVDD, and DVDD connected to power supply		2.1	2.7	3.6	V
Supply Voltage (5V Mode)	V_{HVIN}	PAVDD, AVDD, and DVDD unconnected from HVIN, but connected together		4.5	5.0	5.5	V
Supply Current	I_{DD}	Transmit mode (Note 2)	f_{RF} = 315MHz		11.6	19.1	mA
			f_{RF} = 434MHz		12.4	20.4	
		T_A < +85°C, typ at +25°C (Note 3)	Receiver 315MHz		6.4	8.4	
			Receiver 434MHz		6.7	8.7	
			Deep-sleep (3V mode)		0.8	8.8	µA
			Deep-sleep (5V mode)		2.4	10.9	
		T_A < +125°C, typ at +125°C (Note 2)	Receiver 315MHz		6.8	8.7	mA
			Receiver 434MHz		7.0	8.8	
			Deep-sleep (3V mode)		8.0	34.2	µA
			Deep-sleep (5V mode)		14.9	39.3	
Voltage Regulator	V_{REG}	V_{HVIN} = 5V, I_{LOAD} = 15mA			3.0		V
DIGITAL I/O							
Input-High Threshold	V_{IH}	(Note 2)		0.9 x V_{HVIN}			V
Input-Low Threshold	V_{IL}	(Note 2)				0.1 x V_{HVIN}	V
Pulldown Sink Current		AGC0-1, AUTOCAL, ENABLE, T/R̄, DATA (V_{HVIN} = 5.5V)			20		µA
Output Low Voltage	V_{OL}	I_{SINK} = 500µA			0.15		V
Output High Voltage	V_{OH}	I_{SOURCE} = 500µA			V_{HVIN} - 0.26		V

AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, 50Ω system impedance, V_{PAVDD} = V_{AVDD} = V_{DVDD} = V_{HVIN} = +2.1V to +3.6V, f_{RF} = 308MHz, 315MHz. or 433.92MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{PAVDD} = V_{AVDD} = V_{DVDD} = V_{HVIN} = +2.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Frequency Range					308/315/433.92		MHz
Maximum Input Level	P_{RFIN}				0		dBm
Transmit Efficiency (Note 5)		f_{RF} = 315MHz			32		%
		f_{RF} = 434MHz			30		
Power-On Time	t_{ON}	ENABLE or T/$\overline{R}$ transition low to high, transmitter frequency settled to within 50kHz of the desired carrier			200		µs
		ENABLE or T/$\overline{R}$ transition low to high, transmitter frequency settled to within 5kHz of the desired carrier			350		
		ENABLE transition low to high, or T/$\overline{R}$ transition high to low, receiver startup time (Note 4)			250		
RECEIVER							
Sensitivity		0.2% BER, 4kbps Manchester data rate, 280kHz IF BW, FSK ±50kHz deviation	315MHz		-110		dBm
			434MHz		-107		
Image Rejection					46		dB
POWER AMPLIFIER							
Output Power	P_{OUT}	T_A = +25°C (Note 3)		4.6	10.0	15.5	dBm
		T_A = +125°C, V_{PAVDD} = V_{AVDD} = V_{DVDD} = V_{HVIN} = +2.1V (Note 2)		3.9	6.7		
		T_A = -40°C, V_{PAVDD} = V_{AVDD} = V_{DVDD} = V_{HVIN} = +3.6V (Note 3)			13.1	15.8	
Maximum Carrier Harmonics		With output matching network			-40		dBc
Reference Spur					-50		dBc
PHASE-LOCKED LOOP							
Transmit VCO Gain	K_{VCO}				340		MHz/V
Transmit PLL Phase Noise		10kHz offset, 200kHz loop BW			-68		dBc/Hz
		1MHz offset, 200kHz loop BW			-98		
Receive VCO Gain					340		MHz/V
Receive PLL Phase Noise		10kHz offset, 500kHz loop BW			-80		dBc/Hz
		1MHz offset, 500kHz loop BW			-90		
Loop Bandwidth		Transmit PLL			200		kHz
		Receive PLL			500		

AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, 50Ω system impedance, $V_{PAVDD} = V_{AVDD} = V_{DVDD} = V_{HVIN}$ = +2.1V to +3.6V, f_{RF} = 308MHz, 315MHz. or 433.92MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at $V_{PAVDD} = V_{AVDD} = V_{DVDD} = V_{HVIN}$ = +2.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Frequency Input Level					0.5		V_{P-P}
LOW-NOISE AMPLIFIER/MIXER (Note 7)							
LNA Input Impedance	Z_{INLNA}	Normalized to 50Ω	f_{RF} = 315MHz		1 - j4.7		
			f_{RF} = 434MHz		1 - j3.3		
Voltage-Conversion Gain		High-gain state	f_{RF} = 315MHz		50		dB
			f_{RF} = 434MHz		45		
		Low-gain state	f_{RF} = 315MHz		13		
			f_{RF} = 434MHz		9		
Input-Referred 3rd-Order Intercept Point	IIP3	High-gain state			-42		dBm
		Low-gain state			-6		
Mixer Output Impedance					330		Ω
LO Signal Feedthrough to Antenna					-100		dBm
RSSI							
Input Impedance					330		Ω
Operating Frequency	f_{IF}				10.7		MHz
3dB Bandwidth					10		MHz
Gain					15		mV/dB
FSK DEMODULATOR							
Conversion Gain					2.0		mV/kHz
ANALOG BASEBAND							
Maximum Data Filter Bandwidth					50		kHz
Maximum Data Slicer Bandwidth					100		kHz
Maximum Peak Detector Bandwidth					50		kHz
Maximum Data Rate		Manchester coded			33		kbps
		Nonreturn to zero (NRZ)			66		
CRYSTAL OSCILLATOR							
Crystal Frequency	f_{XTAL}				(f_{RF} - 10.7) / 24		MHz
Frequency Pulling by V_{DD}					2		ppm/V
Crystal Load Capacitance		(Note 6)			4.5		pF

AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, 50Ω system impedance, $V_{PAVDD} = V_{AVDD} = V_{DVDD} = V_{HVIN}$ = +2.1V to +3.6V, f_{RF} = 308MHz, 315MHz. or 433.92MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at $V_{PAVDD} = V_{AVDD} = V_{DVDD} = V_{HVIN}$ = +2.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

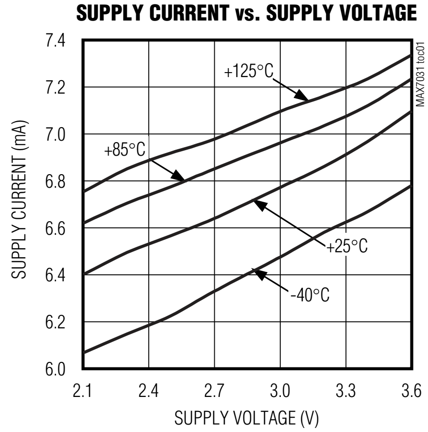
Note 1: Supply current, output power, and efficiency are greatly dependent on board layout and PAOUT match.
Note 2: 100% tested at T_A = +125°C. Guaranteed by design and characterization over temperature.
Note 3: Guaranteed by design and characterization. Not production tested.
Note 4: Time for final signal detection; does not include baseband filter settling.
Note 5: Efficiency = $P_{OUT}/(V_{DD} \times I_{DD})$.
Note 6: Dependent on PCB trace capacitance.
Note 7: Input impedance is measured at the LNAIN pin. Note that the impedance at 315MHz includes the 12nH inductive degeneration from the LNA source to ground. The impedance at 434MHz includes a 10nH inductive degeneration connected from the LNA source to ground. The equivalent input circuit is 50Ω in series with ~2.2pF. The voltage conversion is measured with the LNA input-matching inductor, the degeneration inductor, and the LNA/mixer tank in place, and does not include the IF filter insertion loss.

Typical Operating Characteristics

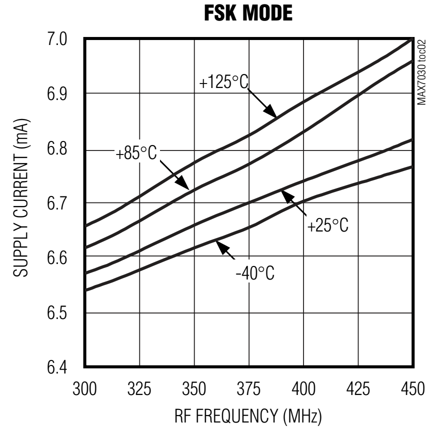
(*Typical Operating Circuit*, $V_{PAVDD} = V_{AVDD} = V_{DVDD} = V_{HVIN}$ = +3.0V, f_{RF} = 433.92MHz, IF BW = 280kHz. 4kbps Manchester encoded, 0.2% BER deviation = ±50kHz, T_A = +25°C, unless otherwise noted.)

RECEIVER

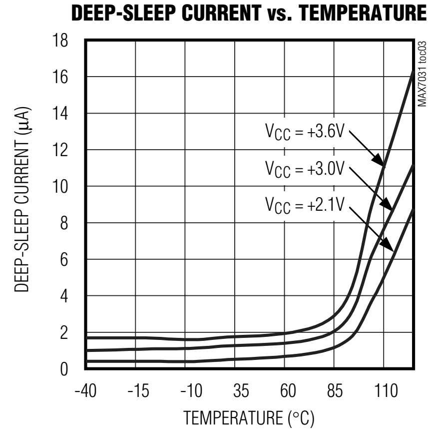
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. RF FREQUENCY FSK MODE



DEEP-SLEEP CURRENT vs. TEMPERATURE



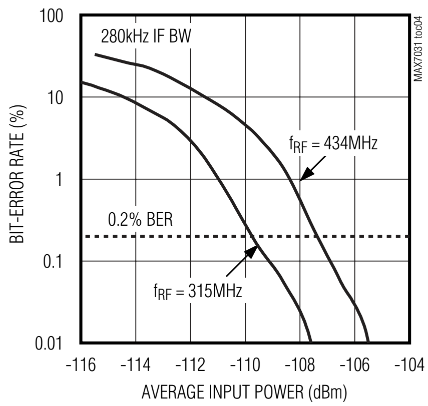
Low-Cost, 308MHz, 315MHz, and 433.92MHz FSK Transceiver with Fractional-N PLL

Typical Operating Characteristics (continued)

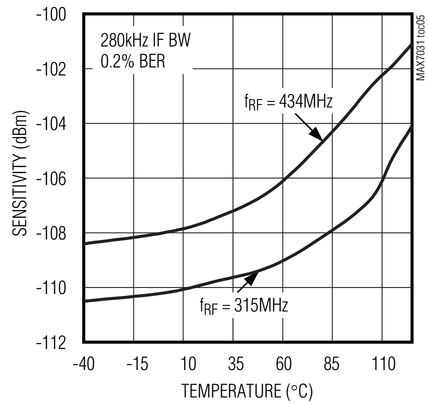
(*Typical Operating Circuit*, V_{PAVDD} = V_{AVDD} = V_{DVDD} = V_{HVIN} = +3.0V, f_{RF} = 433.92MHz, IF BW = 280kHz. 4kbps Manchester encoded, 0.2% BER deviation = ±50kHz, T_A = +25°C, unless otherwise noted.)

RECEIVER

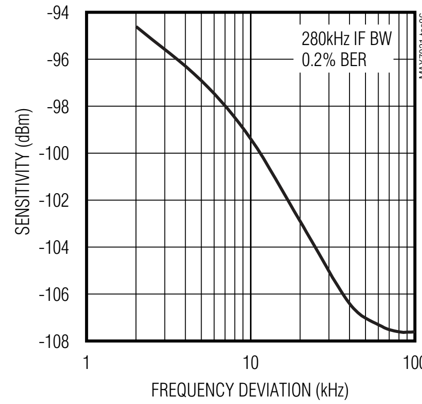
BIT-ERROR RATE vs. AVERAGE INPUT POWER



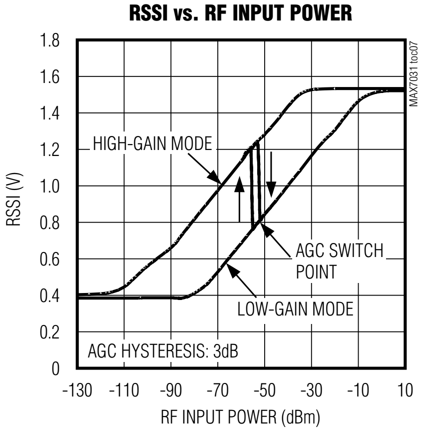
SENSITIVITY vs. TEMPERATURE



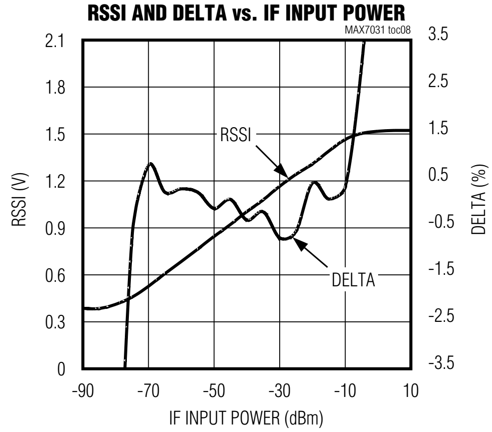
SENSITIVITY vs. FREQUENCY DEVIATION



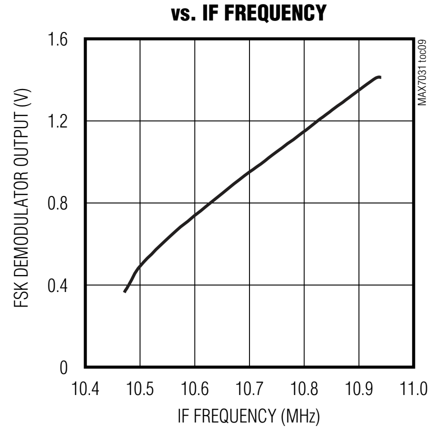
RSSI vs. RF INPUT POWER



RSSI AND DELTA vs. IF INPUT POWER



FSK DEMODULATOR OUTPUT vs. IF FREQUENCY



SYSTEM GAIN vs. IF FREQUENCY

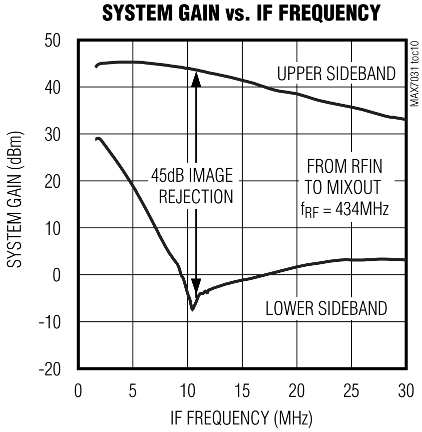
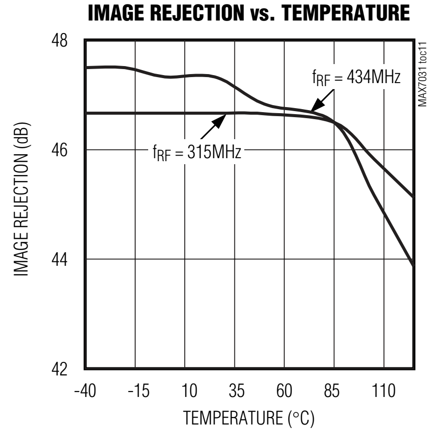
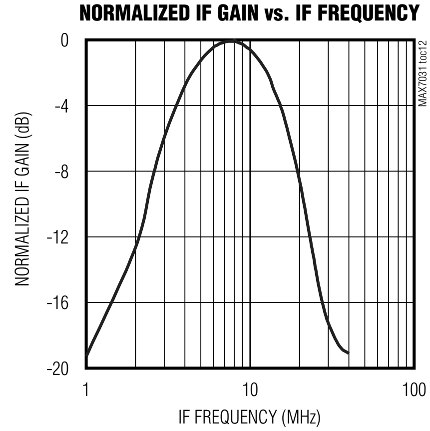


IMAGE REJECTION vs. TEMPERATURE



NORMALIZED IF GAIN vs. IF FREQUENCY

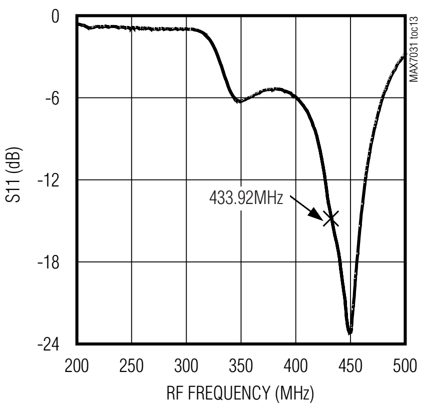


Typical Operating Characteristics (continued)

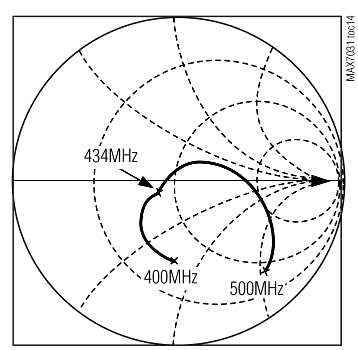
(*Typical Operating Circuit*, $V_{PAVDD} = V_{AVDD} = V_{DVDD} = V_{HVIN} = +3.0V$, $f_{RF} = 433.92MHz$, IF BW = 280kHz. 4kbps Manchester encoded, 0.2% BER deviation = ±50kHz, $T_A = +25°C$, unless otherwise noted.)

RECEIVER

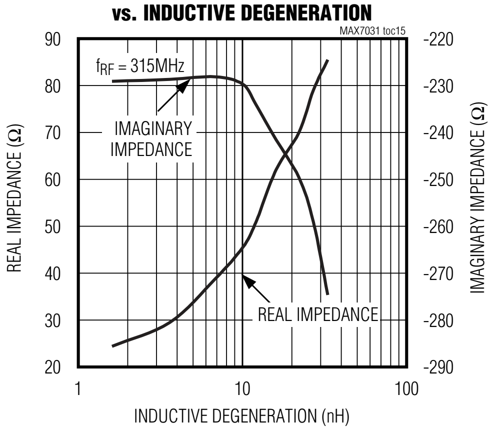
S11 vs. RF FREQUENCY



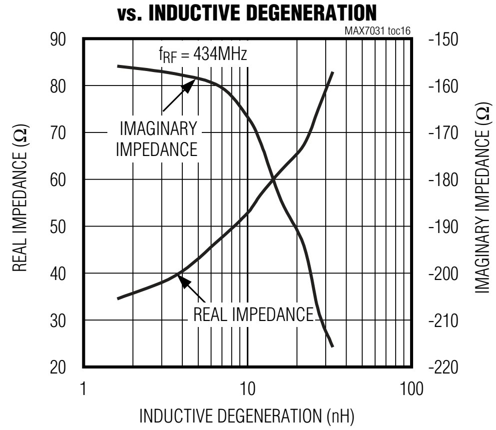
S11 SMITH PLOT OF RFIN



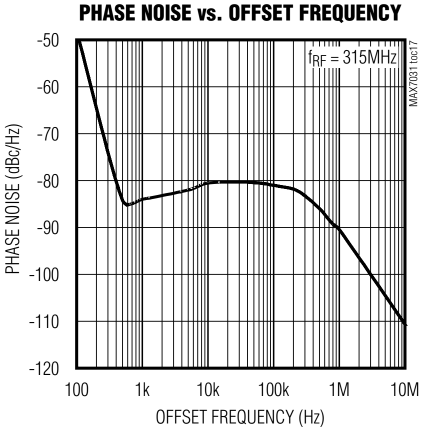
INPUT IMPEDANCE vs. INDUCTIVE DEGENERATION



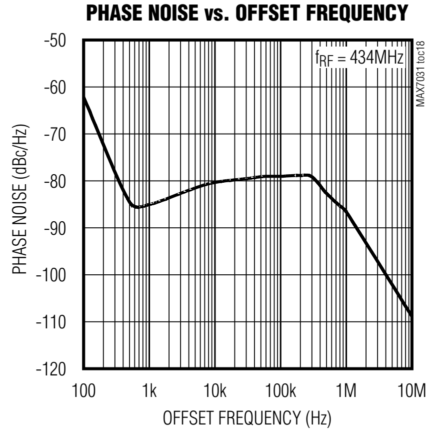
INPUT IMPEDANCE vs. INDUCTIVE DEGENERATION



PHASE NOISE vs. OFFSET FREQUENCY



PHASE NOISE vs. OFFSET FREQUENCY



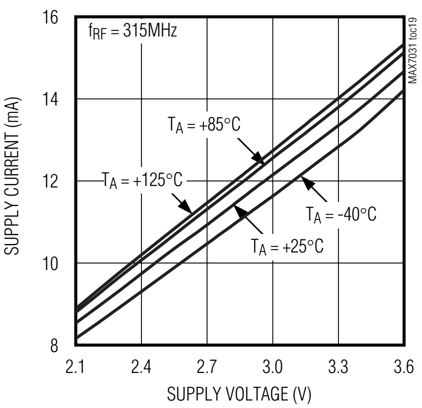
Low-Cost, 308MHz, 315MHz, and 433.92MHz FSK Transceiver with Fractional-N PLL

Typical Operating Characteristics (continued)

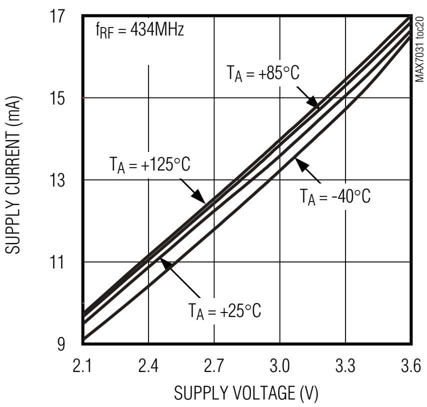
(*Typical Operating Circuit*, $V_{PAVDD} = V_{AVDD} = V_{DVDD} = V_{HVIN} = +3.0V$, $f_{RF} = 433.92MHz$, IF BW = 280kHz. 4kbps Manchester encoded, 0.2% BER deviation = ±50kHz, $T_A = +25°C$, unless otherwise noted.)

TRANSMITTER

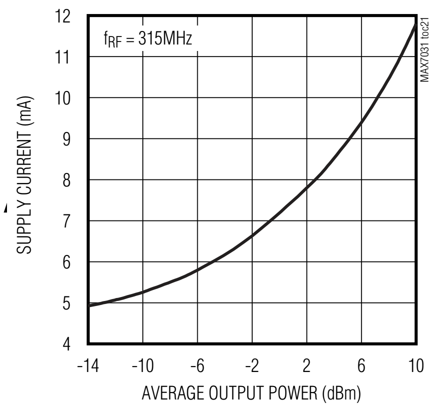
SUPPLY CURRENT vs. SUPPLY VOLTAGE



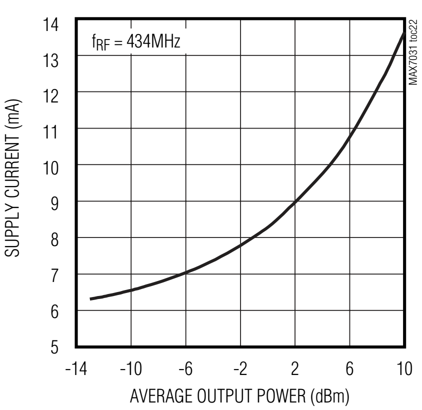
SUPPLY CURRENT vs. SUPPLY VOLTAGE



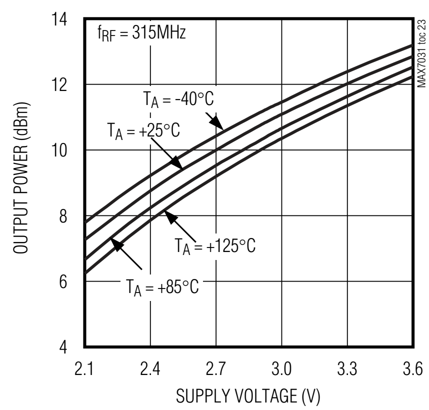
SUPPLY CURRENT vs. OUTPUT POWER



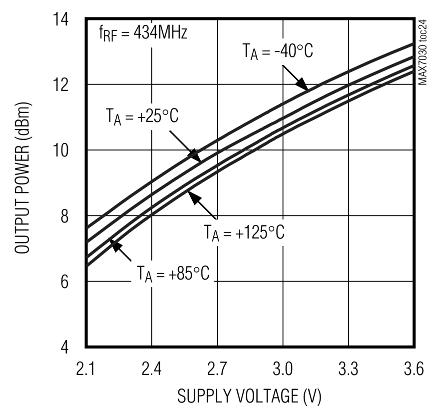
SUPPLY CURRENT vs. OUTPUT POWER



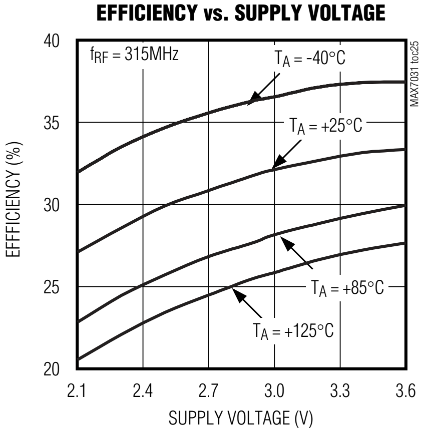
OUTPUT POWER vs. SUPPLY VOLTAGE



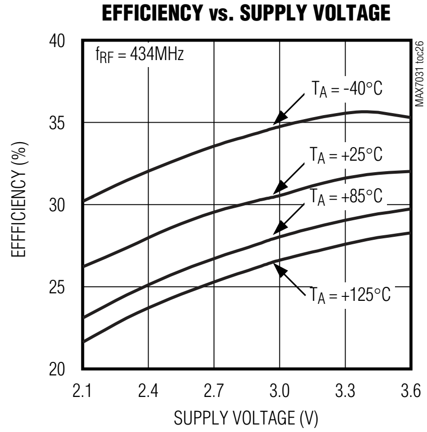
OUTPUT POWER vs. SUPPLY VOLTAGE



EFFICIENCY vs. SUPPLY VOLTAGE



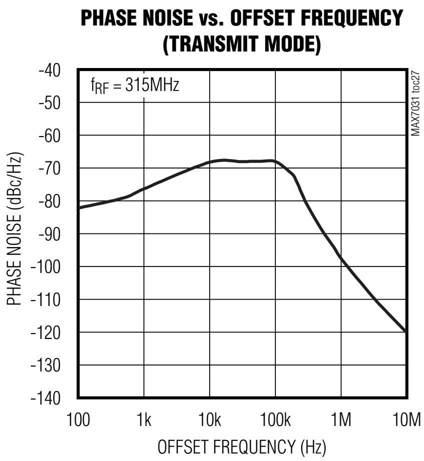
EFFICIENCY vs. SUPPLY VOLTAGE

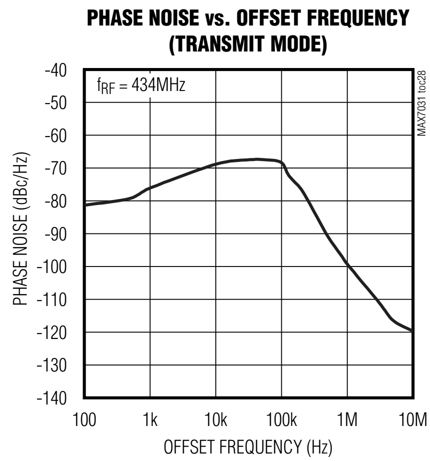


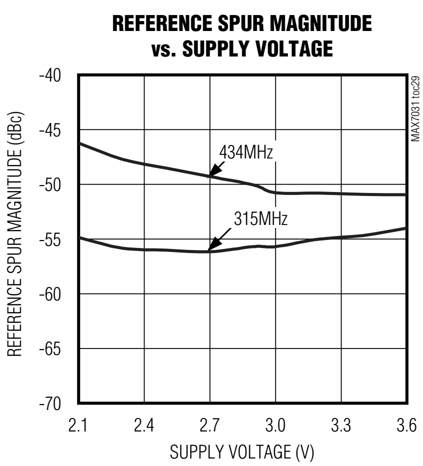
Typical Operating Characteristics (continued)

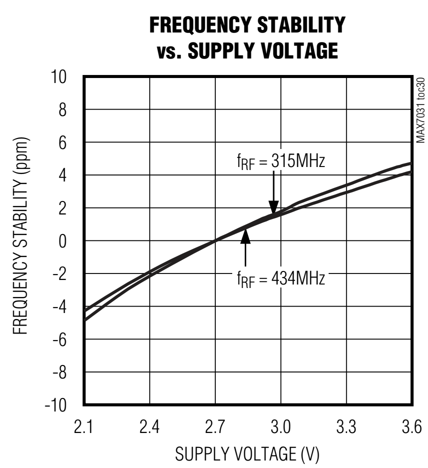
(*Typical Operating Circuit*, $V_{PAVDD} = V_{AVDD} = V_{DVDD} = V_{HVIN}$ = +3.0V, f_{RF} = 433.92MHz, IF BW = 280kHz. 4kbps Manchester encoded, 0.2% BER deviation = ±50kHz, T_A = +25°C, unless otherwise noted.)

TRANSMITTER









Low-Cost, 308MHz, 315MHz, and 433.92MHz FSK Transceiver with Fractional-N PLL

Pin Description

PIN	NAME	FUNCTION
1	PAVDD	Power-Amplifier Supply Voltage. Bypass to GND with 0.01µF and 220pF capacitors placed as close as possible to the pin.
2	ROUT	Envelope-Shaping Output. ROUT controls the power-amplifier envelope's rise and fall times. Connect ROUT to the PA pullup inductor or optional power-adjust resistor. Bypass the inductor to GND as close as possible to the inductor with 680pF and 220pF capacitors as shown in the *Typical Application Circuit*.
3	TX/RX1	Transmit/Receive Switch Throw. Drive T/$\overline{R}$ high to short TX/RX1 to TX/RX2. Drive T/$\overline{R}$ low to disconnect TX/RX1 from TX/RX2. Functionally identical to TX/RX2.
4	TX/RX2	Transmit/Receive Switch Pole. Typically connected to ground. See the *Typical Application Circuit*.
5	PAOUT	Power-Amplifier Output. Requires a pullup inductor to the supply voltage (or ROUT if envelope shaping is desired), which can be part of the output-matching network to an antenna.
6	AVDD	Analog Power-Supply Voltage. AVDD is connected to an on-chip +3.0V regulator in 5V operation. Bypass AVDD to GND with a 0.1µF and 220pF capacitor placed as close as possible to the pin.
7	LNAIN	Low-Noise Amplifier Input. Must be AC-coupled.
8	LNASRC	Low-Noise Amplifier Source for External Inductive Degeneration. Connect an inductor to GND to set the LNA input impedance.
9	LNAOUT	Low-Noise Amplifier Output. Must be connected to AVDD through a parallel LC tank filter. AC-couple to MIXIN+.
10	MIXIN+	Noninverting Mixer Input. Must be AC-coupled to the LNA output.
11	MIXIN-	Inverting Mixer Input. Bypass to AVDD with a capacitor as close as possible to the LNA LC tank filter.
12	MIXOUT	330Ω Mixer Output. Connect to the input of the 10.7MHz filter.
13	IFIN-	Inverting 330Ω IF Limiter Amplifier Input. Bypass to GND with a capacitor.
14	IFIN+	Noninverting 330Ω IF Limiter Amplifier Input. Connect to the output of the 10.7MHz IF filter.
15	PDMIN	Minimum-Level Peak Detector for Demodulator Output
16	PDMAX	Maximum-Level Peak Detector for Demodulator Output
17	DS-	Inverting Data Slicer Input
18	DS+	Noninverting Data Slicer Input
19	OP+	Noninverting Op-Amp Input for the Sallen-Key Data Filter
20	DF	Data-Filter Feedback Node. Input for the feedback capacitor of the Sallen-Key data filter.
21	RSSI	Buffered Received-Signal-Strength-Indicator Output
22	T/$\overline{R}$	Transmit/$\overline{\text{Receive}}$. Drive high to put the device in transmit mode. Drive low or leave unconnected to put the device in receive mode. It is internally pulled down.
23	ENABLE	Enable. Drive high for normal operation. Drive low or leave unconnected to put the device into shutdown mode.
24	DATA	Receiver Data Output/Transmitter Data Input
25	N.C.	No Connection. Do not connect to this pin.
26	DVDD	Digital Power-Supply Voltage. Bypass to GND with a 0.01µF and 220pF capacitor placed as close as possible to the pin.
27	HVIN	High-Voltage Supply Input. For 3V operation, connect HVIN to AVDD, PAVDD, and DVDD. For 5V operation, connect only HVIN to 5V. Bypass HVIN to GND with a 0.01µF and 220pF capacitor placed as close as possible to the pin.

Pin Description (continued)

PIN	NAME	FUNCTION
28	AUTOCAL	Enable (Logic-High) to Allow FSK Demodulator Calibration. Bypass to GND with a 10pF capacitor.
29	AGC1	AGC Enable/Dwell Time Control 1. See Table 1. Bypass to GND with a 10pF capacitor.
30	AGC0	AGC Enable/Dwell Time Control 0 (LSB). See Table 1. Bypass to GND with a 10pF capacitor.
31	XTAL1	Crystal Input 1. Bypass to GND if XTAL2 is driven by an AC-coupled external reference.
32	XTAL2	Crystal Input 2. XTAL2 can be driven from an external AC-coupled reference.
—	EP	Exposed Pad. Solder evenly to the board's ground plane for proper operation.

Detailed Description

The MAX7031 308MHz, 315MHz, and 433.92MHz CMOS transceiver and a few external components provide a complete transmit and receive chain from the antenna to the digital data interface. This device is designed for transmitting and receiving FSK data. All transmit frequencies are generated by a fractional-N-based synthesizer, allowing for very fine frequency steps in increments of $f_{XTAL}/4096$. The receive local oscillator (LO) is generated by a traditional integer-N-based synthesizer. Depending on component selection, data rates as high as 33kbps (Manchester encoded) or 66kbps (NRZ encoded) can be achieved.

Receiver

Low-Noise Amplifier (LNA)

The LNA is a cascode amplifier with off-chip inductive degeneration that achieves approximately 30dB of voltage gain that is dependent on both the antenna-matching network at the LNA input, and the LC tank network between the LNA output and the mixer inputs.

The off-chip inductive degeneration is achieved by connecting an inductor from LNASRC to AGND. This inductor sets the real part of the input impedances at LNAIN, allowing for a more flexible match for low-input impedances such as a PCB trace antenna. A nominal value for this inductor with a 50Ω input impedance is 12nH at 315MHz and 10nH at 434MHz, but the inductance is affected by PCB trace length. LNASRC can be shorted to ground to increase sensitivity by approximately 1dB, but the input match must then be reoptimized.

The LC tank filter connected to LNAOUT consists of L5 and C9 (see the *Typical Application Circuit*). Select L5 and C9 to resonate at the desired RF input frequency. The resonant frequency is given by:

$$f = \frac{1}{2\pi\sqrt{L_{TOTAL} \times C_{TOTAL}}}$$

where $L_{TOTAL} = L5 + L_{PARASITICS}$ and $C_{TOTAL} = C9 + C_{PARASITICS}$.

$L_{PARASITICS}$ and $C_{PARASITICS}$ include inductance and capacitance of the PCB traces, package pins, mixer input impedance, LNA output impedance, etc. These parasitics at high frequencies cannot be ignored, and can have a dramatic effect on the tank filter center frequency. Lab experimentation should be done to optimize the center frequency of the tank. The parasitic capacitance is generally 5pF to 7pF.

Automatic Gain Control (AGC)

When the AGC is enabled, it monitors the RSSI output. When the RSSI output reaches 1.28V, which corresponds to an RF input level of approximately -55dBm, the AGC switches on the LNA gain-reduction attenuator. The attenuator reduces the LNA gain by 36dB, thereby reducing the RSSI output by about 540mV to 740mV. The LNA resumes high-gain mode when the RSSI output level drops back below 680mV (approximately -59dBm at the RF input) for a programmable interval called the AGC dwell time (see Table 1). The AGC has a hysteresis of approximately 4dB. With the AGC function, the RSSI dynamic range is increased. AGC is not necessary for most FSK applications.

AGC Dwell Time Settings

The AGC dwell timer holds the AGC in a low-gain state for a set amount of time after the power level drops below the AGC switching threshold. After that set amount of time, if the power level is still below the AGC threshold, the LNA goes into high-gain state.

Table 1. AGC Dwell Time Settings for MAX7031

AGC1	AGC0	DESCRIPTION
0	0	AGC disabled, high gain selected
0	1	K = 11, short dwell time
1	0	K = 14, medium dwell time
1	1	K = 20, long dwell time

The MAX7031 uses the two AGC control pins (AGC0 and AGC1) to enable or disable the AGC and set three user-controlled dwell timer settings. The AGC dwell time is dependent on the crystal frequency and the bit settings of the AGC control pins. To calculate the dwell time, use the following equation:

$$\text{Dwell Time} = \frac{2^K}{f_{XTAL}}$$

where K is an integer in decimal, determined by the control pin settings shown in Table 1.

For example, a receiver operating at 315MHz has a crystal oscillator frequency of 12.679MHz. For K = 11 (AGC setting = 0, 1), the dwell timer is 162µs; for K = 14 (AGC setting = 1, 0), the dwell timer is 1.3ms; for K = 20 (AGC setting = 1, 1), the dwell time is 83ms.

Mixer

A unique feature of the MAX7031 is the integrated image rejection of the mixer. This eliminates the need for a costly front-end SAW filter for many applications. The advantage of not using a SAW filter is increased sensitivity, simplified antenna matching, less board space, and lower cost.

The mixer cell is a pair of double-balanced mixers that perform an IQ downconversion of the RF input to the 10.7MHz intermediate frequency (IF) with low-side injection (i.e., $f_{LO} = f_{RF} - f_{IF}$). The image-rejection circuit then combines these signals to achieve a typical 46dB of image rejection over the full temperature range. Low-side injection is required as high-side injection is not possible due to the on-chip image rejection. The IF output is driven by a source follower, biased to create a driving impedance of 330Ω to interface with an off-chip 330Ω ceramic IF filter. The voltage conversion gain driving a 330Ω load is approximately 20dB. Note that the MIXIN+ and MIXIN- inputs are functionally identical.

Integer-N, Phase-Locked Loop (PLL)

The MAX7031 utilizes a fixed integer-N PLL to generate the receive LO. All PLL components, including the loop filter, voltage-controlled oscillator, charge pump, asynchronous 24x divider, and phase-frequency detector are internal. The loop bandwidth is approximately 500kHz. The relationship between RF, IF, and reference frequencies is given by:

$$f_{REF} = (f_{RF} - f_{IF})/24$$

Intermediate Frequency (IF)

The IF section presents a differential 330Ω load to provide matching for the off-chip ceramic filter. The internal six AC-coupled limiting amplifiers produce an overall gain of approximately 65dB, with a bandpass filter-type response centered near the 10.7MHz IF frequency with a 3dB bandwidth of approximately 10MHz. The RSSI circuit demodulates the IF to baseband by producing a DC output proportional to the log of the IF signal level with a slope of approximately 15mV/dB.

FSK Demodulator

The FSK demodulator uses an integrated 10.7MHz PLL that tracks the input RF modulation and converts the frequency deviation into a voltage difference. The PLL is illustrated in Figure 1. The input to the PLL comes from the output of the IF limiting amplifiers. The PLL control voltage responds to changes in the frequency of the input signal with a nominal gain of 2.0mV/kHz. For example, an FSK peak-to-peak deviation of 50kHz

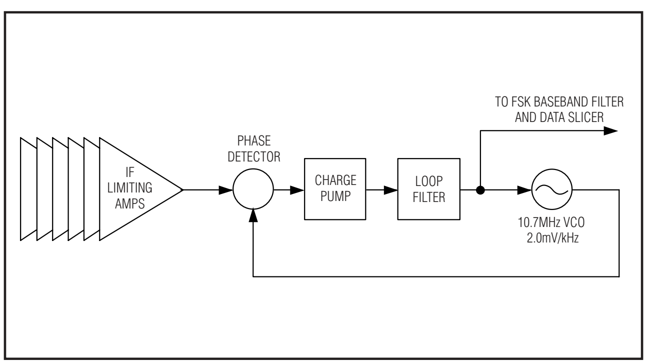


Figure 1. FSK Demodulator PLL Block Diagram

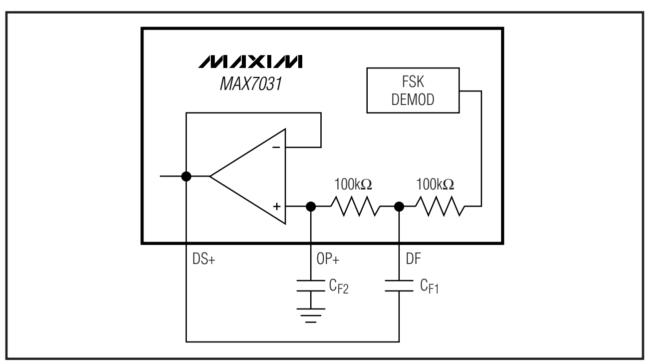


Figure 2. Sallen-Key Lowpass Data Filter

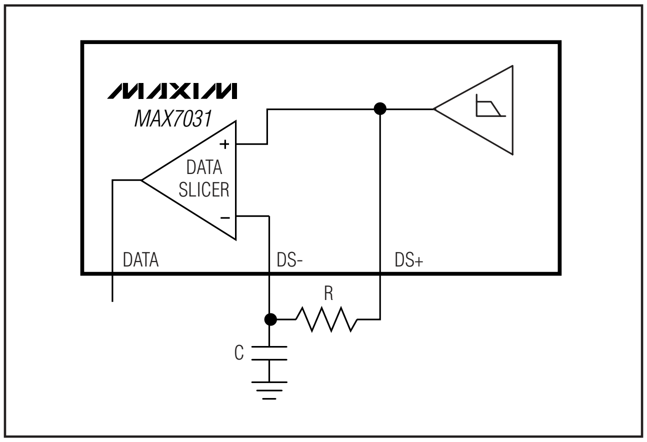


Figure 3. Generating Data Slicer Threshold Using a Lowpass Filter

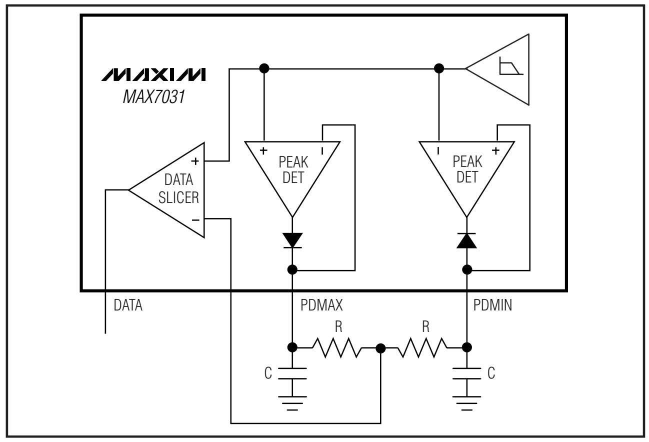


Figure 4. Generating Data Slicer Threshold Using the Peak Detectors

generates a 100mV$_{P-P}$ signal on the control line. This control voltage is then filtered and sliced by the baseband circuitry.

The FSK demodulator PLL requires calibration to overcome variations in process, voltage, and temperature. This is done by cycling the ENABLE pin when the AUTOCAL pin is a logic 1. If the AUTOCAL pin is a logic 0, calibration cannot occur.

Data Filter

The data filter for the demodulated data is implemented as a 2nd-order, lowpass Sallen-Key filter. The pole locations are set by the combination of two on-chip resistors and two external capacitors. Adjusting the value of the external capacitors changes the corner frequency to optimize for different data rates. Set the corner frequency in kHz to approximately 2 times the fastest expected Manchester data rate in kbps from the transmitter (1.0 times the fastest expected NRZ data rate). Keeping the corner frequency near the data rate rejects any noise at higher frequencies, resulting in an increase in receiver sensitivity.

The configuration shown in Figure 2 can create a Butterworth or Bessel response. The Butterworth filter offers a very-flat-amplitude response in the passband and a rolloff rate of 40dB/decade for the two-pole filter. The Bessel filter has a linear phase response, which works well for filtering digital data. To calculate the value of the capacitors, use the following equations, along with the coefficients in Table 2:

$$C_{F1} = \frac{b}{a(100k\Omega)(\pi)(f_C)}$$

$$C_{F2} = \frac{a}{4(100k\Omega)(\pi)(f_C)}$$

where f_C is the desired 3dB corner frequency.

For example, choose a Butterworth filter response with a corner frequency of 5kHz:

$$C_{F1} = \frac{1.000}{(1.414)(100k\Omega)(3.14)(5kHz)} \approx 450pF$$

$$C_{F2} = \frac{1.414}{(4)(100k\Omega)(3.14)(5kHz)} \approx 225pF$$

Choosing standard capacitor values changes C_{F1} to 470pF and C_{F2} to 220pF. In the *Typical Application Circuit*, C_{F1} and C_{F2} are named C16 and C17, respectively.

Table 2. Coefficients to Calculate C_{F1} and C_{F2}

FILTER TYPE	a	b
Butterworth (Q = 0.707)	1.414	1.000
Bessel (Q = 0.577)	1.3617	0.618

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Data Slicer

The data slicer takes the analog output of the data filter and converts it to a digital signal. This is achieved by using a comparator and comparing the analog input to a threshold voltage. The threshold voltage is set by the voltage on the DS- pin, which is connected to the negative input of the data-slicer comparator.

Numerous configurations can be used to generate the data-slicer threshold. For example, the circuit in Figure 3 shows a simple method using only one resistor and one capacitor. This configuration averages the analog output of the filter and sets the threshold to approximately 50% of that amplitude. With this configuration, the threshold automatically adjusts as the analog signal varies, minimizing the possibility for errors in the digital data. The values of R and C affect how fast the threshold tracks the analog amplitude. Be sure to keep the corner frequency of the RC circuit much lower (about 10 times) than the lowest expected data rate.

With this configuration, a long string of NRZ zeros or ones can cause the threshold to drift. This configuration works best if a coding scheme, such as Manchester coding, which has an equal number of zeros and ones, is used.

Figure 4 shows a configuration that uses the positive and negative peak detectors to generate the threshold. This configuration sets the threshold to the midpoint between a high output and a low output of the data filter.

Peak Detectors

The maximum peak detector (PDMAX) and minimum peak detector (PDMIN), with resistors and capacitors shown in Figure 4, create DC output voltages equal to the high- and low-peak values of the filtered demodulated signal. The resistors provide a path for the capacitors to discharge, allowing the peak detectors to dynamically follow peak changes of the data filter output voltages.

The maximum and minimum peak detectors can be used together to form a data slicer threshold voltage at a value midway between the maximum and minimum voltage levels of the data stream (see the *Data Slicer* section and Figure 4). Set the RC time constant of the peak-detector combining network to at least 5 times the data period.

If there is an event that causes a significant change in the magnitude of the baseband signal, such as an AGC gain switch or a power-up transient, the peak detectors may “catch” a false level. If a false peak is detected, the slicing level is incorrect. The MAX7031 peak detectors correct these problems by temporarily tracking the incoming baseband filter voltage when an AGC state switch occurs, or by forcing the peak detectors to track the baseband filter output voltage until all internal circuits are stable following an enable pin low-to-high transition. The peak detectors exhibit a fast attack/slow decay response. This feature allows for an extremely fast startup or AGC recovery.

Transmitter

Power Amplifier (PA)

The PA of the MAX7031 is a high-efficiency, open-drain, switch-mode amplifier. The PA with proper output- matching network can drive a wide range of antenna impedances, which includes a small-loop PCB trace and a 50Ω antenna. The output-matching network for a 50Ω antenna is shown in the *Typical Application Circuit*. The output-matching network suppresses the carrier harmonics and transforms the antenna impedance to an optimal impedance at PAOUT (pin 5). The optimal impedance at PAOUT is 250Ω.

When the output-matching network is properly tuned, the PA transmits power with a high overall efficiency of up to 32%. The efficiency of the PA itself is more than 46%. The output power is set by an external resistor at PAOUT, and is also dependent on the external antenna and antenna-matching network at the PA output.

Envelope Shaping

The MAX7031 features an internal envelope-shaping resistor, which connects between the open-drain output of the PA and the power supply. The envelope-shaping resistor slows the turn-on/turn-off of the PA. Envelope shaping is not necessary for FSK. For most applications, the PA pullup inductor should be connected to PAVDD instead of ROUT.

Fractional-N Phase-Locked Loop (PLL)

The MAX7031 utilizes a fully integrated, fractional-N PLL for its transmit frequency synthesizer. All PLL components, including the loop filter, are integrated internally. The loop bandwidth is approximately 200kHz.

Power-Supply Connections

The MAX7031 can be powered from a 2.1V to 3.6V supply or a 4.5V to 5.5V supply. If a 4.5V to 5.5V supply is used, then the on-chip linear regulator reduces the 5V supply to the 3V needed to operate the chip.

To operate the MAX7031 from a 3V supply, connect PAVDD, AVDD, DVDD, and HVIN to the 3V supply. When using a 5V supply, connect the supply to HVIN only and connect AVDD, PAVDD, and DVDD together. In both cases, bypass PAVDD, DVDD, and HVIN to GND with a 0.01μF and 220pF capacitor and bypass AVDD to GND with a 0.1μF and 220pF capacitor.

Bypass T/$\overline{R}$, ENABLE, DATA, AGC0-1, and AUTOCAL with 10pF capacitors to GND. Place all bypass capacitors as close to the respective pins as possible.

Transmit/Receive Antenna Switch

The MAX7031 features an internal SPST RF switch that, when combined with a few external components, allows the transmit and receive pins to share a common antenna (see the *Typical Application Circuit)*. In receive mode, the switch is open and the power amplifier is shut down, presenting a high impedance to minimize the loading of the LNA. In transmit mode, the switch closes to complete a resonant tank circuit at the PA output and forms an RF short at the input to the LNA. In this mode, the external passive components couple the output of the PA to the antenna to protect the LNA input from strong transmitted signals.

The switch state is controlled by the T/$\overline{R}$ pin (pin 22). Drive T/$\overline{R}$ high to put the device in transmit mode; drive T/$\overline{R}$ low to put the device in receive mode.

Crystal Oscillator (XTAL)

The XTAL oscillator in the MAX7031 is designed to present a capacitance of approximately 3pF between the XTAL1 and XTAL2 pins. In most cases, this corresponds to a 4.5pF load capacitance applied to the external crystal when typical PCB parasitics are added. **It is very important to use a crystal with a load capacitance that is equal to the capacitance of the MAX7031 crystal oscillator plus PCB parasitics.** If a crystal designed to oscillate with a different load capacitance is used, the crystal is pulled away from its stated operating frequency, introducing an error in the reference frequency. Crystals designed to operate with higher differential load capacitance always pull the reference frequency higher.

In actuality, the oscillator pulls every crystal. The crystal's natural frequency is really below its specified frequency, but when loaded with the specified load capacitance, the crystal is pulled and oscillates at its specified frequency. This pulling is already accounted for in the specification of the load capacitance.

Additional pulling can be calculated if the electrical parameters of the crystal are known. The frequency pulling is given by:

$$f_P = \frac{C_m}{2}\left(\frac{1}{C_{CASE} + C_{LOAD}} - \frac{1}{C_{CASE} + C_{SPEC}}\right) \times 10^6$$

where:

f_P is the amount the crystal frequency is pulled in ppm.

Cm is the motional capacitance of the crystal.

C_{CASE} is the case capacitance.

C_{SPEC} is the specified load capacitance.

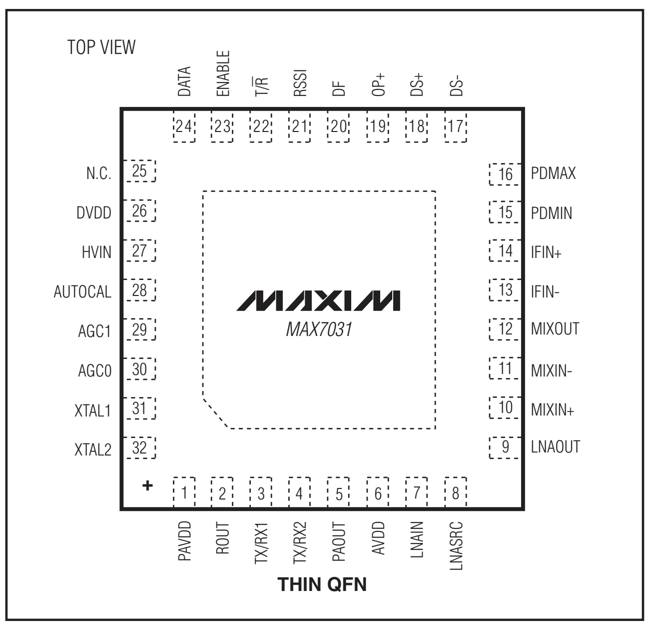
C_{LOAD} is the actual load capacitance.

When the crystal is loaded as specified, i.e., $C_{LOAD} = C_{SPEC}$, the frequency pulling equals zero.

Chip Information

PROCESS: CMOS

Pin Configuration



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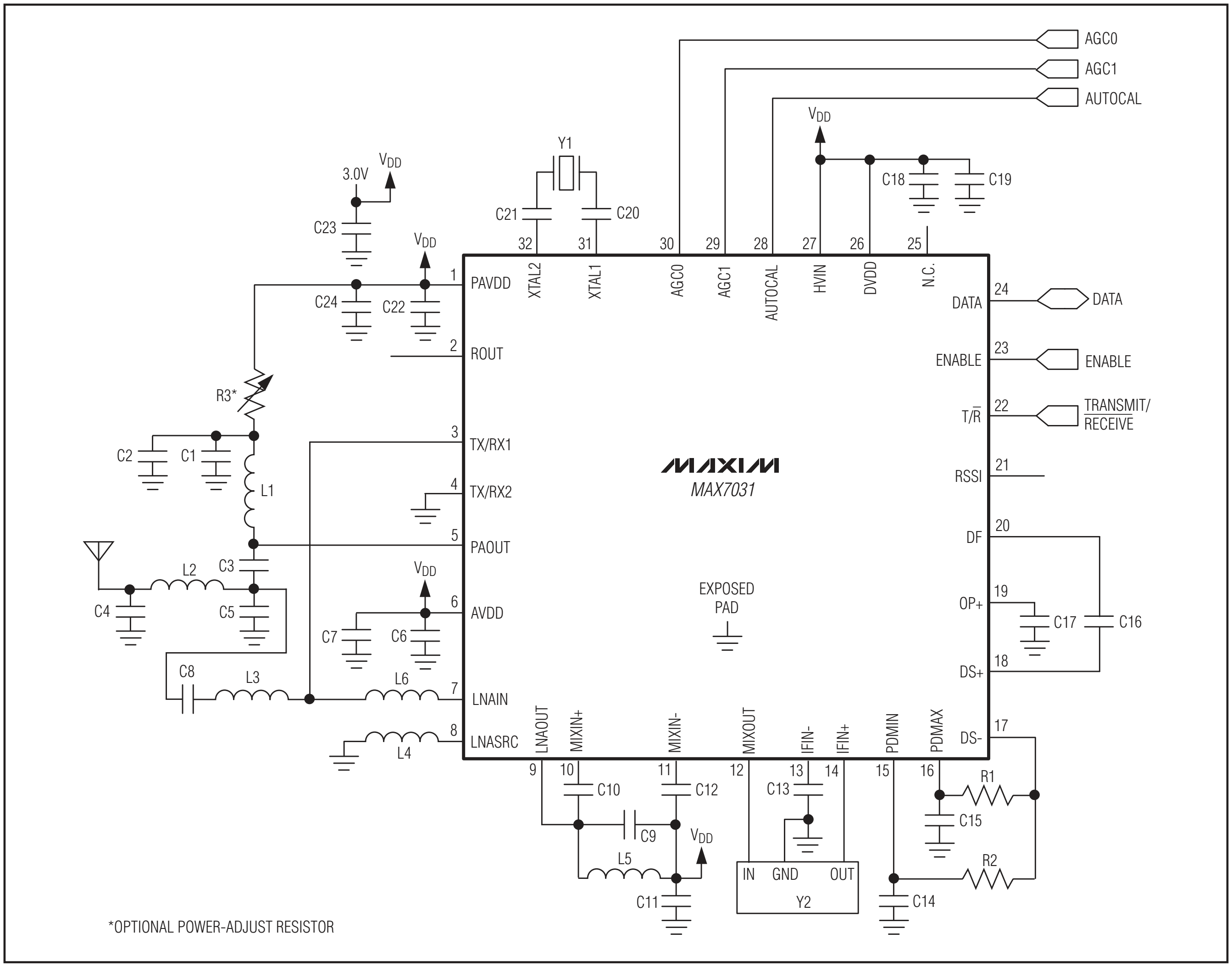
Typical Application Circuit



Selector Guide

PART	CARRIER FREQUENCY (MHz)	FSK DEVIATION FREQUENCY (kHz)
MAX7031LATJ+†	308	±51.413
MAX7031MATJ15+	315	±15.477
MAX7031MATJ50+	315	±49.528
MAX7031HATJ17+	433.92	±17.221
MAX7031HATJ51+	433.92	±51.663

+Denotes a lead(Pb)-free/RoHS-compliant package.

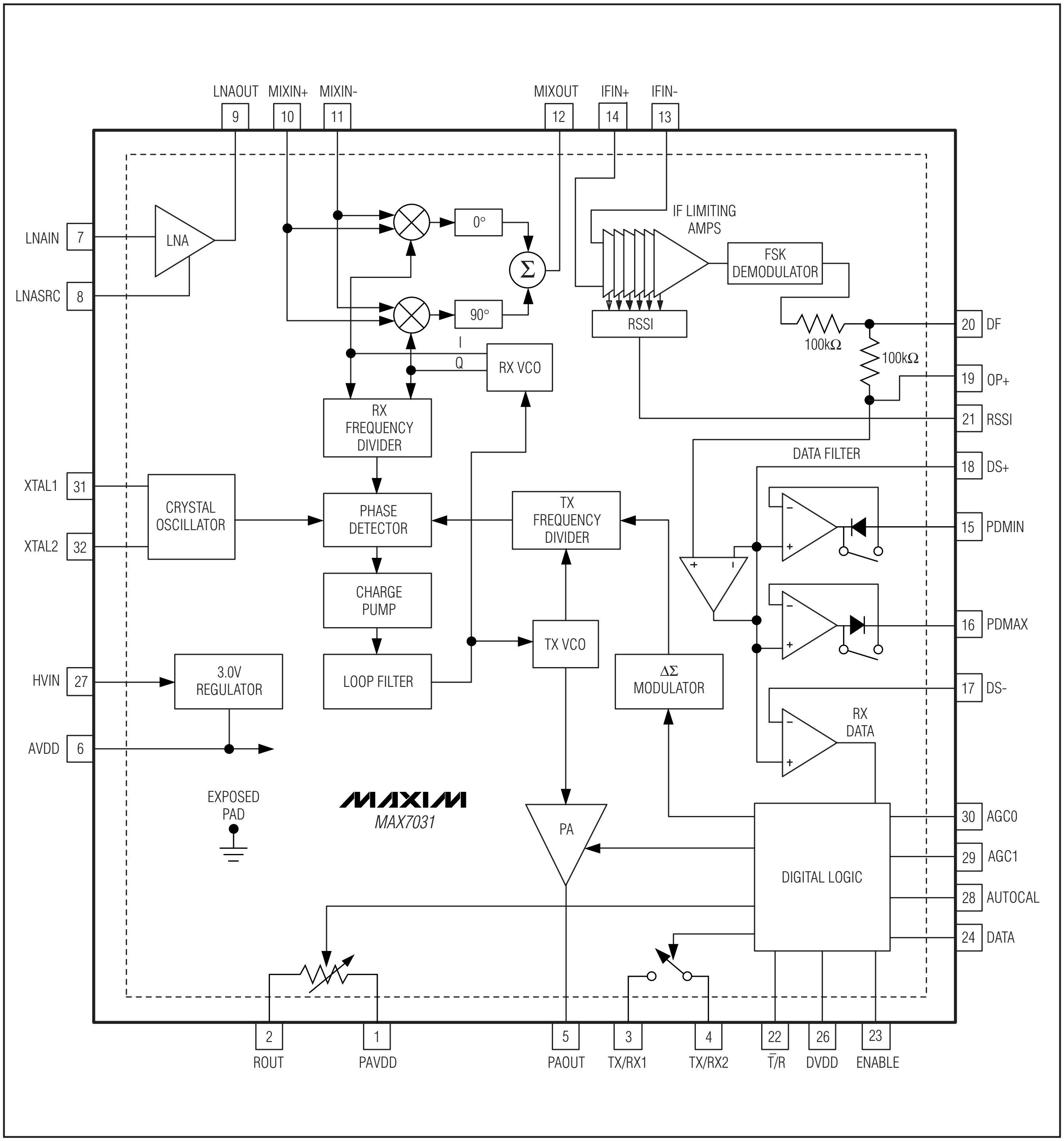
†Contact factory for availability.

Table 3. Component Values for Typical Application Circuit

COMPONENT	VALUE FOR 433.92MHz RF	VALUE FOR 315MHz RF	DESCRIPTION
C1	220pF	220pF	10%
C2	680pF	680pF	10%
C3	6.8pF	12pF	5%
C4	6.8pF	10pF	5%
C5	10pF	22pF	5%
C6	220pF	220pF	10%
C7	0.1µF	0.1µF	10%
C8	100pF	100pF	5%
C9	1.8pF	2.7pF	±0.1pF
C10	100pF	100pF	5%
C11	220pF	220pF	10%
C12	100pF	100pF	5%
C13	1500pF	1500pF	10%
C14	0.047µF	0.047µF	10%
C15	0.047µF	0.047µF	10%
C16	470pF	470pF	10%
C17	220pF	220pF	10%
C18	220pF	220pF	10%
C19	0.01µF	0.01µF	10%
C20	100pF	100pF	5%
C21	100pF	100pF	5%
C22	220pF	220pF	10%
C23	0.01µF	0.01µF	10%
C24	0.01µF	0.01µF	10%
L1	22nH	27nH	Coilcraft 0603CS
L2	22nH	30nH	Coilcraft 0603CS
L3	22nH	30nH	Coilcraft 0603CS
L4	10nH	12nH	Coilcraft 0603CS
L5	16nH	30nH	Murata LQW18A
L6	68nH	100nH	Coilcraft 0603CS
R1	100kΩ	100kΩ	5%
R2	100kΩ	100kΩ	5%
R3	0Ω	0Ω	—
Y1	17.63416MHz	12.67917MHz	Crystal, 4.5pF load capacitance
Y2	10.7MHz ceramic filter	10.7MHz ceramic filter	Murata SFECV10.7 series

Note: *Component values vary depending on PCB layout.*

Functional Diagram



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255+3	**21-0140**	**90-0001**

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/05	Initial release	—
1	9/08	Added + to each part to denote lead-free/RoHS-compliant package and explicitly calling out the odd frequency as contact factory for availability	16
2	6/09	Made correction in *Power Amplifer (PA)* section	14
3	11/10	Updated AUTOCAL pin function description and *FSK Demodulator* section	11, 12