To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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2SJ317

Silicon P Channel MOS FET

REJ03G0857-0200
(Previous: ADE-208-1191)
Rev.2.00
Sep 07, 2005

Description

High speed power switching

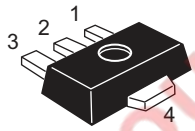
Low voltage operation

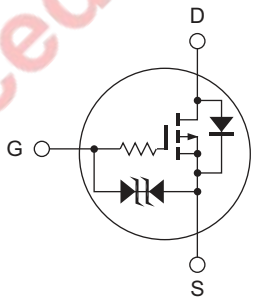
Features

- Very low on-resistance
- High speed switching
- Suitable for camera or VTR motor drive circuit, power switch, solenoid drive and etc.

Outline

RENESAS Package code: PLZZ0004CA-A
(Package name: UPAK®)





1. Gate
2. Drain
3. Source
4. Drain

Note: Marking is “NY”.

*UPAK is a trademark of Renesas Technology Corp.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	–12	V
Gate to source voltage	V_{GSS}	–7	V
Drain current	I_D	±2	A
Drain peak current	$I_{D\ (pulse)}$ Note 1	±4	A
Body to drain diode reverse drain current	I_{DR}	2	A
Channel dissipation	Pch Note 2	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 100 ∝s, duty cycle ≤ 10%
2. Value on the alumina ceramic board (12.5 · 20 · 0.7 mm)

Electrical Characteristics

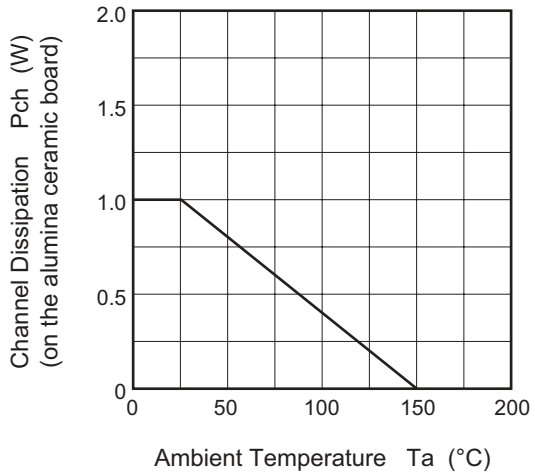
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)\ DSS}$	–12	—	—	V	I_D = –1 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)\ GSS}$	±7	—	—	V	I_G = ±10 ∝A, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±5	∝A	V_{GS} = ±6.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–1	∝A	V_{DS} = –8 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS\ (off)}$	–0.4	—	–1.4	V	I_D = –100 ∝A, V_{DS} = –5 V
Static drain to source on state resistance	$R_{DS\ (on)\ 1}$	—	0.4	0.7	Ω	I_D = –0.5 A, V_{GS} = –2.2 V Note 3
	$R_{DS\ (on)\ 2}$	—	0.28	0.35	Ω	I_D = –1 A, V_{GS} = –4 V Note 3
Forward transfer admittance	$\|y_{fs}\|$	1.0	2.3	—	S	I_D = –1 A, V_{DS} = –5 V Note 3
Input capacitance	Ciss	—	63	—	pF	V_{DS} = –5 V
Output capacitance	Coss	—	180	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	23	—	pF	f = 1 MHz
Turn-on delay time	$t_{d\ (on)}$	—	500	—	ns	I_D = –0.2 A
Turn-off delay time	$t_{d\ (off)}$	—	2860	—	ns	Vin = –4 V, R_L = 51 Ω

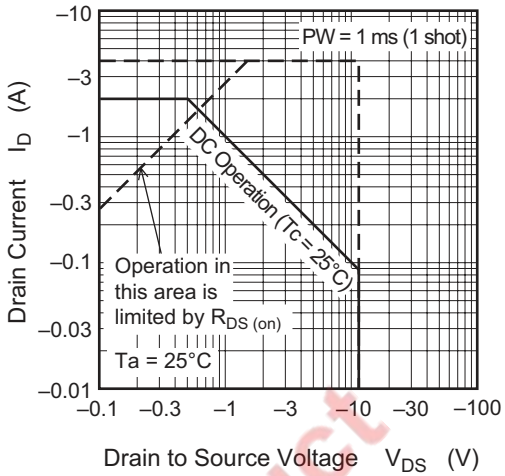
Note: 3. Pulse test

Main Characteristics

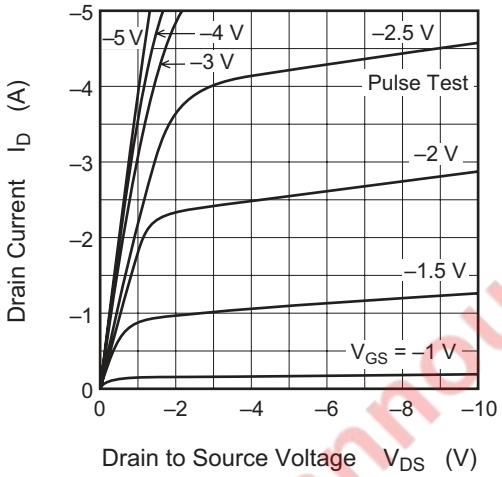
Power vs. Temperature Derating



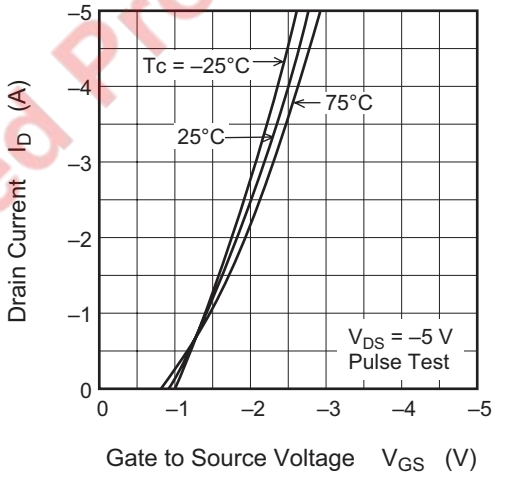
Maximum Safe Operation Area



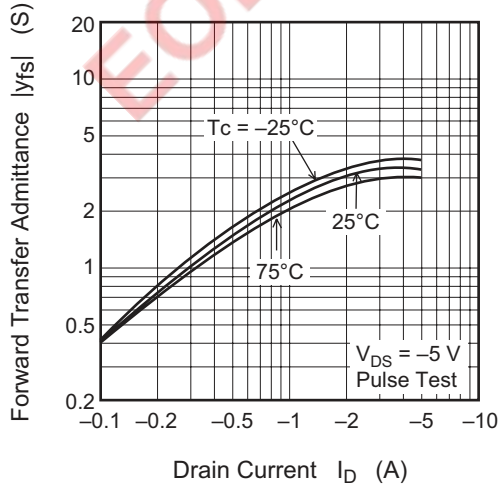
Typical Output Characteristics



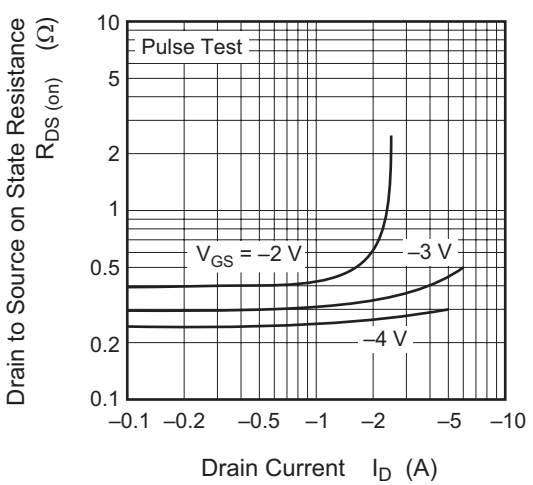
Typical Foward Transfer Characteristics



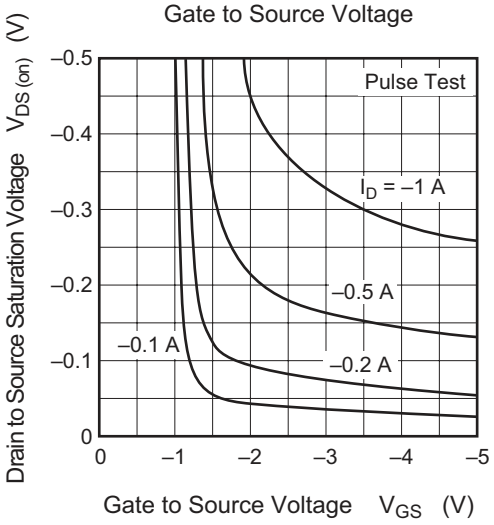
Forward Transfer Admittance vs. Drain Current



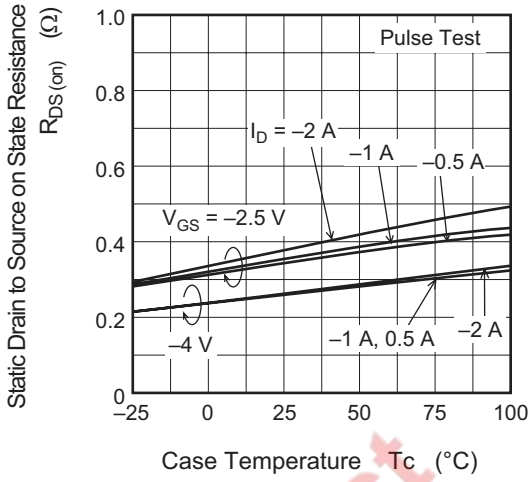
Drain to Source on State Resistance vs. Drain Current



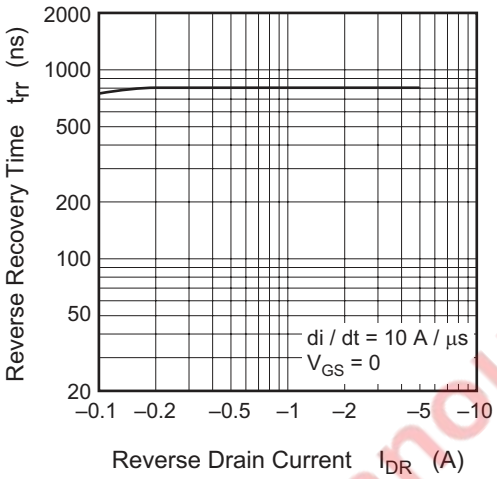
Drain to Source Saturation Voltage vs. Gate to Source Voltage



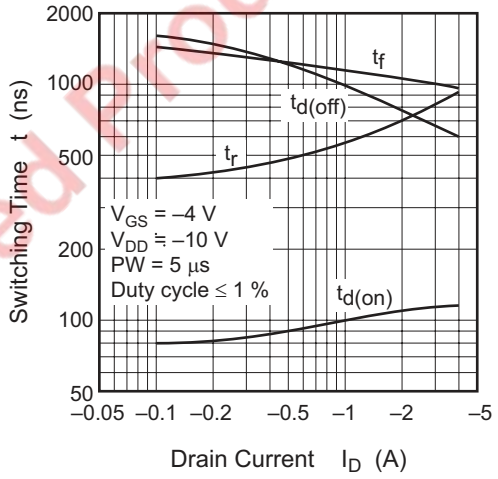
Static Drain to Source on State Resistance vs. Temperature



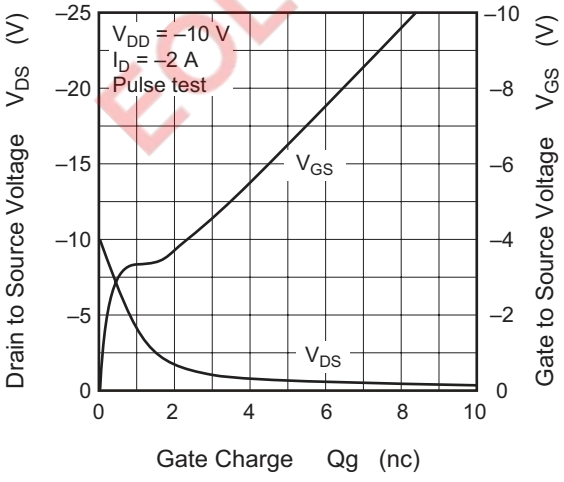
Reverse Recovery Time vs. Recovery Time



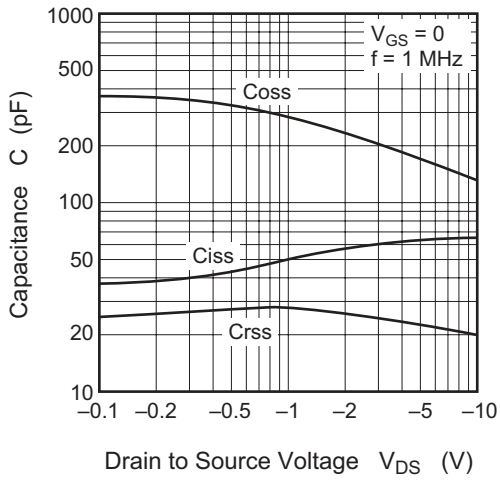
Switching Time vs. Drain Current



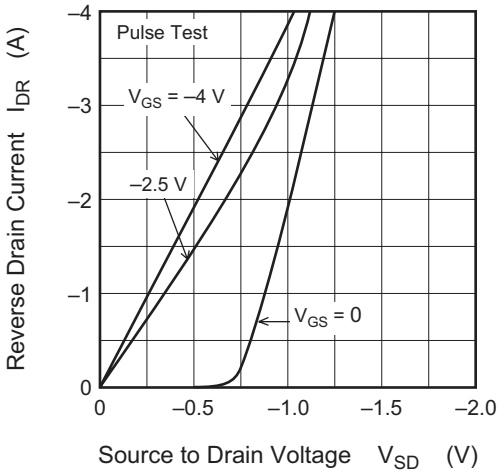
Dynamic Input Characteristics



Typical Capacitance vs. Drain to Source Voltage



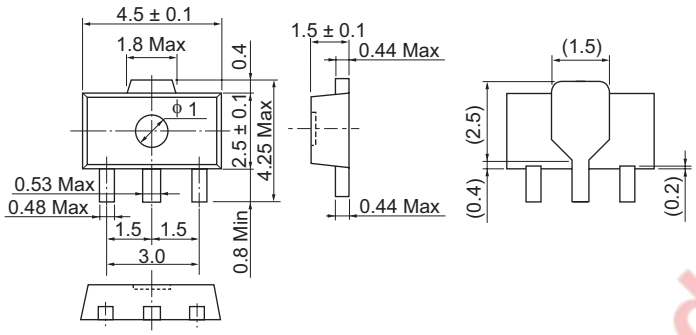
Reverse Drain Current vs.
Source to Drain Voltage



Package Dimensions

JEITA Package Code	RENESAS Code	Package Name	MASS[Typ.]
SC-62	PLZZ0004CA-A	UPAK / UPAKV	0.050g

Unit: mm



Ordering Information

Part Name	Quantity	Shipping Container
2SJ317NYTL-E	1000 pcs	Taping
2SJ317NYTR-E	1000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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