

NP90N03VLG

R07DS0129EJ0100 Rev.1.00 Sep 24, 2010

MOS FIELD EFFECT TRANSISTOR

Description

The NP90N03VLG is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Low on-state resistance
 - $R_{DS(on)1} = 3.2 \text{ m}\Omega$ MAX. ($V_{GS} = 10 \text{ V}$, $I_D = 45 \text{ A}$)
 - --- $R_{DS(on)2} = 8.0 \text{ m}\Omega \text{ MAX}. (V_{GS} = 4.5 \text{ V}, I_D = 35 \text{ A})$
- Low input capacitance
 - Ciss = 5000 pF TYP. $(V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
NP90N03VLG-E1-AY*1	Pure Sn (Tin)	Tape 2500 p/reel	TO-252, Taping (E1 type)
NP90N03VLG-E2-AY*1			TO-252, Taping (E2 type)

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	30	V
Gate to Source Voltage (V _{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	±90	А
Drain Current (pulse) *1	I _{D(pulse)}	±360	А
Total Power Dissipation (T _C = 25°C)	P _{T1}	105	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.2	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	−55 to +175	°C
Repetitive Avalanche Current *2	I _{AR}	41	А
Repetitive Avalanche Energy *2	E _{AR}	168	mJ

Notes: *1. T_C = 25°C, PW \leq 10 μ s, Duty Cycle \leq 1%

Thermal Resistance

^{*2.} $T_{ch(peak)} \le 150$ °C, $R_G = 25 \Omega$

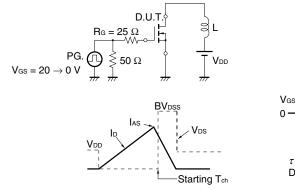
Electrical Characteristics ($T_A = 25^{\circ}C$)

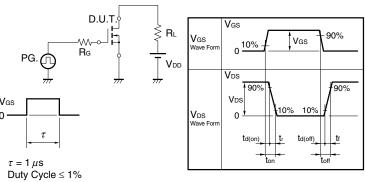
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μA	V _{DS} = 30 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}			±10	μA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	1.4	1.8	2.5	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$
Forward Transfer Admittance *1	y _{fs}	30	67		S	$V_{DS} = 5 \text{ V}, I_{D} = 45 \text{ A}$
Drain to Source On-state	R _{DS(on)1}		2.5	3.2	mΩ	$V_{GS} = 10 \text{ V}, I_D = 45 \text{ A}$
Resistance *1	R _{DS(on)2}		3.8	8.0	mΩ	V_{GS} = 4.5 V, I_{D} = 35 A
Input Capacitance	C _{iss}		5000	7500	pF	V _{DS} = 25 V,
Output Capacitance	Coss		600	900	pF	$V_{GS} = 0 V$,
Reverse Transfer Capacitance	C _{rss}		420	760	pF	f = 1 MHz
Turn-on Delay Time	t _{d(on)}		17	34	ns	$V_{DD} = 15 \text{ V}, I_D = 45 \text{ A},$
Rise Time	t _r		13	33	ns	$V_{GS} = 10 \text{ V},$
Turn-off Delay Time	$t_{d(off)}$		73	146	ns	$R_G = 0 \Omega$
Fall Time	t _f		9	23	ns	
Total Gate Charge	Q_G		90	135	nC	V _{DD} = 24 V,
Gate to Source Charge	Q_{GS}		13		nC	$V_{GS} = 10 \text{ V},$
Gate to Drain Charge	Q_{GD}		26		nC	I _D = 90 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.9	1.5	V	I _F = 90 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		42		ns	$I_F = 90 \text{ A}, V_{GS} = 0 \text{ V},$
Reverse Recovery Charge	Q _{rr}		35		nC	di/dt = 100 A/μs

Note: *1. Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY

TEST CIRCUIT 2 SWITCHING TIME



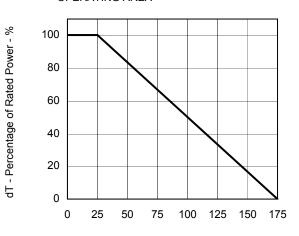


TEST CIRCUIT 3 GATE CHARGE

$$\begin{array}{c|c} D.U.T. \\ I_G = 2 \underbrace{mA}_{WV} \\ \hline \\ PG. \\ \hline \\ \end{array} \begin{array}{c} S \\ 50 \ \Omega \\ \hline \\ \end{array} \begin{array}{c} V_{DD} \\ \hline \\ \end{array}$$

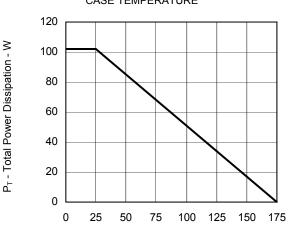
Typical Characteristics $(T_A = 25^{\circ}C)$

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



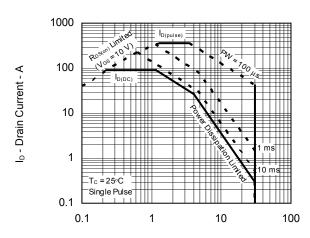
 T_{C} - Case Temperature - $^{\circ}\text{C}$

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



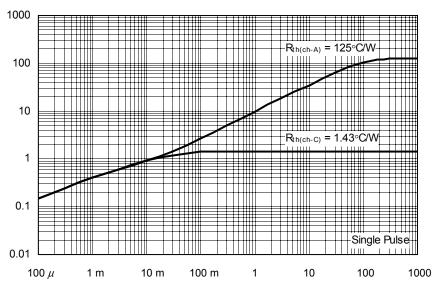
 T_{C} - Case Temperature - $^{\circ}\text{C}$

FORWARD BIAS SAFE OPERATING AREA



 $V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

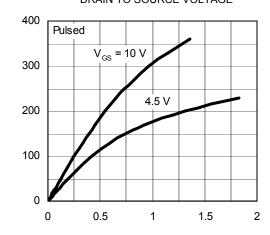


PW - Pulse Width - s

I_D - Drain Current - A

V_{GS(th)} - Gate to Source Threshold Voltage - V

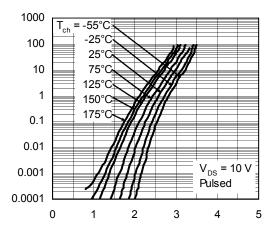
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



 $V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

I_D - Drain Current - A

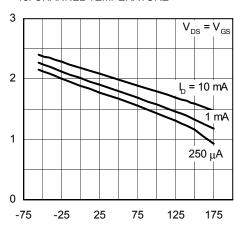
y_s | - Forward Transfer Admittance - S



FORWARD TRANSFER CHARACTERISTICS

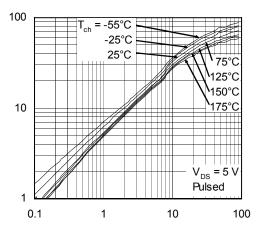
V_{GS} - Gate to Source Voltage - V

GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



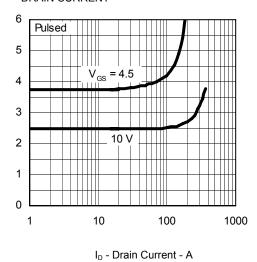
T_{ch} - Channel Temperature - °C

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

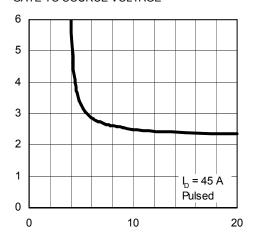


ID - Drain Current - A

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

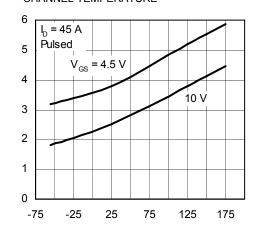


V_{GS} - Gate to Source Voltage - V

 $R_{\text{DS(on)}}$ - Drain to Source On-state Resistance - $m\Omega$

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DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



T_{ch} - Channel Temperature - °C

100000

V_{DS} - Drain to Source Voltage - V

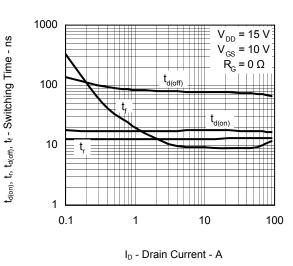
t_{rr} - Reverse Recovery Time - ns

V_{GS} = 0 V

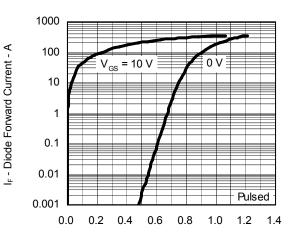
V_{DS} - Drain to Source Voltage - V

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

SWITCHING CHARACTERISTICS

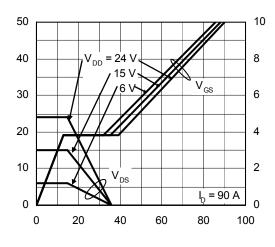


SOURCE TO DRAIN DIODE FORWARD VOLTAGE



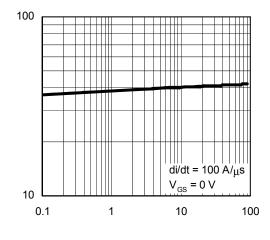
 $V_{\text{F(S-D)}}$ - Source to Drain Voltage - V

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



Q_G - Gate Charge - nC

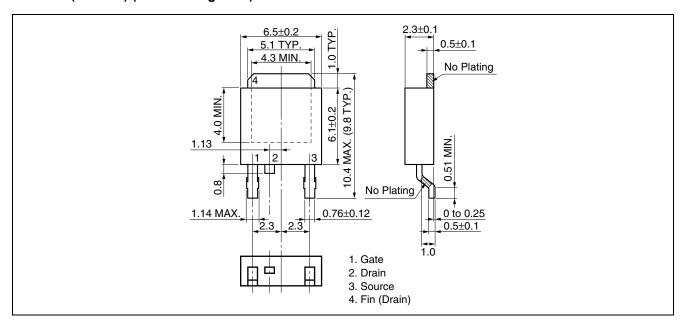
REVERSE RECOVERY TIME vs. DRAIN CURRENT



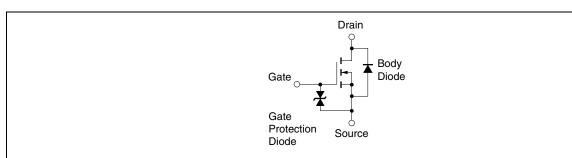
I_F - Drain Current - A

Package Drawings (Unit: mm)

TO-252 (MP-3ZP) (Mass: 0.27 g TYP.)



Equivalent Circuit



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Revision History NP90N03VLG

		Description		
Rev.	Date	Page	Summary	
1.00	Sep 24, 2010	-	First Edition Issued	

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