

# Low-Power BiCMOS Current-Mode PWM

## FEATURES

- 100 $\mu$ A Typical Starting Supply Current
- 500 $\mu$ A Typical Operating Supply Current
- Operation to 1MHz
- Internal Soft Start
- Internal Fault Soft Start
- Internal Leading-Edge Blanking of the Current Sense Signal
- 1 Amp Totem-Pole Output
- 70ns Typical Response from Current-Sense to Gate Drive Output
- 1.5% Tolerance Voltage Reference
- Same Pinout as UC3842 and UC3842A

## DESCRIPTION

The UCC1800/1/2/3/4/5 family of high-speed, low-power integrated circuits contain all of the control and drive components required for off-line and DC-to-DC fixed frequency current-mode switching power supplies with minimal parts count.

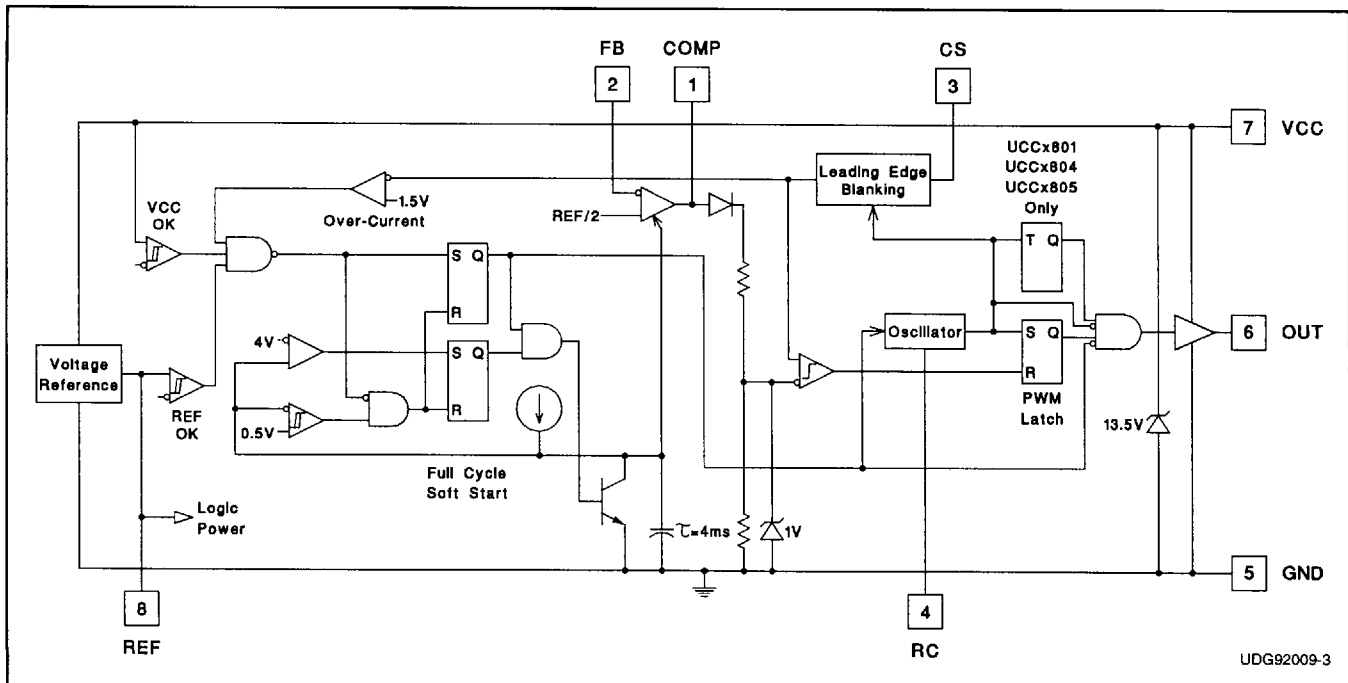
These devices have the same pin configuration as the UC1842/3/4/5 family, and also offer the added features of internal full-cycle soft start and internal leading-edge blanking of the current-sense input.

The UCC1800/1/2/3/4/5 family offers a variety of package options, temperature range options, choice of maximum duty cycle, and choice of critical voltage levels. Lower reference parts such as the UCC1803 and UCC1805 fit best into battery operated systems, while the higher reference and the higher UVLO hysteresis of the UCC1802 and UCC1804 make these ideal choices for use in off-line power supplies.

The UCC180x series is specified for operation from -55 $^{\circ}$ C to +125 $^{\circ}$ C, the UCC280x series is specified for operation from -40 $^{\circ}$ C to +85 $^{\circ}$ C, and the UCC380x series is specified for operation from 0 $^{\circ}$ C to +70 $^{\circ}$ C.

Part Number	Maximum Duty Cycle	Reference Voltage	Turn-On Threshold	Turn-Off Threshold
UCCx800	100%	5V	7.2V	6.9V
UCCx801	50%	5V	9.4V	7.4V
UCCx802	100%	5V	12.5V	8.3V
UCCx803	100%	4V	4.1V	3.6V
UCCx804	50%	5V	12.5V	8.3V
UCCx805	50%	4V	4.1V	3.6V

## BLOCK DIAGRAM



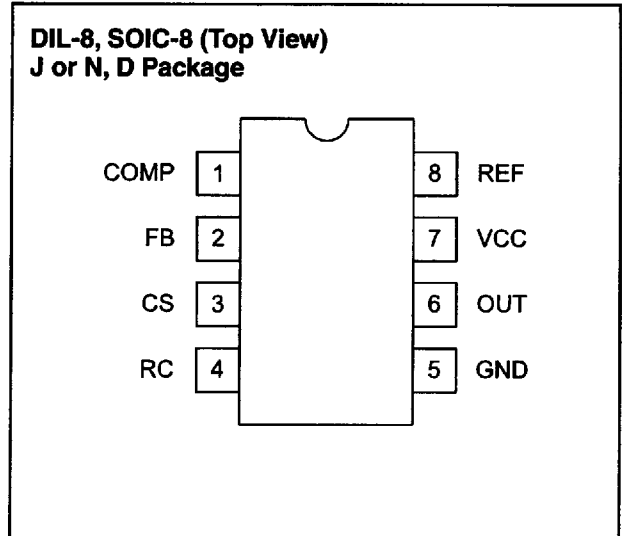
**ABSOLUTE MAXIMUM RATINGS (Note 1)**

V <sub>CC</sub> Voltage (Note 2)	12.0V
V <sub>CC</sub> Current	30.0mA
OUT Current	±1.0A
OUT Energy (Capacitive Load)	20.0μJ
Analog Inputs (FB, CS)	-0.3V to 6.3V
Power Dissipation at T <sub>A</sub> < +25°C (N or J Package)	1.0W
Power Dissipation at T <sub>A</sub> < +25°C (D Package)	0.65W
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	+300°C

*Note 1: All voltages are with respect to GND. All currents are positive into the specified terminal. Consult Unitorde databook for information regarding thermal specifications and limitations of packages.*

*Note 2: In normal operation V<sub>CC</sub> is powered through a current limiting resistor. Absolute maximum of 12V applies when V<sub>CC</sub> is driven from a low impedance source such that I<sub>CC</sub> does not exceed 30mA.*

**CONNECTION DIAGRAM**



**ELECTRICAL CHARACTERISTICS** Unless otherwise stated, these specifications apply for -55°C ≤ T<sub>A</sub> ≤ +125°C for UCC180x; -40° ≤ T<sub>A</sub> ≤ +85°C for UCC280x; 0°C ≤ T<sub>A</sub> ≤ +70°C for UCC380x; V<sub>CC</sub>=10V (Note 3); RT=100k from REF to RC; CT=330pF from RC to GND; 0.1μF capacitor from V<sub>CC</sub> to GND; 0.1μF capacitor from V<sub>REF</sub> to GND. T<sub>A</sub>=T<sub>J</sub>.

PARAMETER	TEST CONDITIONS	UCC180X UCC280X			UCC380X			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Reference Section</b>								
Output Voltage	T <sub>J</sub> =+25°C, I=0.2mA, UCCx800/1/2/4	4.925	5.00	5.075	4.925	5.00	5.075	V
	T <sub>J</sub> =+25°C, I=0.2mA, UCCx803/5	3.94	4.00	4.06	3.94	4.00	4.06	
Load Regulation	0.2mA < I < 5mA		10	30		10	25	mV
Total Variation	UCCx800/1/2/4 (Note 7)	4.88	5.00	5.10	4.88	5.00	5.10	V
	UCCx803/5 (Note 7)	3.90	4.00	4.08	3.90	4.00	4.08	
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T <sub>J</sub> =+25°C (Note 9)		70			70		μV
Long Term Stability	T <sub>A</sub> =+125°C, 1000 Hours (Note 9)		5			5		mV
Output Short Circuit		-5		-35	-5		-35	mA
<b>Oscillator Section</b>								
Oscillator Frequency	UCCx800/1/2/4 (Note 4)	40	46	52	40	46	52	kHz
	UCCx803/5 (Note 4)	26	31	36	26	31	36	
Temperature Stability	(Note 9)		2.5			2.5		%
Amplitude peak-to-peak		2.25	2.40	2.55	2.25	2.40	2.55	V
Oscillator Peak Voltage			2.45			2.45		V
<b>Error Amplifier Section</b>								
Input Voltage	COMP=2.5V; UCCx800/1/2/4	2.44	2.50	2.56	2.44	2.50	2.56	V
	COMP=2.0V; UCCx803/5	1.95	2.0	2.05	1.95	2.0	2.05	
Input Bias Current		-1		1	-1		1	μA
Open Loop Voltage Gain		60	80		60	80		dB
COMP Sink Current	FB=2.7V, COMP=1.1V	0.3		3.5	0.4		2.5	mA
COMP Source Current	FB=1.8V, COMP=REF-1.2V	-0.2	-0.5	-0.8	-0.2	-0.5	-0.8	mA
Gain Bandwidth Product	(Note 9)		2			2		MHz

**UCC1800/1/2/3/4/5**  
**UCC2800/1/2/3/4/5**  
**UCC3800/1/2/3/4/5**

**ELECTRICAL CHARACTERISTICS** Unless otherwise stated, these specifications apply for  $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$  for UCC180x;  $-40^{\circ} \leq T_A \leq +85^{\circ}\text{C}$  for UCC280x;  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$  for UCC380x;  $V_{CC}=10\text{V}$  (Note 3);  $RT=100\text{k}$  from REF to RC;  $CT=330\text{pF}$  from RC to GND;  $0.1\mu\text{F}$  capacitor from  $V_{CC}$  to GND;  $0.1\mu\text{F}$  capacitor from  $V_{REF}$  to GND.  $T_A=T_J$ .

PARAMETER	TEST CONDITIONS	UCC180X UCC280X			UCC380X			UNITS
<b>PWM Section</b>								
Maximum Duty Cycle	UCCx800/2/3	97	99	100	97	99	100	%
	UCCx801/4/5	48	49	50	48	49	50	
Minimum Duty Cycle	COMP=0V			0			0	%
<b>Current Sense Section</b>								
Gain	(Note 5)	1.10	1.65	1.80	1.10	1.65	1.80	V/V
Maximum Input Signal	COMP=5V (Note 6)	0.9	1.0	1.1	0.9	1.0	1.1	V
Input Bias Current		-200		200	-200		200	nA
CS Blank Time		50	100	150	50	100	150	ns
Over-Current Threshold		1.42	1.55	1.68	1.42	1.55	1.68	V
COMP to CS Offset	CS=0V	0.45	0.90	1.35	0.45	0.90	1.35	V
<b>Output Section</b>								
OUT Low Level	I=20mA, all parts		0.1	0.4		0.1	0.4	V
	I=200mA, all parts		0.35	0.90		0.35	0.90	V
	I=50mA, VCC=5V, UCCx803/5		0.15	0.40		0.15	0.40	V
	I=20mA, VCC=0V, all parts		0.7	1.2		0.7	1.2	V
OUT High V <sub>SAT</sub> (V <sub>CC</sub> -OUT)	I=-20mA, all parts		0.15	0.40		0.15	0.40	V
	I=-200mA, all parts		1.0	1.9		1.0	1.9	V
	I=-50mA, VCC=5V, UCCx803/5		0.4	0.9		0.4	0.9	V
Rise Time	C <sub>L</sub> =1nF		41	70		41	70	ns
Fall Time	C <sub>L</sub> =1nF		44	75		44	75	ns
<b>Undervoltage Lockout Section</b>								
Start Threshold (Note 8)	UCCx800	6.6	7.2	7.8	6.6	7.2	7.8	V
	UCCx801	8.6	9.4	10.2	8.6	9.4	10.2	V
	UCCx802/4	11.5	12.5	13.5	11.5	12.5	13.5	V
	UCCx803/5	3.7	4.1	4.5	3.7	4.1	4.5	V
Stop Threshold (Note 8)	UCCx1800	6.3	6.9	7.5	6.3	6.9	7.5	V
	UCCx1801	6.8	7.4	8.0	6.8	7.4	8.0	V
	UCCx802/4	7.6	8.3	9.0	7.6	8.3	9.0	V
	UCCx803/5	3.2	3.6	4.0	3.2	3.6	4.0	V
Start to Stop Hysteresis	UCCx800	0.12	0.3	0.48	0.12	0.3	0.48	V
	UCCx801	1.6	2	2.4	1.6	2	2.4	V
	UCCx802/4	3.5	4.2	5.1	3.5	4.2	5.1	V
	UCCx803/5	0.2	0.5	0.8	0.2	0.5	0.8	V
<b>Soft Start Section</b>								
COMP Rise Time	FB=1.8V, Rise from 0.5V to REF-1V		4	10		4	10	ms

**ELECTRICAL CHARACTERISTICS** Unless otherwise stated, these specifications apply for  $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$  for UCC180x;  $-40^{\circ} \leq T_A \leq +85^{\circ}\text{C}$  for UCC280x;  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$  for UCC380x;  $V_{CC}=10\text{V}$  (Note 3);  $RT=100\text{k}$  from REF to RC;  $CT=330\text{pF}$  from RC to GND;  $0.1\mu\text{F}$  capacitor from  $V_{CC}$  to GND;  $0.1\mu\text{F}$  capacitor from  $V_{REF}$  to GND.  $T_A=T_J$ .

PARAMETER	TEST CONDITIONS	UCC180X UCC280X			UCC380X			UNITS
<b>Overall Section</b>								
Start-up Current	$V_{CC} < \text{Start Threshold}$		0.1	0.2		0.1	0.2	mA
Operating Supply Current	$FB=0\text{V}, CS=0\text{V}$		0.5	1.0		0.5	1.0	mA
VCC Internal Zener Voltage	$I_{CC}=10\text{mA}$ (Note 8)	12	13.5	15	12	13.5	15	V
VCC Internal Zener Voltage Minus Start Threshold Voltage	UCCx802/4	0.5	1.0		0.5	1.0		V

Note 3: Adjust VCC above the start threshold before setting at 10V.

Note 4: Oscillator frequency for the UCCx800, UCCx802 and UCCx803 is the output frequency.  
Oscillator frequency for the UCCx801, UCCx804 and UCCx805 is twice the output frequency.

Note 5: Gain is defined by:  $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}} \quad 0 \leq V_{CS} \leq 0.8\text{V}$ .

Note 6: Parameter measured at trip point of latch with Pin 2 at 0V.

Note 7: Total Variation includes temperature stability and load regulation.

Note 8: Start Threshold, Stop Threshold and Zener Shunt Thresholds track one another.

Note 9: Guaranteed by design. Not 100% tested in production.

## PIN DESCRIPTIONS

**COMP:** COMP is the output of the error amplifier and the input of the PWM comparator.

Unlike other devices, the error amplifier in the UCC3800 family is a true, low output-impedance, 2MHz operational amplifier. As such, the COMP terminal can both source and sink current. However, the error amplifier is internally current limited, so that you can command zero duty cycle by externally forcing COMP to GND.

The UCC3800 family features built-in full cycle Soft Start. Soft Start is implemented as a clamp on the maximum COMP voltage.

**CS:** CS is the input to the current sense comparators. The UCC3800 family has two different current sense comparators: the PWM comparator and an over-current comparator.

The UCC3800 family contains digital current sense filtering, which disconnects the CS terminal from the current sense comparator during the 100ns interval immediately following the rising edge of the OUT pin. This digital filtering, also called leading-edge blanking, means that in most applications, no analog filtering (RC filter) is required on CS. Compared to an external RC filter technique, the leading-edge blanking provides a smaller effective CS to OUT propagation delay. Note, however, that the minimum non-zero On-Time of the OUT signal is directly affected by the leading-edge-blanking and the CS to OUT propagation delay.

The over-current comparator is only intended for fault sensing, and exceeding the over-current threshold will cause a soft start cycle.

**FB:** FB is the inverting input of the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

**GND:** GND is reference ground and power ground for all functions on this part.

**OUT:** OUT is the output of a high-current power driver capable of driving the gate of a power MOSFET with peak currents exceeding  $\pm 750\text{mA}$ . OUT is actively held low when  $V_{CC}$  is below the UVLO threshold.

The high-current power driver consists of FET output devices, which can switch all of the way to GND and all of the way to  $V_{CC}$ . The output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external schottky clamp diodes are not required.

**RC:** RC is the oscillator timing pin. For fixed frequency operation, set timing capacitor charging current by connecting a resistor from REF to RC. Set frequency by connecting a timing capacitor from RC to GND. For best performance, keep the timing capacitor lead to GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions.

The frequency of oscillation can be estimated with the following equations:

**PIN DESCRIPTIONS (continued)**

UCCx800/1/2/4:  $F = \frac{15}{R \cdot C}$

UCCx803, UCCx805:  $F = \frac{10}{R \cdot C}$

where frequency is in Hz, resistance is in ohms, and capacitance is in farads. The recommended range of timing resistors is between 10k and 200k and timing capacitor is 100pF to 1000pF. Never use a timing resistor less than 10k.

To prevent noise problems, bypass VCC to GND with a ceramic capacitor as close to the VCC pin as possible. An electrolytic capacitor may also be used in addition to the ceramic capacitor.

**REF:** REF is the voltage reference for the error amplifier and also for many other functions on the IC. REF is also used as the logic power supply for high speed switching logic on the IC.

When VCC is greater than 1V and less than the UVLO threshold, REF is pulled to ground through a 5k ohm resistor.

This means that REF can be used as a logic output indicating power system status. It is important for reference stability that REF is bypassed to GND with a ceramic capacitor as close to the pin as possible. An electrolytic capacitor may also be used in addition to the ceramic capacitor. A minimum of 0.1µF ceramic is required. Additional REF bypassing is required for external loads greater than 2.5mA on the reference.

To prevent noise problems with high speed switching transients, bypass REF to ground with a ceramic capacitor very close to the IC package.

**VCC:** VCC is the power input connection for this device. In normal operation VCC is powered through a current limiting resistor. Although quiescent VCC current is very low, total supply current will be higher, depending on OUT current. Total VCC current is the sum of quiescent VCC current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from:

$$I_{OUT} = Q_g \times F.$$

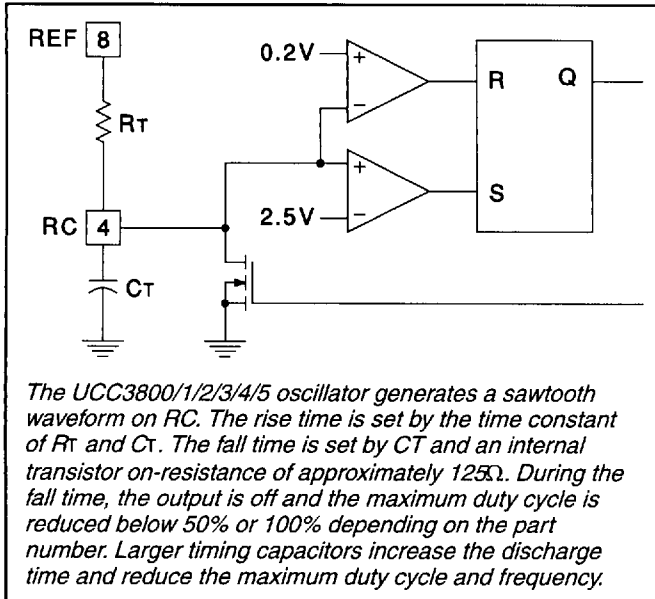


Figure 1. Oscillator

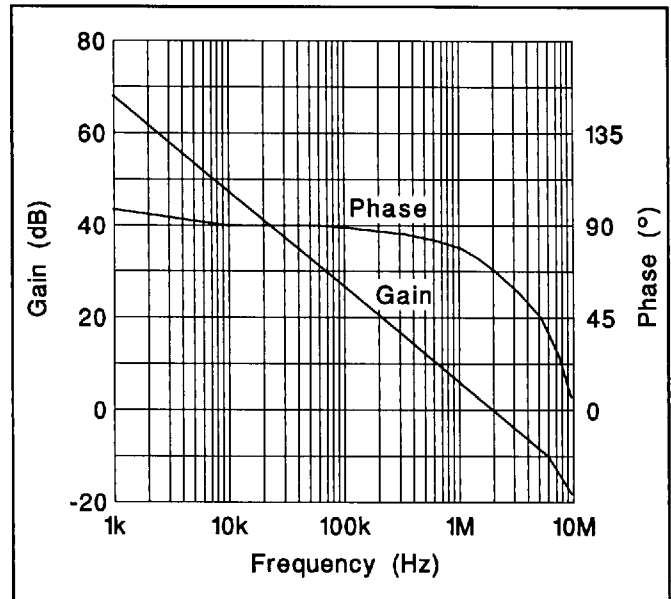


Figure 2. Error Amplifier Gain/Phase Response

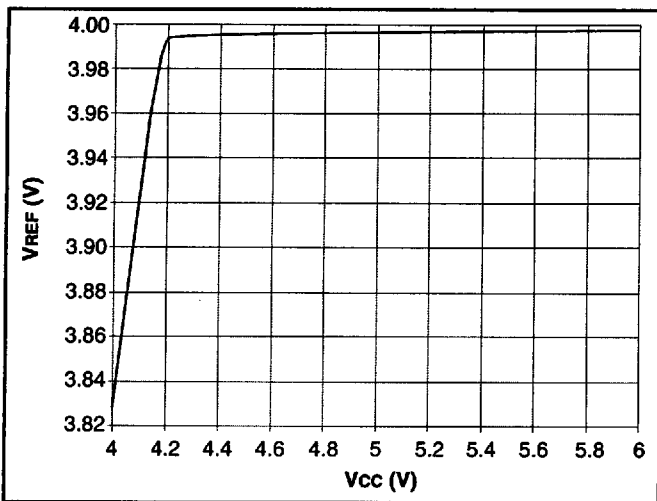


Figure 3. UCC1803/5  $V_{REF}$  vs.  $V_{CC}$ ;  $I_{LOAD} = 0.5mA$

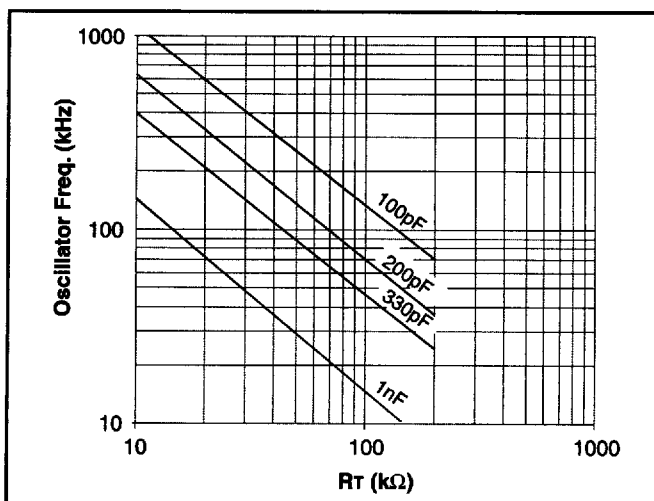


Figure 4. UCC1800/1/2/4 Oscillator Freq vs.  $R_T$  and  $C_T$

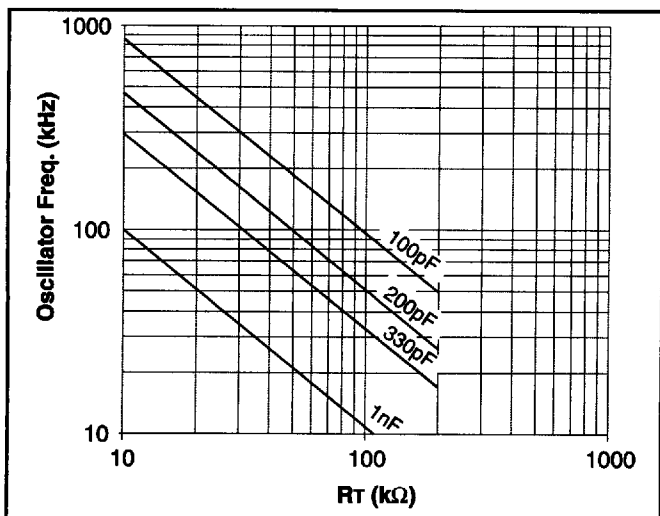


Figure 5. UCC1803/5 Oscillator Freq vs.  $R_T$  and  $C_T$

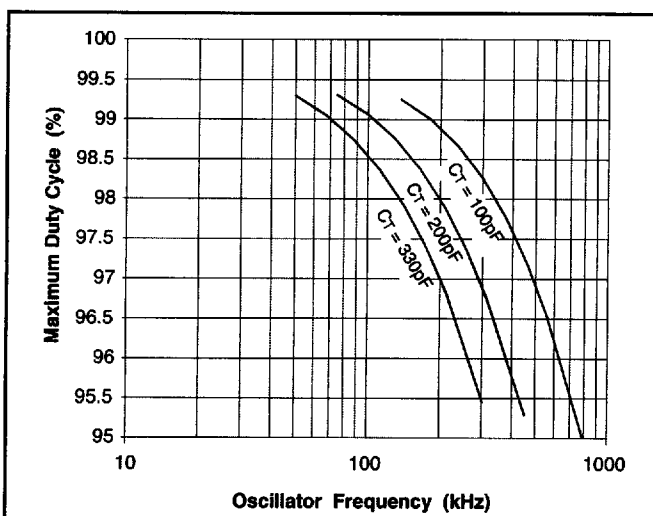


Figure 6. UCC1800/2/3 Maximum Duty Cycle vs. Oscillator Frequency

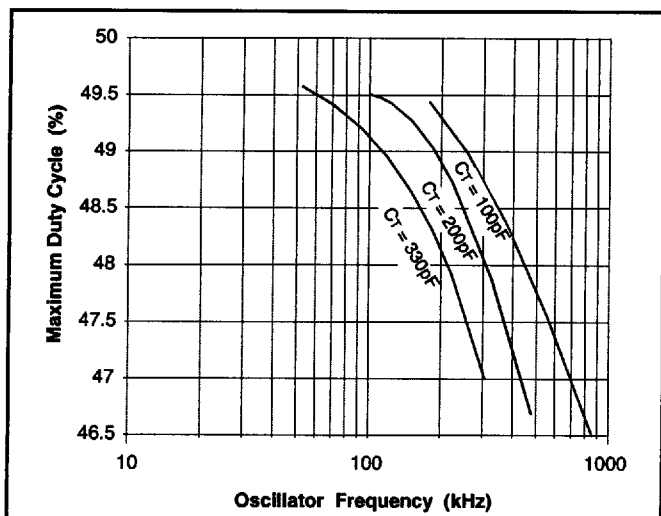


Figure 7. UCC1801/4/5 Maximum Duty Cycle vs. Oscillator

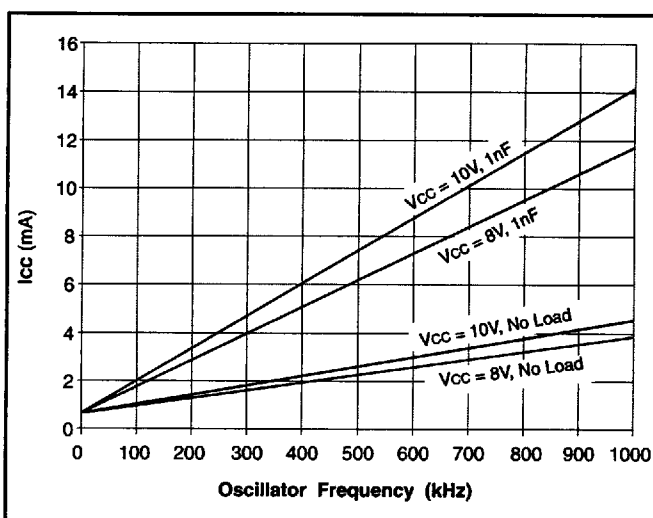


Figure 8. UCC1800  $I_{CC}$  vs. Oscillator Frequency

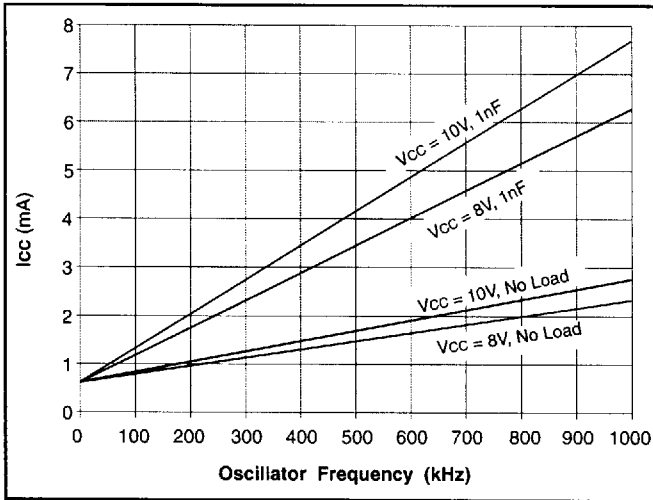


Figure 8. UCC1805 ICC vs. Oscillator Frequency

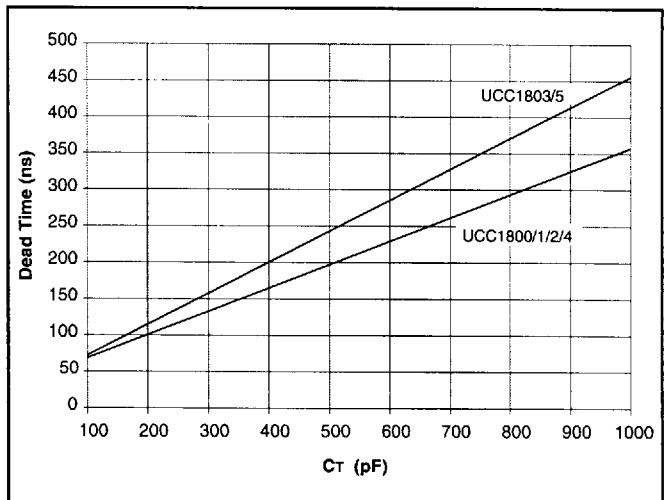


Figure 9. Dead Time vs.  $C_T$ ,  $R_T = 100k$

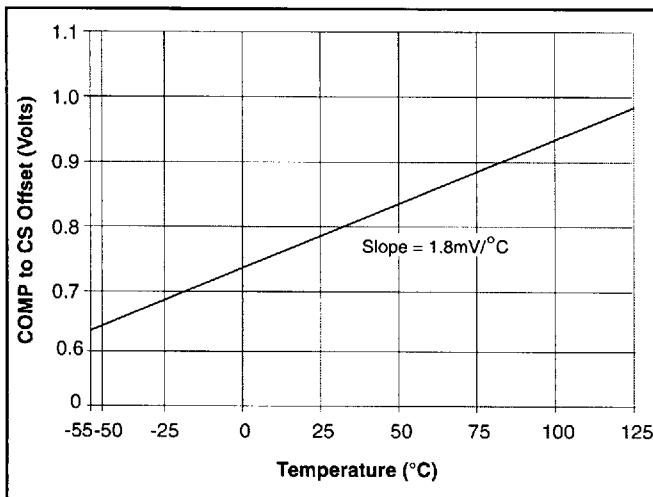
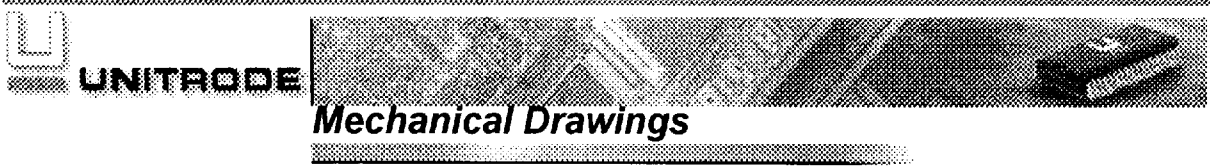


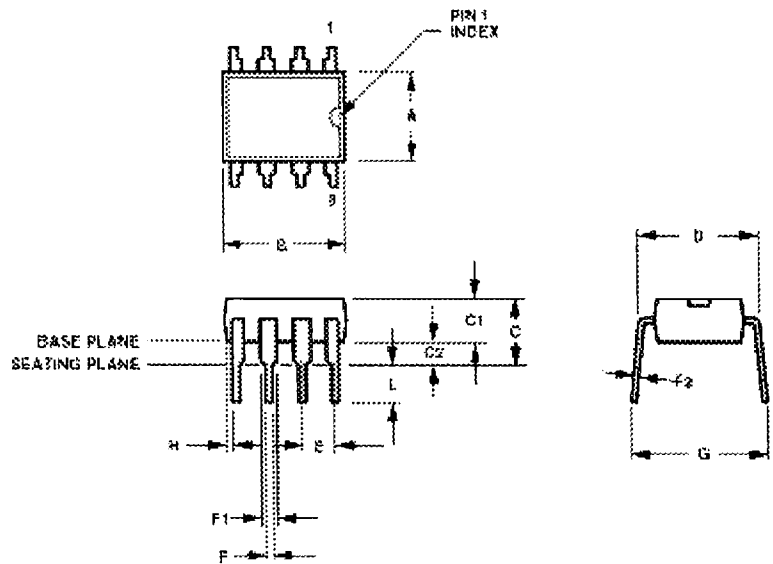
Figure 10. COMP to CS Offset vs. Temperature, CS = 0V



[Back to Packaging Index](#)

**8-PIN PLASTIC DIP ~ N PACKAGE SUFFIX**

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.320	.400	9.40	10.16	1
C	-	.210	-	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	-	0.13	-	
L	.115	.160	2.92	4.06	



**NOTES:**

1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.



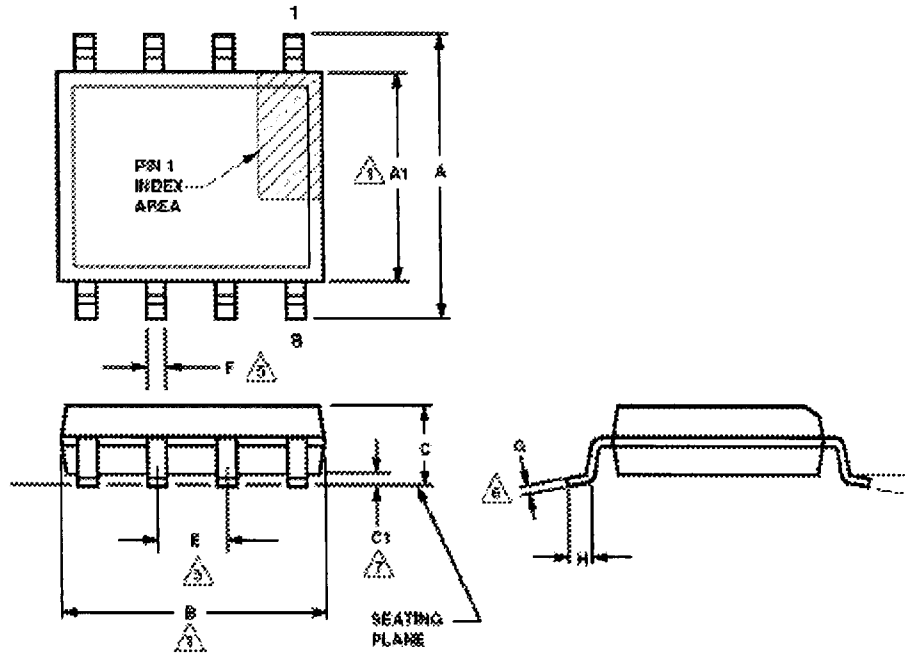


# Mechanical Drawings

[Back to Packaging Index](#)

## 8-PIN SOIC SURFACE MOUNT~ D, DP PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.189	.196	4.80	4.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.23
E	.050 BSC		1.27 BSC	
F	.014	.019	0.35	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°



**NOTES:**

- 1 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.006 IN. PER SIDE.
- 2 LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
- 3 THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
- 4 CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
- 5 DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- 6 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
- 7 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

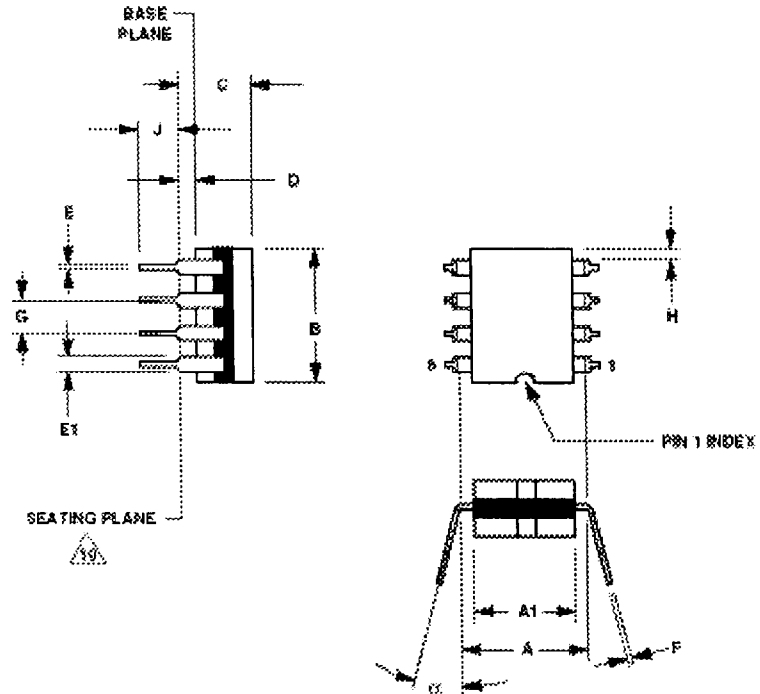


# Mechanical Drawings

[Back to Packaging Index](#)

## 8-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	-	0.405	-	10.29	4
C	-	0.200	-	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	-	0.13	-	6
J	0.125	0.200	3.18	5.08	
$\epsilon$	0°	15°	0°	15°	



### NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION 'E1' MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 4, 5 AND 8 ONLY.
3. DIMENSION 'D' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN  $\pm 0.010$  (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 4, 5 AND 8).
7. DIMENSION 'A' SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN  $\epsilon = 0^\circ$ .
8. THE MAXIMUM LIMITS OF DIMENSIONS 'E' AND 'F' SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.