eZ80F920020MOD

eZ80F92 Flash Module

Product Specification

PS018906-0908

Warning: DO NOT USE IN LIFE SUPPORT

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Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

Date	Revision Level	Description	Page Number
September 2008	06	Removed Preliminary. Updated as per latest template and style guide changes.	All
December 2003	05	Fixed incorrect conditional indicators.	All
August 2003	04	Modified to remove zservice@zilog.com and other external hyperlinks to documentation.	All
February 2003	03	Fixed incorrect hyperlinks.	All
January 2003	02	Modified references for eZ80Acclaim!®.	All

Table of Contents

Architectural Overview

Zilog's eZ80F92 Flash Module is a low-cost, general-purpose compact module. It is specially designed for the rapid development and deployment of embedded systems. This expandable module is powered by Zilog's latest power-efficient, high-speed, optimized pipeline architecture eZ80F92 Microcontroller Unit (MCU). This MCU, the first device in Zilog's eZ80Acclaim!® product line, features 128 KB of on-chip Flash memory and 8 KB of on-chip SRAM.

The eZ80F92 MCU is a high-speed, single-cycle instruction-fetch MCU, which can operate with a clock speed of 20 MHz. It can operate in Z80®-compatible addressing mode (64 KB) or full 24-bit addressing mode (16 MB).

The rich peripheral set of the eZ80F92 Flash Module makes it suitable for a variety of applications, including industrial control, IrDA connectivity, communication, security, automation, point-of-sale (POS) terminals.

Note: *The eZ80F92 Flash Module incorporates the eZ80F92 MCU. The eZ80F92 can be replaced with the eZ80F93 MCU, which features 64 KB of internal Flash memory and 4 KB of internal SRAM.*

eZ80F92 Flash Module Features

The key features of eZ80F92 Flash Module include:

- eZ80Acclaim! Flash MCU with factory-default operating clock frequency at 20 MHz
- 512 KB zero-wait-state onboard SRAM
- 128 KB on-chip Flash memory
- GoldCap backup for Real-Time Clock (RTC)
- Input/Output (I/O) connector provides 24 general-purpose 5 V-tolerant I/O pinouts
- Zilog's industry-leading IrDA transceiver—Zilog's ZHX1810
- I/O circuit Flash programming circuitry
- Onboard connector provides I^2C 2-wire SDA/SCL interface
- Onboard connector provides I/O bus for external peripheral connections (IRQ, $\overline{CS}$, 24 address, 8 data)
- Low-cost adaptation to carrier board via two 2 x 25 pin (2.54 mm) headers
- Horizontal or vertical mounting onto the eZ80® Development Platform
- Small footprint 64 x 64 mm
- 3.3 V power supply
- Standard operating temperature range: 0 ºC to +70 ºC

eZ80F92 Flash Module Bill of Materials

Table 1 lists the installed components of the eZ80F92 Flash Module.

Table 1. Bill of Materials for the eZ80F92 Flash Module

Part Number	Part Name	Qty.	Jumper Location	Manufacturer
98C0873-001	FAB, eZ80F92/93 MODULE, Rev. A	1	—	Prime Technologies
35-0180-12	IC, SRAM, 512K x 8, 12 ns, 3 V, 36-SOJ	1	U1	Alliance Semi. AS7C34096-12JC
35-0016-05	IC, 74LVC04, 3.3 V, GATE, 14-SOIC	1	U2	Texas Instruments SN74LVC04AD
35-0719-00	IC, MAX6328, RESET, SOT-23	1	U4	Maxim Inc. MAX6328UR29-T
ZHX1810	IC, IR Transceiver, low profile	1	U5	Zilog Inc. ZHX1810MV115THTR
35-0062-01	IC, 74LCX32, LV, QUAD, or 14-TSSOP	1	U6	Fairchild Semi. 74LCX32MTC
EZ80F92	IC, eZ80F92AZ020SC, 20 MHZ, 100 V QFP	1	U8	Zilog Inc. EZ80F92AZ020SC
48-1013-01	DIODE, TVS ARRAY, XCVR PROT, 8-SOIC	1	U9	Semtec LCDA15C-6
17-2005-70	CAP, 1, 000 pF, 50 V, ceramic chip, 0603	5	C3, C5, C21–23	Panasonic ECJ-1VC1H102J
17-2005-66	CAP, 0.1µF, 16 V, ceramic chip, 0603	9	C4, C6–9, C13–15, C18	Kemet Inc. C0603C104K5RAC
17-2005-54	CAP, 0.01 µF, 50V, ceramic chip, 0603	1	C10	Panasonic ECJ-1VB1C103K
17-2005-83	CAP, 0.33 µF, 16 V, ceramic chip, 0603	1	C11	Panasonic ECJ-1VF1C334Z
17-2005-39	CAP, 560 pF, 50 V, ceramic chip, 0603	1	C12	Panasonic ECJ-1VC1H561J
17-2001-03	CAP, 12 pF, 50 V, ceramic chip, 0603	4	C16, C17, C20, C24	Panasonic ECJ-1VC1H120J
15-0100-01	CAP, 1.10 F, 5.5 V, GOLD, SD, COIN	1	C19	Panasonic EEC-SOHD104V
48-0030-04	Diode, Schottky, Power rectifier, SMT	1	D1	On Semiconductor MBR0520LT1

Table 1. Bill of Materials for the eZ80F92 Flash Module (Continued)

Part Number	Part Name	Qty.	Jumper Location	Manufacturer
46-3001-03	Resistor, 10 kΩ, 1%, 1/16W, 0603 SMT	9	R1, 11, 12, 17, 19, 29, 30, 34, 36	Sprague 420CK472X2PD
46-3000-00	Resistor, 0 Ω, 1%, 1/16W, 0603 SMT	2	R2, C25	"
46-3000-71	Resistor, 2.21 kΩ, 1%, 1/16W, 0603 SMT	3	R3, R10, R33	"
46-3000-35	Resistor, 68 Ω, 1%, 1/16W, 0603 SMT	1	R5	"
46-1005-03	Resistor, 2.7 Ω, 5%, 1/4W, 1206 SMT	1	R6	"
46-3001-03	Resistor, 4.75 kΩ, 1%, 1/16W, 0603 SMT	4	R7, 8, 13, 22	"
46-3000-27	Resistor, 33.2 Ω, 1%, 1/16W, 0603 SMT	1	R9	"
46-3000-39	Resistor, 100 Ω, 1%, 1/16W, 0603 SMT	5	R20, 21, 26, 28, 32	"
46-3000-80	Resistor, 4.99 kΩ, 1%, 1/16W, 0603 SMT	1	R23	"
46-3000-07	Resistor, 8.2 Ω, 1%, 1/16W, 0603 SMT	2	R24, R25	"
46-3001-51	Resistor, 1M Ω, 1%, 1/16W, 0603 SMT	1	R27	"
23-0000-10	Internal crystal, 20.0000 MHz, SER/RESN, HC-49S	2	Y1, Y2	Fox Series HC-49S 20.0000 MHz
23-0006-00	Internal crystal, 32.768 kHz, SER/RESN, TF CASE	1	Y3	NDK MX-38
21-0055-02	Connector, HDR/PIN,. 025SQ, double row	2	JP1, JP2	"

eZ80F92 Controller Features

The key features of eZ80F92 include:

- The eZ80F92 device contains 128 KB of Flash memory and 8 KB of SRAM
- Single-cycle instruction fetch, high-performance, and pipelined eZ80® CPU core
- Low power features including SLEEP mode, HALT mode, and selective peripheral power-down control
- Two Universal Asynchronous Receiver/Transceivers (UARTs) with independent baud rate generators and support for 9-bit operation
- Serial Peripheral Interface (SPI) with independent clock rate generator
- I^2C with independent clock rate generator
- Infrared Data Association (IrDA)-compliant infrared encoder/decoder
- New Direct Memory Access (DMA)-like eZ80 CPU instructions for efficient block data transfer
- Glueless external memory interface with four chip selects, individual wait state generators, and an external WAIT input pin—supports Intel- and Motorola-style buses
- Fixed-priority vectored interrupts (both internal and external) and interrupt controller
- RTC with an on-chip 32 kHz oscillator, selectable 50/60 Hz input, and separate V_{DD} pin for battery backup
- Six 16-bit Counter/Timers with prescalers and direct input/output drive
- Watchdog Timer (WDT)
- 24 bits of general-purpose input/output (GPIO)
- JTAG and ZDI debug interfaces
- 100-pin LQFP package
- 3.0 V to 3.6 V supply voltage with 5 V tolerant inputs
- Standard operating temperature range: 0 ºC to +70 ºC

Note: *All signals with an overline are active Low. For example, B/$\overline{W}$, for which WORD is active Low, and $\overline{B}$/W, for which BYTE is active Low.*

Block Diagram

Figure 1 displays a block diagram of the eZ80F92 Flash Module.

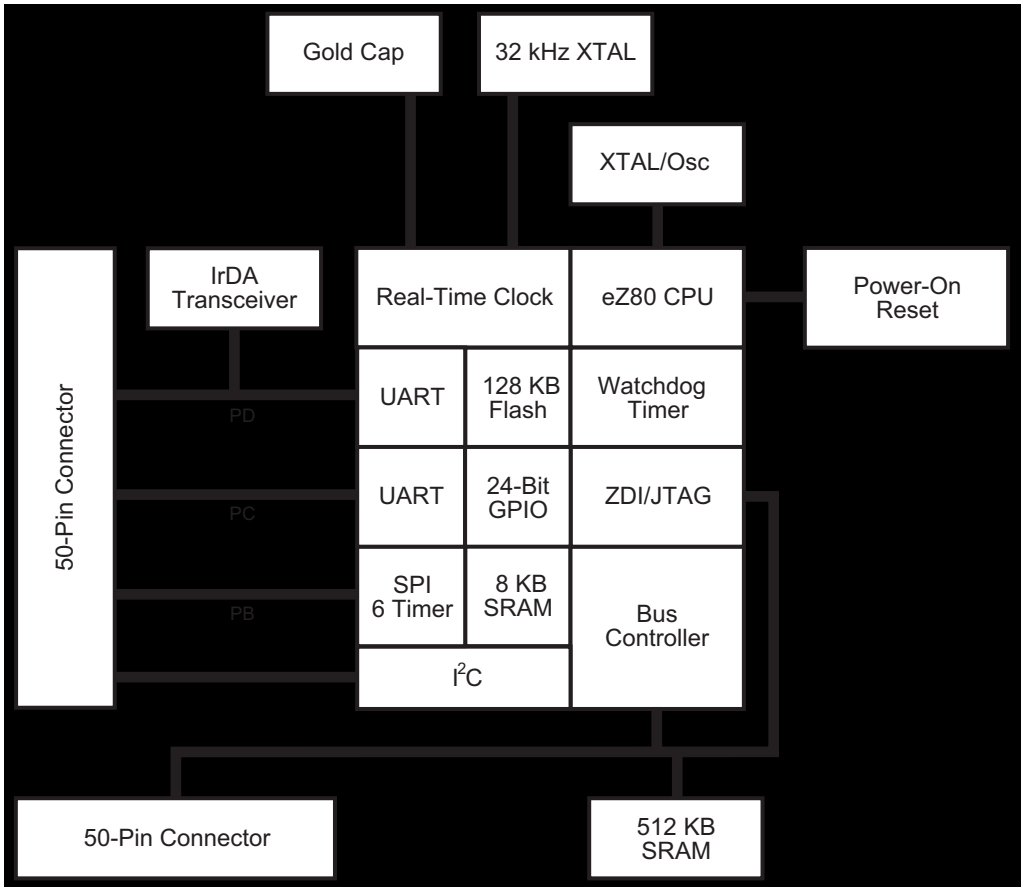


Figure 1. eZ80F92 Flash Module Functional Block Diagram

Pin Description

Peripheral Bus Connector

Figure 2 displays the pin layout of the eZ80F92 Flash Module's I/O Connector (JP1) in the 50-pin package. Table 2 on page 7 lists the pins and their functions.

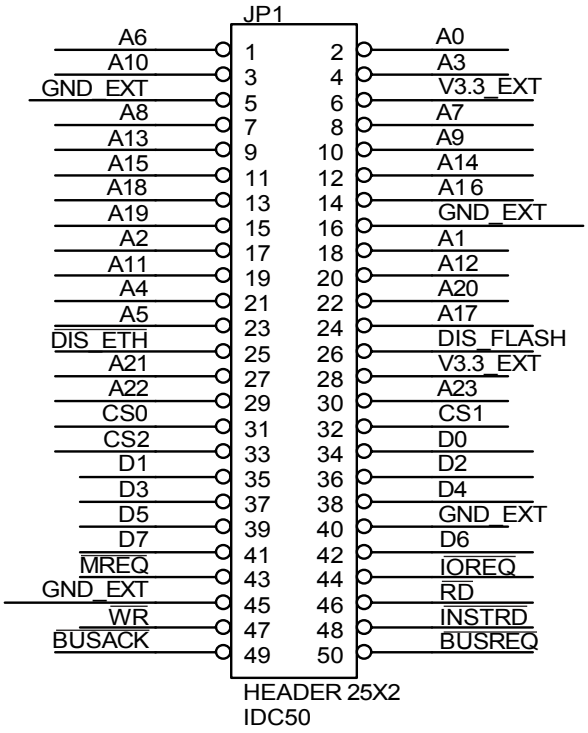


Figure 2. eZ80F92 Flash Module Peripheral Bus Connector Pin Configuration

Table 2. eZ80F92 Flash Module Peripheral Bus Connector Pin Identification*

Pin No.	Symbol	Pull Up/Down*	Signal Direction	Comments
1	A6		Bidirectional	
2	A0		Bidirectional	
3	A10		Bidirectional	
4	A3		Bidirectional	
5	GND			V_{SS}/Ground (0 V).
6	V_{DD}			3.3 V Supply Input Pin.
7	A8		Bidirectional	
8	A7		Bidirectional	
9	A13		Bidirectional	
10	A9		Bidirectional	
11	A15		Bidirectional	
12	A14		Bidirectional	
13	A18		Bidirectional	
14	A16		Bidirectional	
15	A19		Bidirectional	
16	GND			V_{SS}/Ground (0 V).
17	A2		Bidirectional	
18	A1		Bidirectional	
19	A11		Bidirectional	
20	A12		Bidirectional	
21	A4		Bidirectional	
22	A20		Bidirectional	
23	A5		Bidirectional	
24	A17		Bidirectional	
25	$\overline{\text{DIS\_ETH}}$	PU 10 kΩ	Input	This pin is not used on the eZ80F92 Flash Module. However, it is connected to the pad of the CS8900 EMAC footprint.
26	$\overline{\text{DIS\_FLASH}}$	PU 10 kΩ	Input	This pin is not used on the eZ80F92 Flash Module. However, it is connected to the pad of the external Flash footprint.

Table 2. eZ80F92 Flash Module Peripheral Bus Connector Pin Identification* (Continued)

Pin No.	Symbol	Pull Up/Down*	Signal Direction	Comments
27	A21		Bidirectional	
28	V_{DD}			3.3 V supply input pin.
29	A22		Bidirectional	
30	A23		Bidirectional	
31	$\overline{CS0}$		Output	
32	$\overline{CS1}$		Output	
33	$\overline{CS2}$		Output	
34	D0	PU 4k7	Bidirectional	
35	D1	PU 4k7	Bidirectional	
36	D2	PU 4k7	Bidirectional	
37	D3	PU 4k7	Bidirectional	
38	D4	PU 4k7	Bidirectional	
39	D5	PU 4k7	Bidirectional	
40	GND			V_{SS}/Ground (0 V).
41	D7	PU 4k7	Bidirectional	
42	D6		Bidirectional	
43	$\overline{MREQ}$		Bidirectional	
44	$\overline{IORQ}$		Bidirectional	
45	GND			V_{SS}/Ground (0 V).
46	$\overline{RD}$		Bidirectional	
47	$\overline{WR}$		Bidirectional	
48	$\overline{INSTRD}$		Output	
49	$\overline{BUSACK}$		Output	
50	$\overline{BUSREQ}$	PU 2k2	Input	

* External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7, and A0–A23 should be below 10 pF to satisfy timing requirements for the CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the eZ80CLK output can be deactivated via software in the eZ80F92 Peripheral Power-Down Register. All inputs are CMOS level 3.3 V (5 V tolerant), except otherwise noted.

I/O Connector

Figure 3 displays the pin layout of the eZ80F92 Flash Module's I/O Connector (JP2) in the 50-pin package. Table 3 on page 9 lists the pins and their functions.

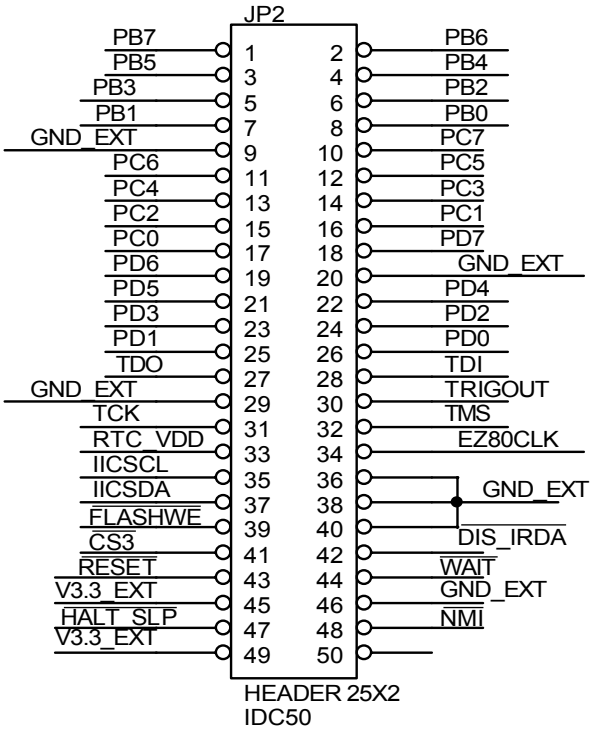


Figure 3. eZ80F92 Flash Module I/O Connector Pin Configuration

Table 3. eZ80F92 Flash Module I/O Connector Pin Identification*

Pin No.	Symbol	Pull Up/Down	Signal Direction	Comments
1	PB7		Bidirectional	
2	PB6		Bidirectional	
3	PB5		Bidirectional	
4	PB4		Bidirectional	
5	PB3		Bidirectional	
6	PB2		Bidirectional	
7	PB1		Bidirectional	

Table 3. eZ80F92 Flash Module I/O Connector Pin Identification* (Continued)

Pin No.	Symbol	Pull Up/Down	Signal Direction	Comments
8	PB0		Bidirectional	
9	GND			V_{SS}/Ground (0 V).
10	PC7		Bidirectional	
11	PC6		Bidirectional	
12	PC5		Bidirectional	
13	PC4		Bidirectional	
14	PC3		Bidirectional	
15	PC2		Bidirectional	
16	PC1		Bidirectional	
17	PC0		Bidirectional	
18	PD7		Bidirectional	
19	PD6		Bidirectional	
20	GND			V_{SS}/Ground (0 V).
21	PD5		Bidirectional	
22	PD4	PD 4k7	Bidirectional	
23	PD3		Bidirectional	
24	PD2		Bidirectional	
25	PD1		Bidirectional	
26	PD0		Bidirectional	
27	TDO		Output	JTAG Data Output pin.
28	TDI/ZDA		Input	JTAG Data Input pin.
	ZDA		Bidirectional	ZDI Data I/O.
29	GND			V_{SS}/Ground (0 V).
30	TRIGOUT		Output	Active High trigger event indicator.
31	TCK	PU 10 kΩ	Input	JTAG Input. High on reset enables ZDI mode; Low on reset enables OCI debug.
32	TMS	PU 10 kΩ	Input	JTAG Test Mode Select Input.
33	RTC_V_{DD}			RTC supply from GoldCap (or external battery).
34	EZ80CLK		Output	20 MHz synchronous CPU clock output.

Table 3. eZ80F92 Flash Module I/O Connector Pin Identification* (Continued)

Pin No.	Symbol	Pull Up/Down	Signal Direction	Comments
35	SCL	PU 4k7	Bidirectional	I^2C Bus Clock.
36	GND			V_{SS}/Ground (0 V).
37	SDA	PU 4k7	Bidirectional	I^2C Data Clock.
38	GND			V_{SS}/Ground (0 V).
39	$\overline{\text{FlashWE}}$	PU 10 kΩ	Input	This pin has no function on the eZ80F92 Flash Module. It is pulled up to V_{DD} and a connection is available on the external Flash memory pads.
40	GND			V_{SS}/Ground (0V).
41	CS3		Output	Chip select for onboard or external devices; CMOS output 3.3 V.
42	$\overline{\text{DIS\_IRDA}}$	PU 10 kΩ	Input	Low disables onboard IRDA transceiver to use PD0/ PD1 UART pins externally.
43	$\overline{\text{RESET}}$	PU 2k2	Bidirectional	Reset Output from module or push-button reset.
44	$\overline{\text{WAIT}}$	PU 2k2	Input	Driving the $\overline{\text{WAIT}}$ pin Low forces the CPU to provide additional clock cycles for an external peripheral or external memory to complete its Read or Write operation.
45	V_{DD}			3.3 V supply input pin.
46	GND			V_{SS}/Ground (0 V).
47	$\overline{\text{HALT\_SLP}}$		Output, Active Low	A Low on this pin indicates that the CPU enters either HALT or SLEEP mode because of execution of either a HALT or SLP instruction.
48	$\overline{\text{NMI}}$	PU 10 kΩ	Schmitt_Trigger Input, Active Low	The $\overline{\text{NMI}}$ input is a higher priority input than the maskable interrupts. It is always recognized at the end of an instruction, regardless of the state of the interrupt enable control bits. This input includes a Schmitt_Trigger to allow RC rise times. This external $\overline{\text{NMI}}$ signal is combined with an internal $\overline{\text{NMI}}$ signal generated from the WDT block before being connected to the $\overline{\text{NMI}}$ input of the CPU.
49	V_{DD}			3.3 V supply input pin.

Table 3. eZ80F92 Flash Module I/O Connector Pin Identification* (Continued)

Pin No.	Symbol	Pull Up/Down	Signal Direction	Comments
50	Reserved			

* External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7, and A0–A23 should be below 10 pF to satisfy timing requirements for the CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the eZ80CLK output can be deactivated via software in the eZ80F91 Peripheral Power-Down Register. All inputs are CMOS level 3.3 V (5 V tolerant), except otherwise noted.

Onboard Component Description

Logic-Level I/Os

The I/O connector features 24 general-purpose 3.3 V CMOS I/O pins that can be used as outputs or inputs interfacing to external logic. All I/Os are 5 V tolerant. Some of the GPIO pins support dual mode functions (SPI, Timer I/O, UARTs, and bit I/O with edge- or level-triggered interrupt functions on each pin). For more information on eZ80F92 dual modes, refer to *eZ80F92/eZ80F93 Product Specification (PS0153)*.

Onboard Battery Backup

An onboard 0.1 F capacitor (GoldCap) is used to bridge power outages of 2–4 hours if the power supply to the module is disconnected. The capacitor is charged to 3.1 V during normal operation and is discharged through the on-chip RTC. The V_{RTC} pin is available on the I/O connector of the module to connect external components to a power supply or to a larger GoldCap.

Caution: *Do not connect a Lithium Battery to the GoldCap capacitor, because onboard charging circuitry for the capacitor can destroy the lithium battery.*

Memory

The eZ80F92 Flash Module offers external SRAM memory and Flash memories. The wait states selectable in the eZ80F92 MCU's support memory operations, as described in this section.

Wait States

To ensure that valid data is read from or written to slower memories, a number of wait states must be inserted into the memory or I/O access operations by the controller. The number of wait states that are required should be added by programming the chip select control registers. To calculate the minimum number of wait states required, see Table 4.

Table 4. Chip Frequency to Wait State Cycle Time Calculation

MHz	Cycle Time
12	83.3 ns
20	50.0 ns

Static RAM

The eZ80F92 Flash Module features 512 KB of fast SRAM. Access speed is typically 50 ns, allowing zero-wait-state operation at 20 MHz. With the CPU at 20 MHz, SRAM can be accessed with zero wait states in eZ80® mode. CS1_CTL (chip select $\overline{CS1}$) can be set to 08h (no wait states).

Flash Memory

The eZ80F92 Flash Module allows NOR Flash memories between 4 megabits (512 KB) and 32 megabits (4 MB) to be added. The chips are housed in wide TSOP40 cases. Flash ROM access times are 55 ns to 150 ns; typically 90 ns. The Flash Boot Loader, application code, and user configuration data are held permanently in NOR Flash memory.

NOR Flash should be operated in Intel bus mode to satisfy setup and hold times and to prevent bus contention with a WRITE cycle that could possibly follow. For proper CPU operation at 20 MHz, first set the bus mode control register CS0_BMC (I/O address 0xF0h) to 82h, then set the Chip Select Control register CS0_CTL (I/O address 0xAAh) to 08h. These settings select Intel Bus Mode with two system clocks per bus cycle and zero wait states.

The eZ80F92 Flash Module features the following memory configurations:

- On-chip SRAM: 8 KB
- Off-chip SRAM: 512 KB
- On-chip Flash: 128 KB
- Off-chip Flash: 1 MB

IrDA Transceiver

An onboard IrDA transceiver (ZHX1810) is connected to PD0 (TX), PD1 (RX), and PD2 (Shutdown, R_SD). The IrDA transceiver is of the LED type 870 nm Class 1.

The receiver supply current is 90 µA to150 µA and the transmitter supply current is 260 mA when the LED is active. The IrDA transceiver is accessible via the IrDA controller attached to UART0 on the eZ80F92 device. The UART0 console and the IrDA transceiver cannot be used simultaneously.

To use the UART0 for console or to save power, the transceiver can be disabled by the software or by an off-board signal when using the proper jumper selection. The transceiver is disabled by setting PD2 (IR_SD) High or by pulling the $\overline{DIS\_IRDA}$ pin on the I/O connector Low. The shutdown is used for power savings. To enable the IrDA transceiver, $\overline{DIS\_IRDA}$ is left floating and PD2 is set to Low.

Reset Generator

The onboard Reset Generator Chip performs reliable Power-On Reset (POR). The chip generates a reset pulse with a duration of 200 ms if the power supply drops below 2.93 V. This reset pulse ensures that the board always starts in a defined condition. The RESET pin on the I/O connector reflects the status of the RESET line. It is a bidirectional pin for resetting external peripheral components or for resetting the eZ80F92 Flash Module with a low-impedance output (for example, a 100 Ω push-button).

Serial Interface Ports

The controller contains two 16550-style UARTs with programmable baud rate generators. UART0 is typically used for console I/O, and initial boot code upload, or to connect remote peripherals that can be controlled and monitored via Ethernet. UART0 is connected to GPIO PD[0:3] on the I/O connector. There are no RS-232 level shifters on the eZ80F92 Flash Module.

Note: *Do not connect an RS-232 interface without level shifters.*

UART1 can be used for modem attachment or as a communications port to a host computer, where the embedded Ethernet module emulates an AT-style modem for internet access. UART1 does not offer onboard RS-232 level shifters.

Physical Dimensions

The size of the eZ80F92 Flash Module PCB is 64 x 64 mm. See Figure 4.

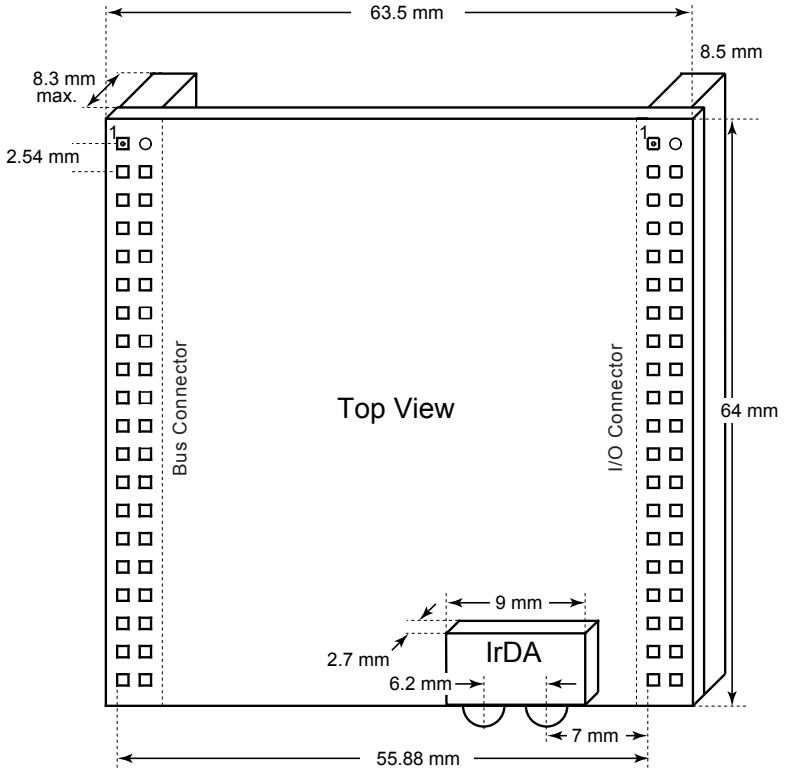


Figure 4. Dimension Drawing

Figure 5 displays a top view of the eZ80F92 Flash Module.

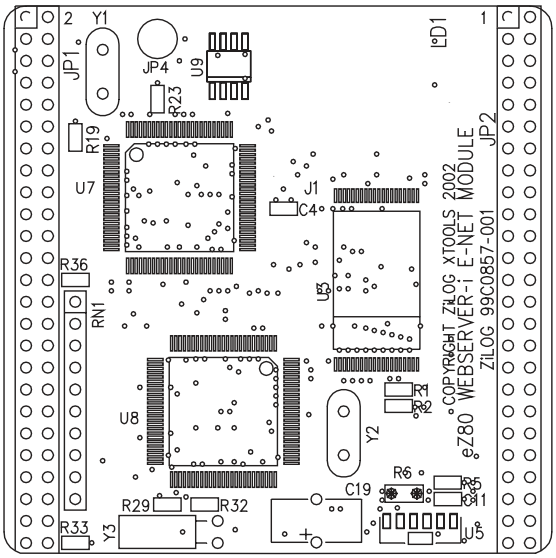


Figure 5. Top Layer

Figure 6 displays a bottom view of the eZ80F92 Flash Module.

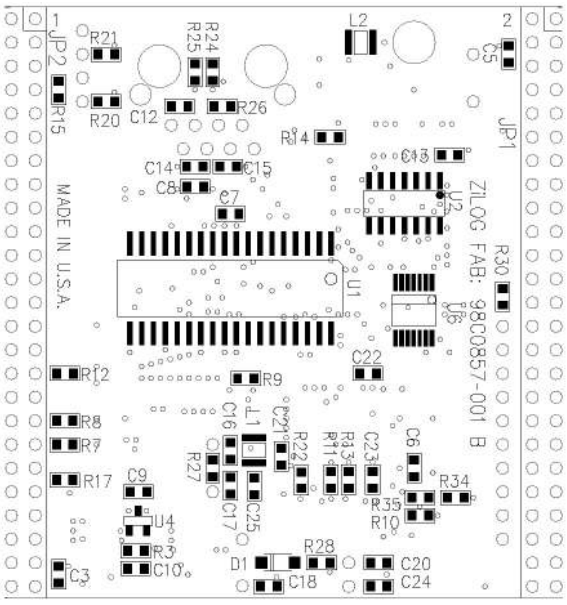
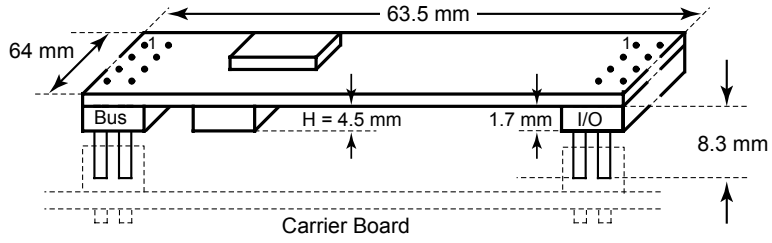


Figure 6. Bottom Layer

Mounting the Module onto the eZ80® Development Platform

The eZ80F92 Flash Module can be mounted in several positions. Depending on volume and area restrictions, it can be mounted horizontally or vertically with or without components between the connectors on the eZ80® Development Platform. Figure 7 displays examples.

Low Profile Mounting



Stacked Mounting

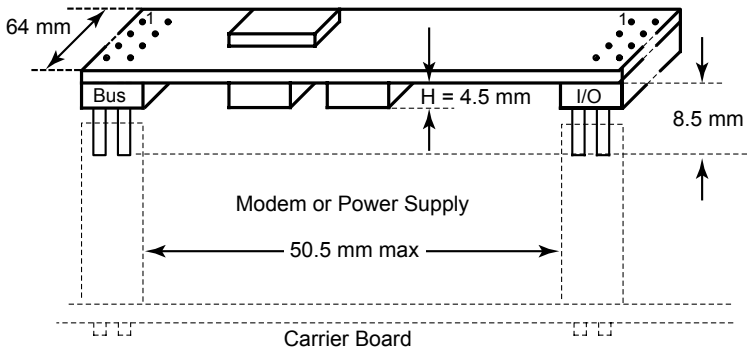


Figure 7. Mounting Examples

ESD/EMI Protection

Caution: *The eZ80F92 Flash Module is a component that is intended to be part of a system design for end-user devices. Therefore, you must take precaution to use ESD protection on the I/O pins.*

Caution: *CMOS I/Os are ESD-sensitive and must be handled with care. Handling of the module should be performed in ESD-safe environments (for example, with a wrist-wrap attached). When developing applications, you must provide for proper ESD protection on external, user-accessible I/Os (for example, suppressor arrays for the I/Os).*

The components are mounted on a multilayer PCB to provide a stable ground plane for onboard components. The module features several GND pins next to pins with higher switching frequency for short ground returns. If unused, the clock output can be separated from the module header by removing a series resistor on the module. Removing the series resistor further reduces electromagnetic emissions.

Absolute Maximum Ratings

Stresses greater than those listed in Table 5 can cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, unused inputs should be tied to one of the supply voltages (V_{DD} or V_{SS}).

Table 5. Absolute Maximum Ratings

Parameter	Min	Max	Units
Standard operating temperature	0	+70	ºC
Storage temperature	–45	+85	ºC
Operating Humidity (RH @ 50 ºC)	25%	90%	
Operating Voltage (±5%)	—	3.3	V

Power Supply

The eZ80F92 Flash Module requires a regulated external 3.3 V DC/0.5 A power supply. You may use a Low Dropout Regulator (LDO) to get 3.3 V from 5 V or use the following switcher circuit to generate 3.3 V from unregulated 10 V to 28 V power supply.

Power connections conventional description is provided in the following table:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Figure 8 displays two power supply examples.

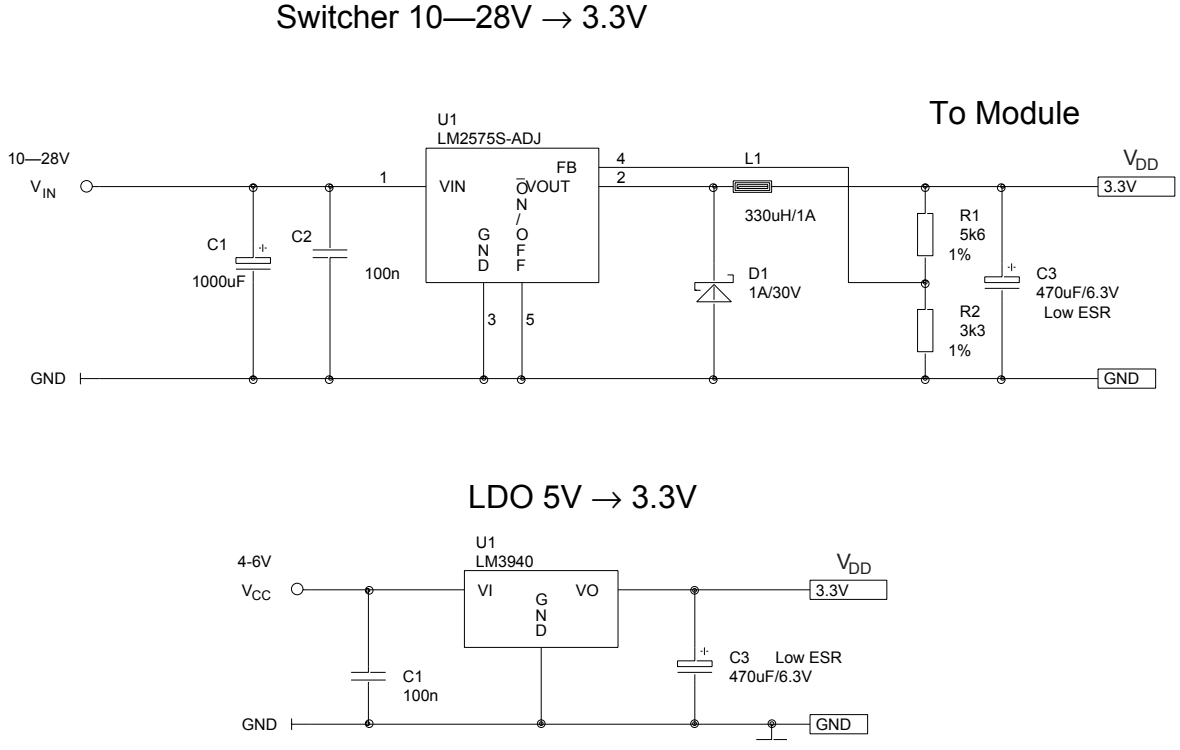


Figure 8. Power Supply Examples

Schematics

Figure 9 through Figure 17 on page 29 displays the layout of the eZ80F92 Flash Module. Ethernet and external Flash circuiting devices are not loaded on the eZ80F92 Flash Module. However, these devices appear in the following schematics for reference.

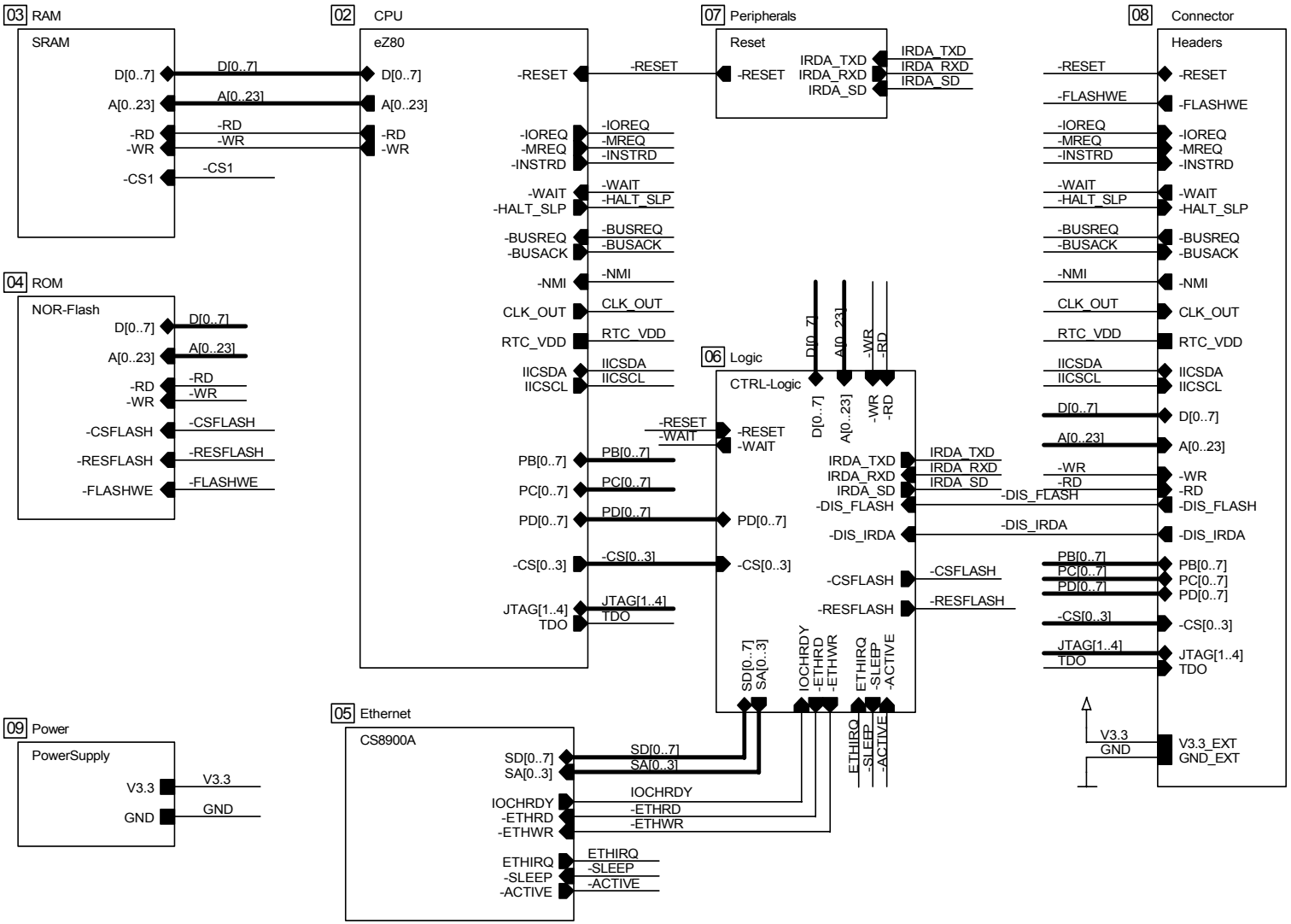


Figure 9. eZ80F92 Flash Module Schematics—Top Level

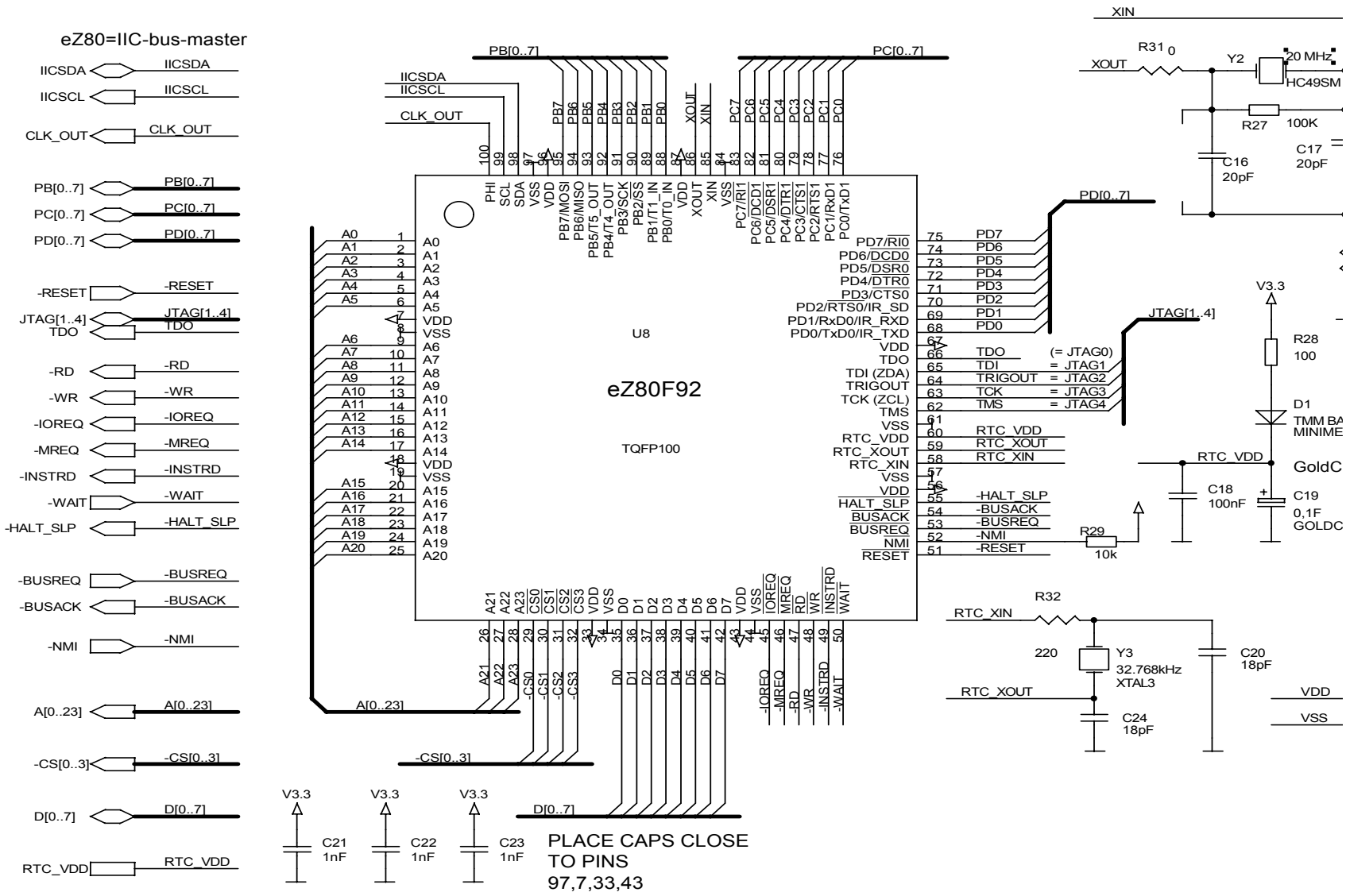


Figure 10. eZ80F92 Flash Module Schematics—100-Pin QFP eZ80F92 Device

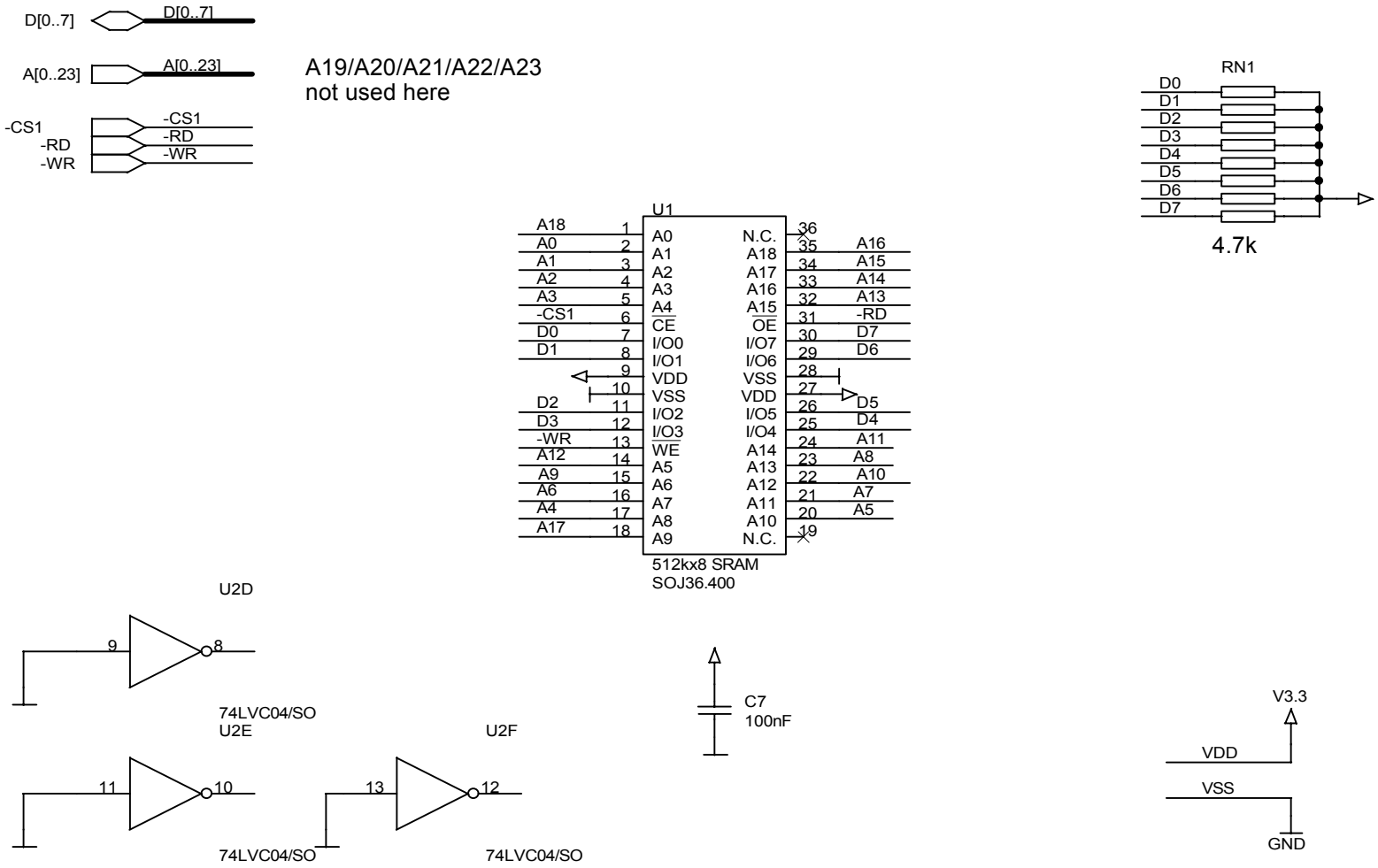


Figure 11. eZ80F92 Flash Module Schematics—36-Pin SRAM Device

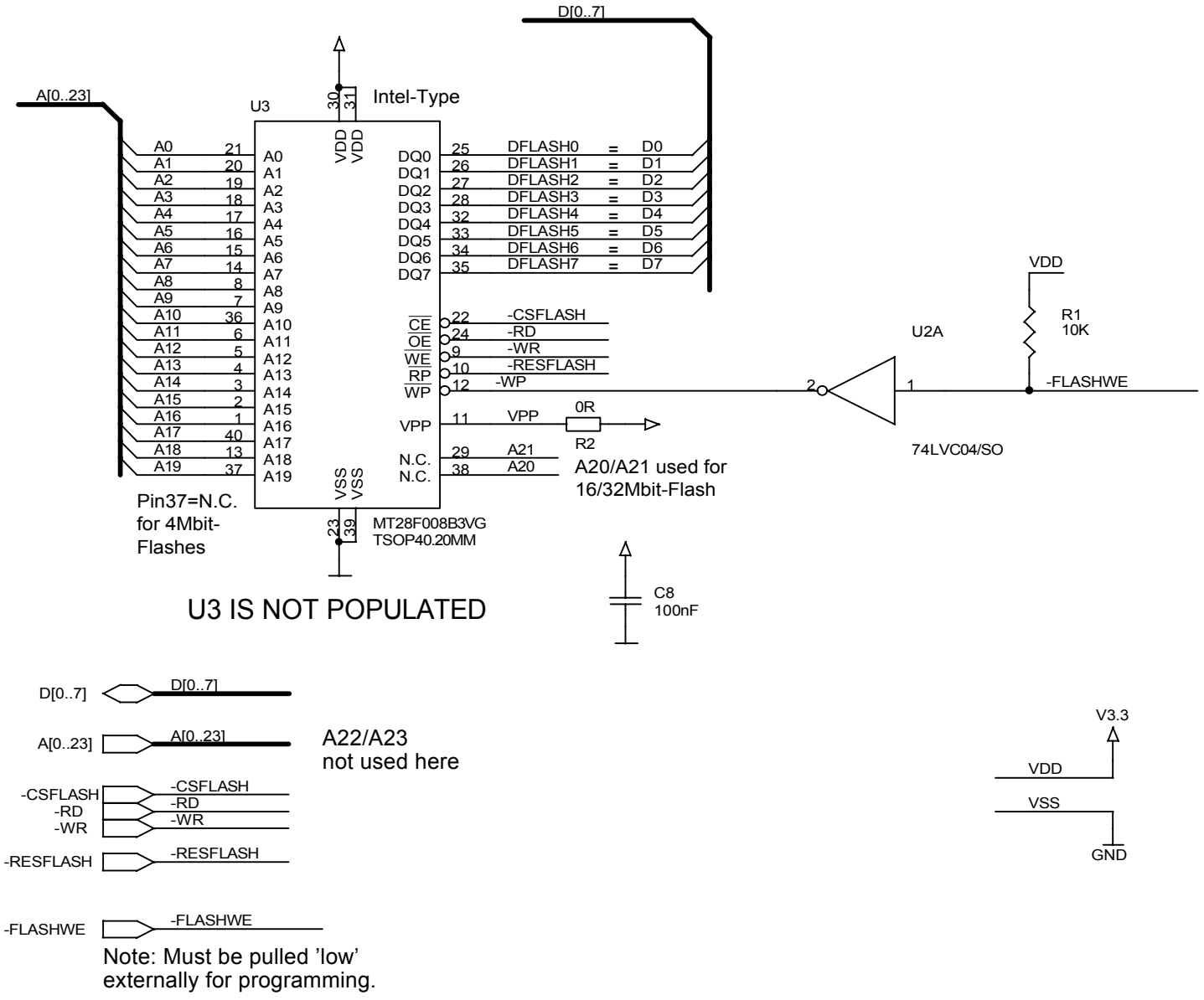


Figure 12. eZ80F92 Flash Module Schematics—NOR Flash Device

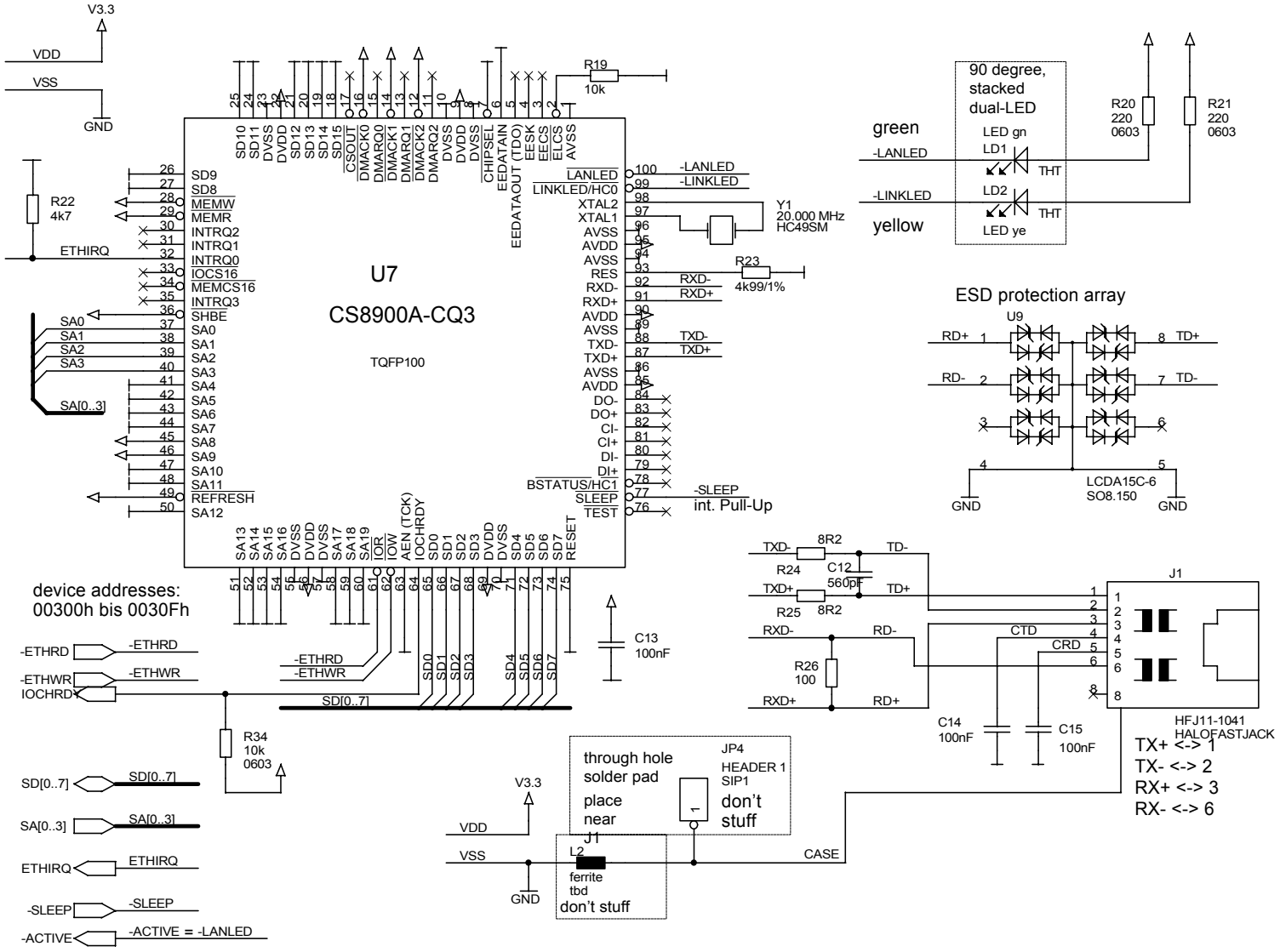


Figure 13. eZ80F92 Flash Module Schematics—Module

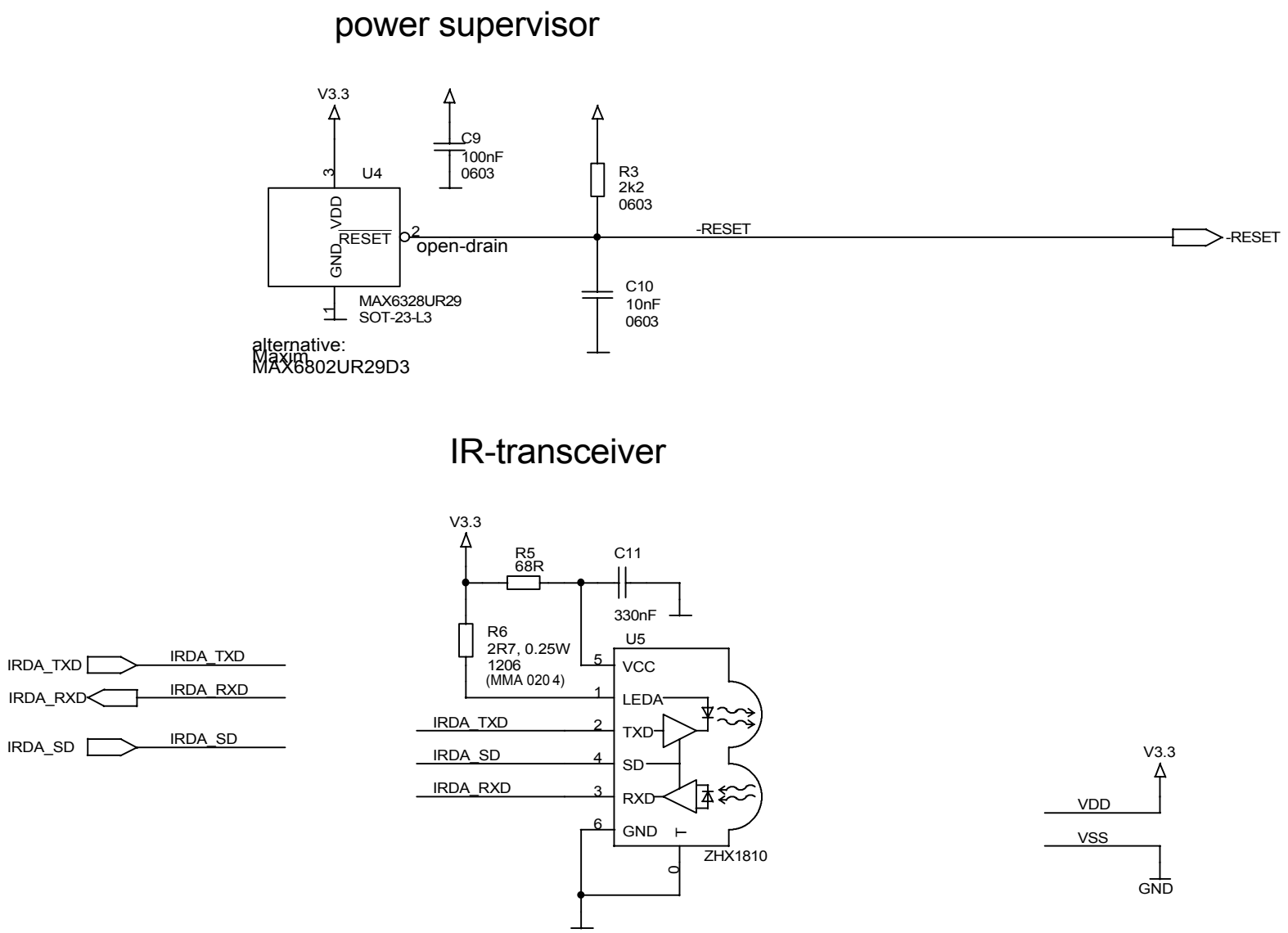


Figure 14. eZ80F92 Flash Module Schematics—IrDA Reset

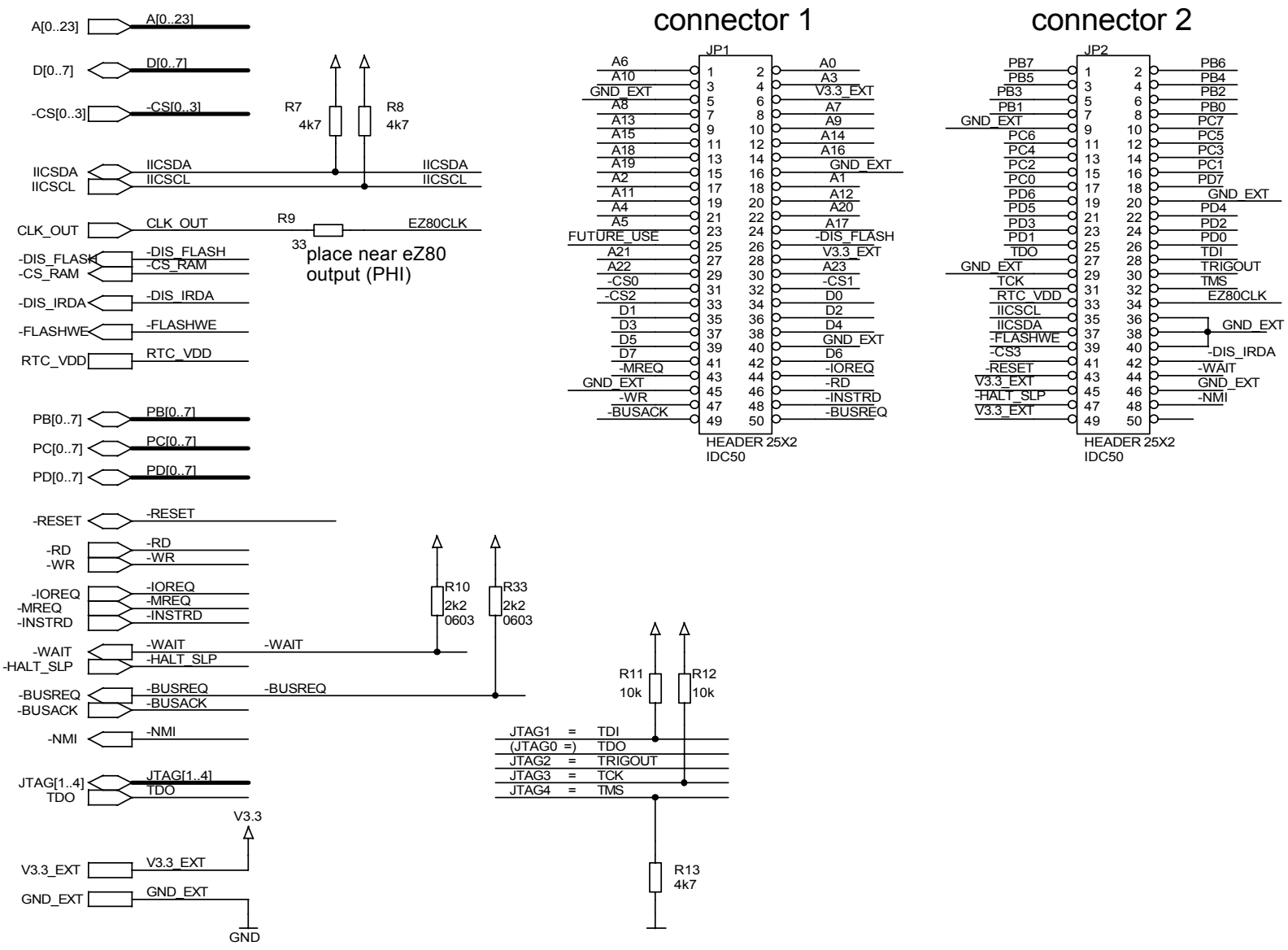
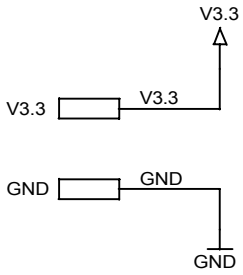
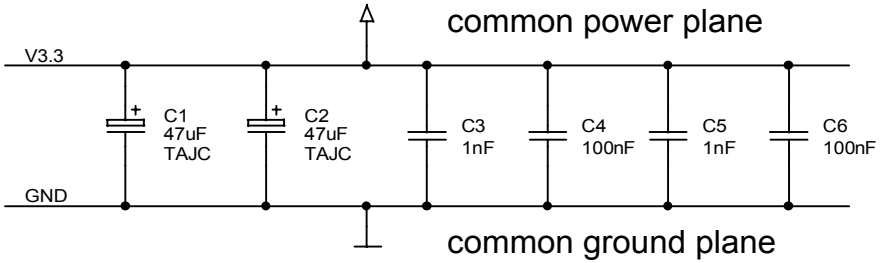


Figure 15. eZ80F92 Flash Module Schematics—Headers





no power supply on board!

Input: VDD(=V3.3) = 3.3V –5%

Power: Pmax = 1.6W
Ptyp = 0.4W

Current: Imax = 200mA (IrDA not in use)
Imax = 460mA (IrDA in use)
Ityp = 100mA

PCB1

E-NET Module Rev.B
98Cxxxx-xxx

for test purposes

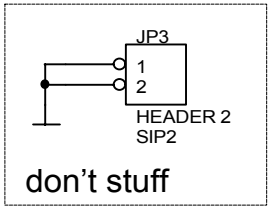


Figure 16. eZ80F92 Flash Module Schematics—Power Supply

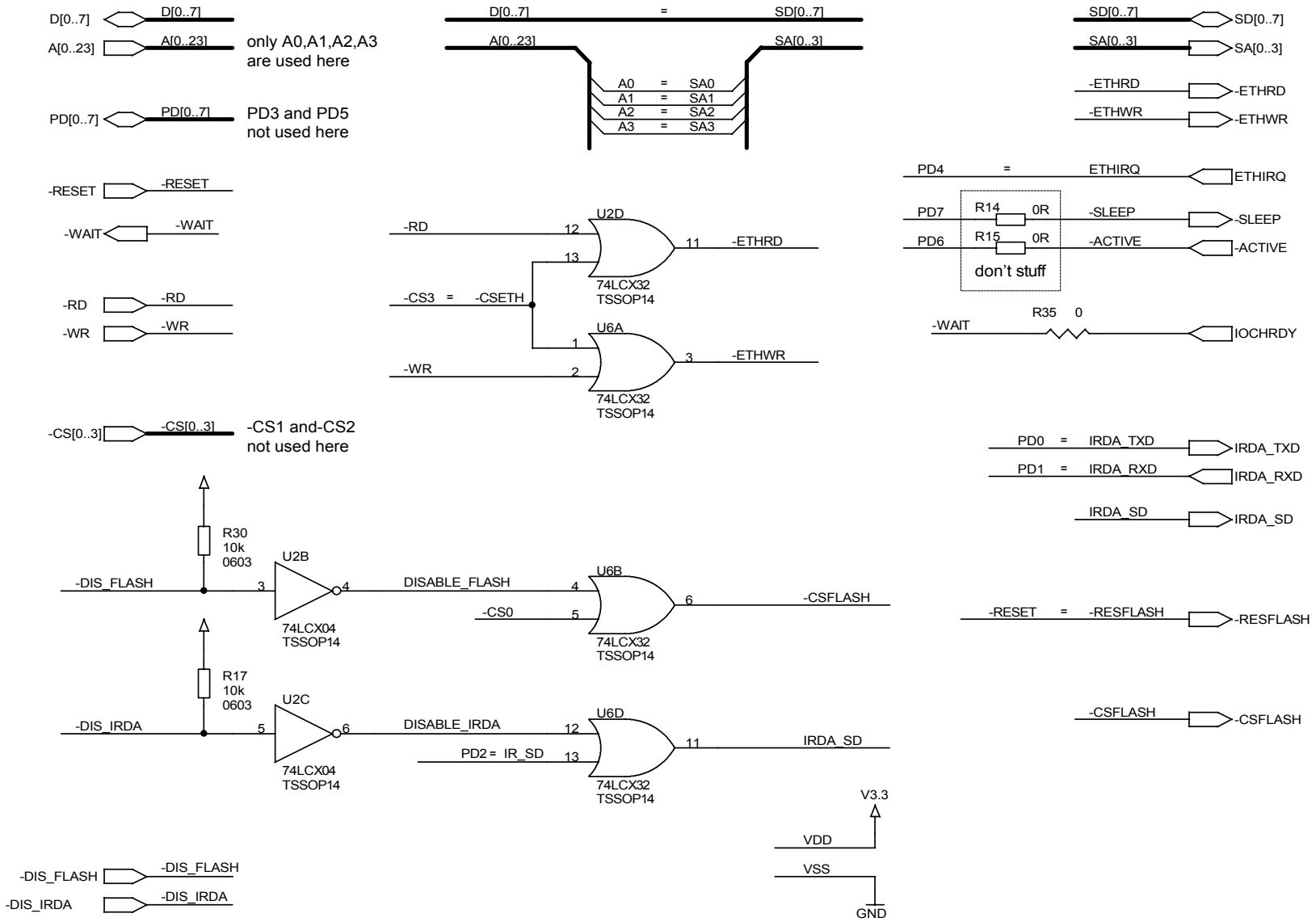


Figure 17. eZ80F92 Flash Module Schematics—Control Logic

Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.