LME49723 Dual High Fidelity Audio Operational Amplifier

Check for Samples: LME49723

FEATURES

- **Easily Drives 600Ω Loads**
- **Optimized for Superior Audio Signal Fidelity**
- **Output Short Circuit Protection**
- **PSRR and CMRR Exceed 100dB (typ)**
- **SOIC Package**

APPLICATIONS

- **High Quality Audio Amplification**
- **High Fidelity Preamplifiers**
- **High Fidelity Multimedia**
- **Phono Pre Amps**
- **High Performance Professional Audio**
- **High Fidelity Equalization and Crossover Networks**
- **High Performance Line Drivers**
- **High Performance Line Receivers**
- **High Fidelity Active Filters**

KEY SPECIFICATIONS

- **Power Supply Voltage Range: ±2.5 to ±17 V**
- **THD+N (A_V = 1, V_{OUT} = 3V_{RMS}, f_{IN} = 1kHz)**
  - **R_L = 2kΩ: 0.0002 % (typ)**
  - **R_L = 600Ω: 0.0002 % (typ)**
- **Input Noise Density: 3.6 nV/$\sqrt{Hz}$ (typ)**
- **Slew Rate: ±8 V/μs (typ)**
- **Gain Bandwidth Product: 17 MHz (typ)**
- **Open Loop Gain (R_L = 600Ω): 105 dB (typ)**
- **Input Bias Current: 200 nA (typ)**
- **Input Offset Voltage: 0.3 mV (typ)**

DESCRIPTION

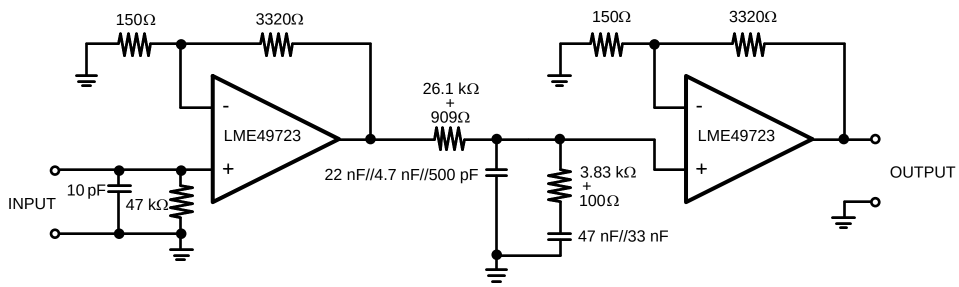
The LME49723 is part of the ultra-low distortion, low noise, high slew rate operational amplifier series optimized and fully specified for high performance, high fidelity applications. Combining advanced leading-edge process technology with state-of-the-art circuit design, the LME49723 audio operational amplifiers deliver superior audio signal amplification for outstanding audio performance. The LME49723 combines extremely low voltage noise density (3.6nV/$\sqrt{Hz}$) with vanishingly low THD+N (0.0002%) to easily satisfy the most demanding audio applications. To ensure that the most challenging loads are driven without compromise, the LME49723 has a high slew rate of ±20V/μs and an output current capability of ±26mA. Further, dynamic range is maximized by an output stage that drives 2kΩ loads to within 1V of either power supply voltage and to within 1.4V when driving 600Ω loads.

The LME49723's outstanding CMRR (100dB), PSRR (100dB), and V_{OS} (0.3mV) give the amplifier excellent operational amplifier DC performance.

The LME49723 has a wide supply range of ±2.5V to ±17V. Over this supply range the LME49723's input circuitry maintains excellent common-mode and power supply rejection, as well as maintaining its low input bias current. The LME49723 is unity gain stable.

The LME49723 is available in an 8–lead narrow body SOIC package. Demonstration boards are available for each package.

TYPICAL APPLICATION



Note: 1% metal film resistors, 5% polypropylene capacitors

Figure 1. Passively Equalized RIAA Phono Preamplifier

CONNECTION DIAGRAM

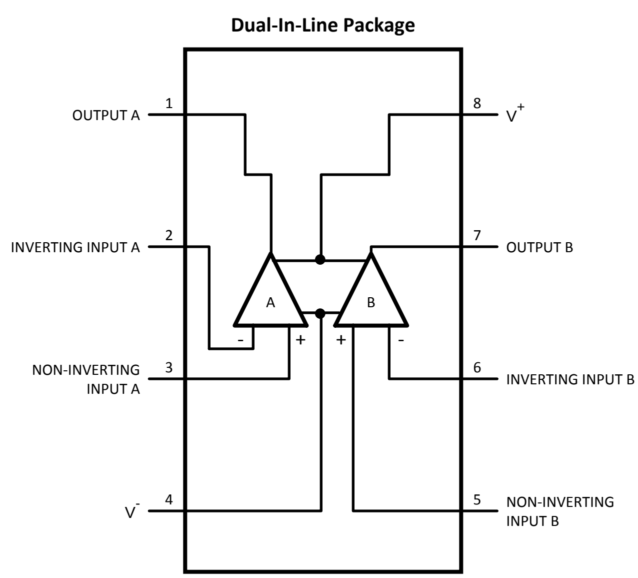


Figure 2. SOIC Package
See Package Number D0008A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

Power Supply Voltage ($V_S = V^+ - V^-$)	36V
Storage Temperature	−65°C to 150°C
Input Voltage	(V-) - 0.7V to (V+) + 0.7V
Output Short Circuit(4)	Continuous
Power Dissipation	Internally Limited
ESD Susceptibility(5)	800V
ESD Susceptibility(6)	180V
Junction Temperature	150°C
Thermal Resistance θ_{JA} (SO)	145°C/W
Temperature Range $T_{MIN} \leq T_A \leq T_{MAX}$	–40°C ≤ T_A ≤ 85°C
Supply Voltage Range	±2.5V ≤ V_S ≤ ± 17V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
(2) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Amplifier output connected to GND, any number of amplifiers within a package.
(5) Human body model, 100pF discharged through a 1.5kΩ resistor.
(6) Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200pF cap is charged to the specified voltage and then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).

ELECTRICAL CHARACTERISTICS FOR THE LME49723(1)(2)

The specifications apply for V_S = ±15V, R_L = 2kΩ, f_{IN} = 1kHz, T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions		LME49723		Units (Limits)
				Typical(3)	Limit(4)	
THD+N	Total Harmonic Distortion + Noise	A_V = 1, V_{OUT} = $3V_{rms}$	R_L = 2kΩ	0.0002		% (max)
			R_L = 600Ω	0.0002	0.0004	
IMD	Intermodulation Distortion	A_V = 1, V_{OUT} = $3V_{RMS}$ Two-tone, 60Hz & 7kHz 4:1		0.0005		%
GBWP	Gain Bandwidth Product			19	15	MHz (min)
SR	Slew Rate			±8	±6	V/μs (min)
FPBW	Full Power Bandwidth	V_{OUT} = $1V_{P-P}$, –3dB referenced to output magnitude at f = 1kHz		4		MHz
e_n	Equivalent Input Noise Voltage	f_{BW} = 20Hz to 20kHz		0.45	0.65	μV_{RMS} (max)
	Equivalent Input Noise Density	f = 1kHz f = 10Hz		3.2 8.5	5	nV/√Hz (max)
i_n	Current Noise Density	f = 1kHz f = 10Hz		0.7 1.3		pA/√Hz
V_{OS}	Offset Voltage			±0.3	1	mV (max)
$\Delta V_{OS}/\Delta Temp$	Average Input Offset Voltage Drift vs Temperature	–40°C ≤ T_A ≤ 85°C		0.2		μV/°C
PSRR	Average Input Offset Voltage Shift vs Power Supply Voltage	ΔV_S = 20V(5)		100	95	dB (min)
ISO_{CH-CH}	Channel-to-Channel Isolation	f_{IN} = 1kHz f_{IN} = 20kHz		118 112		dB
I_B	Input Bias Current	V_{CM} = 0V		200	300	nA (max)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
(2) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) Typical specifications are specified at +25ºC and represent the most likely parametric norm.
(4) Tested limits are specified to AOQL (Average Outgoing Quality Level).
(5) PSRR is measured as follows: V_{OS} is measured at two supply voltages, ±5V and ±15V. PSRR = | 20log($\Delta V_{OS}/\Delta V_S$) |.

ELECTRICAL CHARACTERISTICS FOR THE LME49723(1)(2) (continued)

The specifications apply for V_S = ±15V, R_L = 2kΩ, f_{IN} = 1kHz, T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	LME49723		Units (Limits)
			Typical(3)	Limit(4)	
$\Delta I_{OS}/\Delta Temp$	Input Bias Current Drift vs Temperature	–40°C ≤ T_A ≤ 85°C	0.1		nA/°C
I_{OS}	Input Offset Current	V_{CM} = 0V	7	100	nA (max)
$V_{IN\text{-}CM}$	Common-Mode Input Voltage Range		±14	(V+) – 2.0 (V-) + 2.0	V (min)
CMRR	Common-Mode Rejection	–10V<Vcm<10V	100	90	dB (min)
Z_{IN}	Differential Input Impedance		30		kΩ
	Common Mode Input Impedance	–10V<Vcm<10V	1000		MΩ
A_{VOL}	Open Loop Voltage Gain	–10V<Vout<10V, R_L = 600Ω	100	98	dB (min)
		–10V<Vout<10V, R_L = 2kΩ	105		
		–10V<Vout<10V, R_L = 10kΩ	105		
V_{OUTMAX}	Maximum Output Voltage Swing	R_L = 600Ω	±13.5	±12.5	V (min)
		R_L = 2kΩ	±14.0		
		R_L = 10kΩ	±14.1		
I_{OUT}	Output Current	R_L = 600Ω, V_S = ±17V	±25	±21	mA (min)
$I_{OUT\text{-}CC}$	Instantaneous Short Circuit Current		+53 –42		mA
R_{OUT}	Output Impedance	f_{IN} = 10kHz Closed-Loop Open-Loop	 0.01 13		Ω
C_{LOAD}	Capacitive Load Drive Overshoot	100pF	16		%
I_S	Total Quiescent Current	I_{OUT} = 0mA	6.7	7.5	mA (max)

TYPICAL PERFORMANCE CHARACTERISTICS

THD+N vs Output Voltage
V_S = ±5V, R_L = 2kΩ

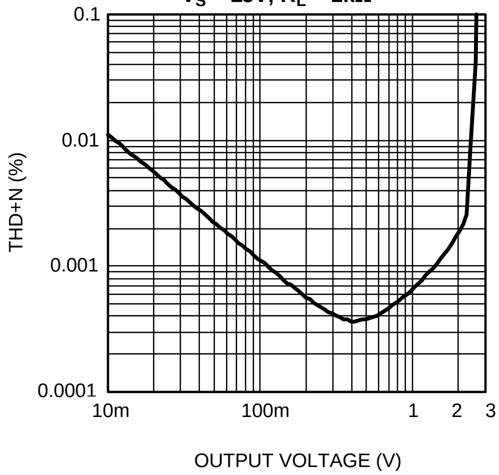


Figure 3.

THD+N vs Output Voltage
V_S = ±5V, R_L = 10kΩ

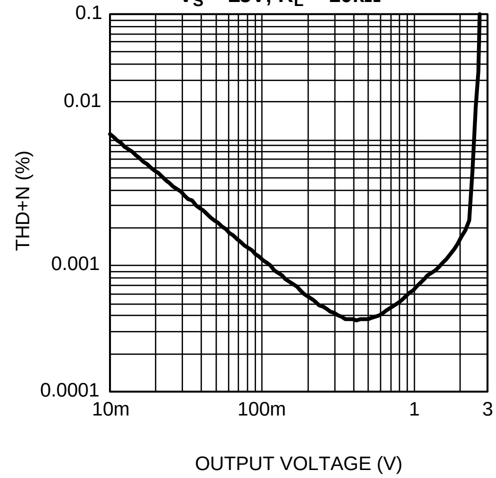


Figure 4.

THD+N vs Output Voltage
V_S = ±5V, R_L = 600Ω

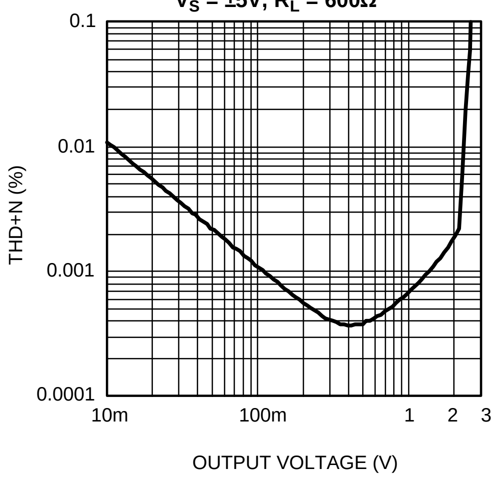


Figure 5.

THD+N vs Output Voltage
V_S = ±15V, R_L = 2kΩ

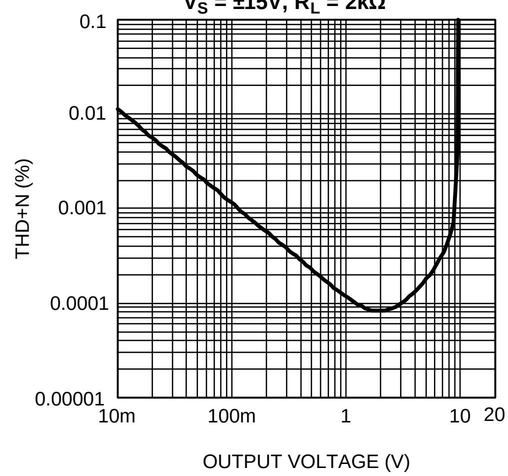


Figure 6.

THD+N vs Output Voltage
V_S = ±15V, R_L = 10kΩ

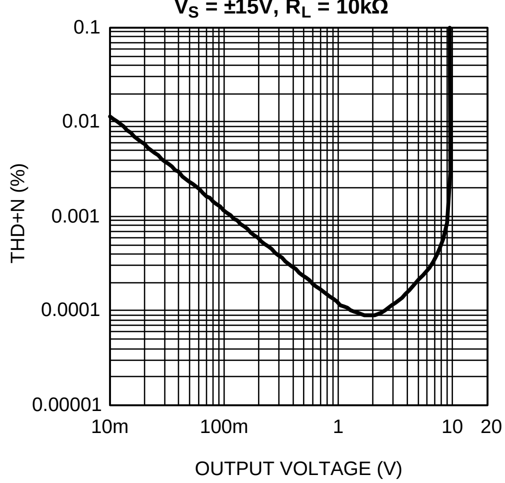


Figure 7.

THD+N vs Output Voltage
V_S = ±15V, R_L = 600Ω

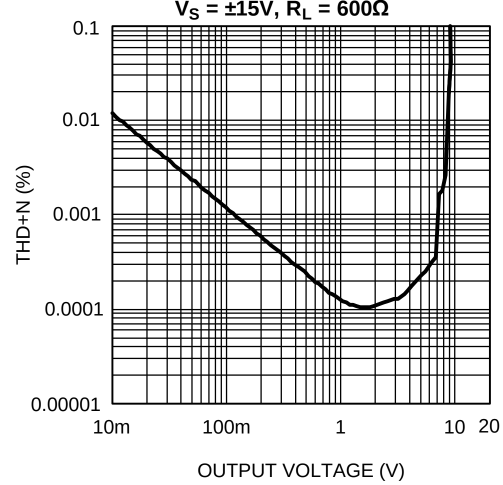


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

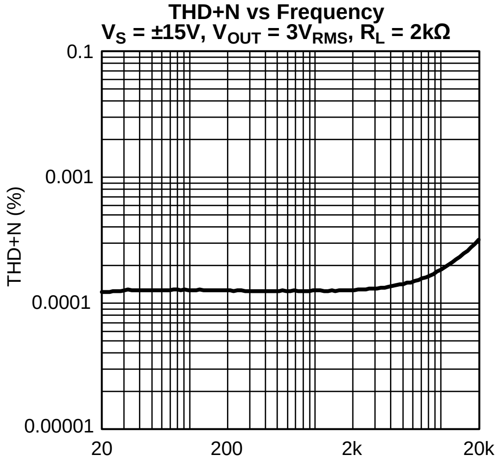


Figure 9.

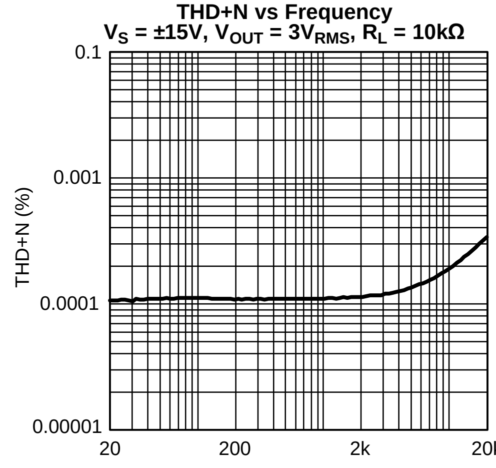


Figure 10.

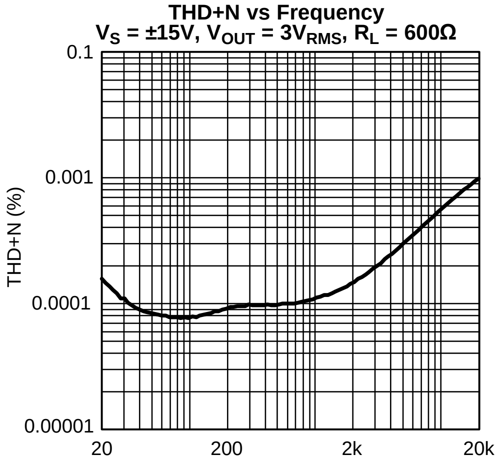
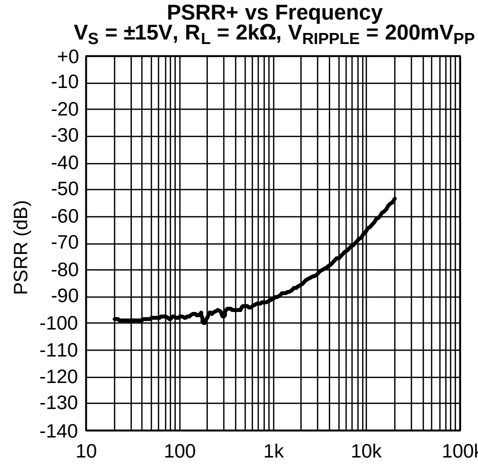


Figure 11.



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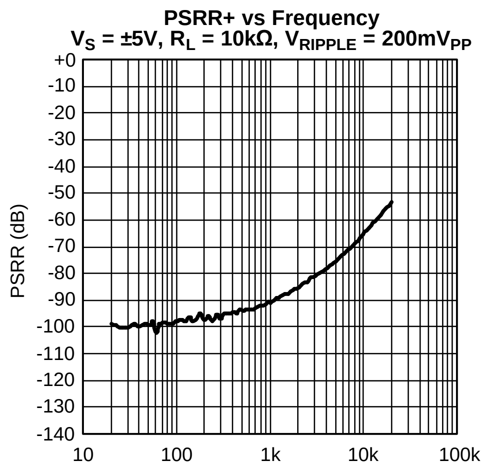

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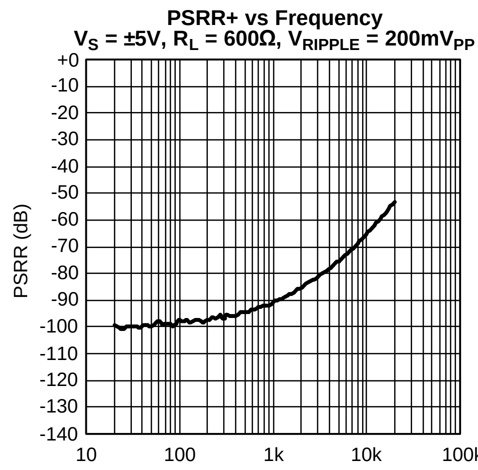


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

PSRR+ vs Frequency
V_S = ±15V, R_L = 2kΩ, V_{RIPPLE} = 200mV$_{PP}$

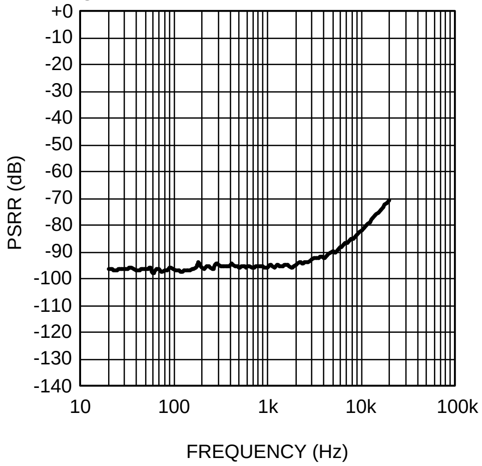


Figure 15.

PSRR+ vs Frequency
V_S = ±15V, R_L = 10kΩ, V_{RIPPLE} = 200mV$_{PP}$

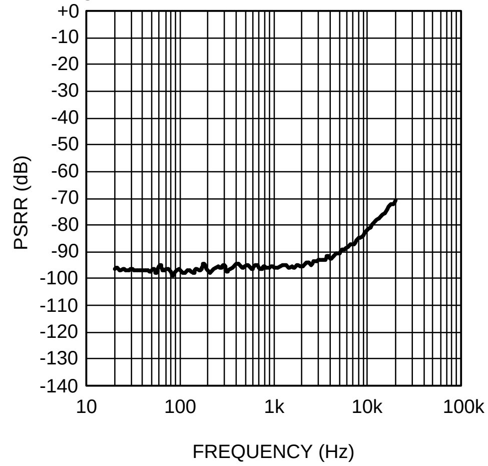


Figure 16.

PSRR+ vs Frequency
V_S = ±15V, R_L = 600Ω, V_{RIPPLE} = 200mV$_{PP}$

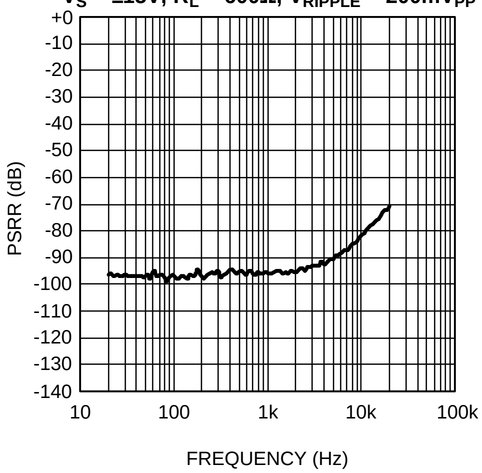


Figure 17.

PSRR- vs Frequency
V_S = ±5V, R_L = 2kΩ, V_{RIPPLE} = 200mV$_{PP}$

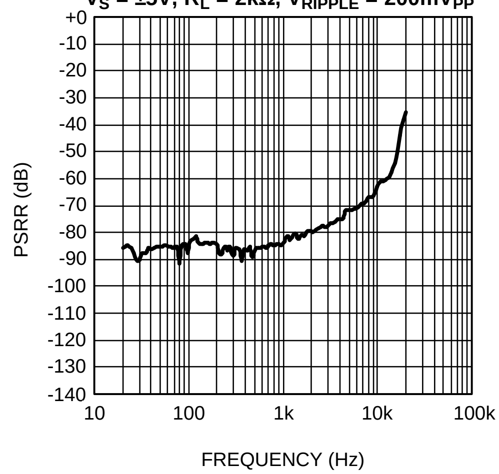


Figure 18.

PSRR- vs Frequency
V_S = ±5V, R_L = 10kΩ, V_{RIPPLE} = 200mV$_{PP}$

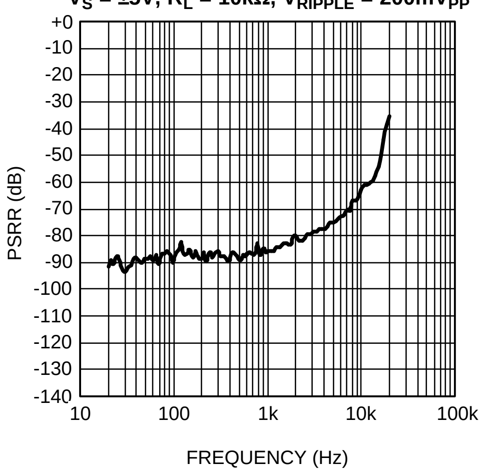


Figure 19.

PSRR- vs Frequency
V_S = ±5V, R_L = 600Ω, V_{RIPPLE} = 200mV$_{PP}$

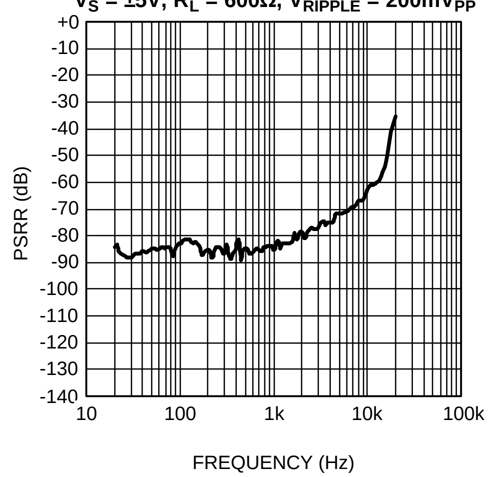


Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

PSRR- vs Frequency
V_S = ±15V, R_L = 2kΩ, V_{RIPPLE} = 200mV_{PP}

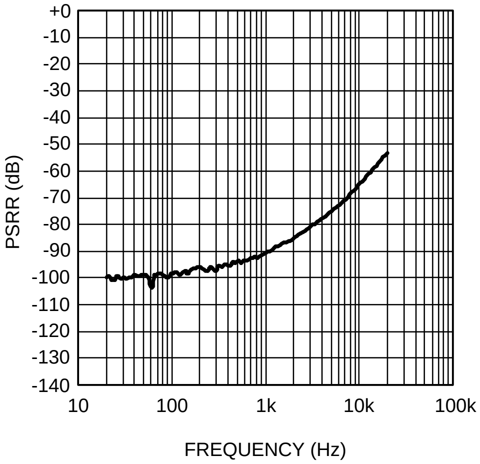


Figure 21.

PSRR- vs Frequency
V_S = ±15V, R_L = 10kΩ, V_{RIPPLE} = 200mV_{PP}

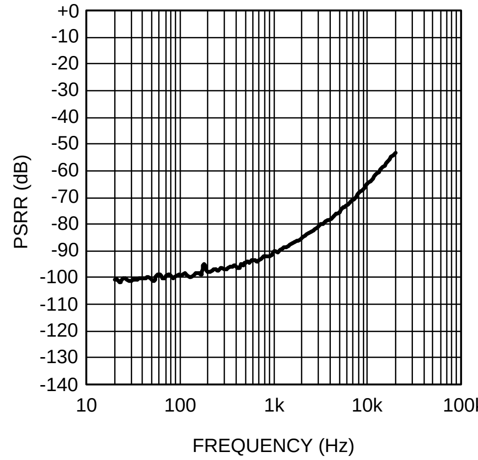


Figure 22.

PSRR- vs Frequency
V_S = ±15V, R_L = 10kΩ, V_{RIPPLE} = 200mV_{PP}

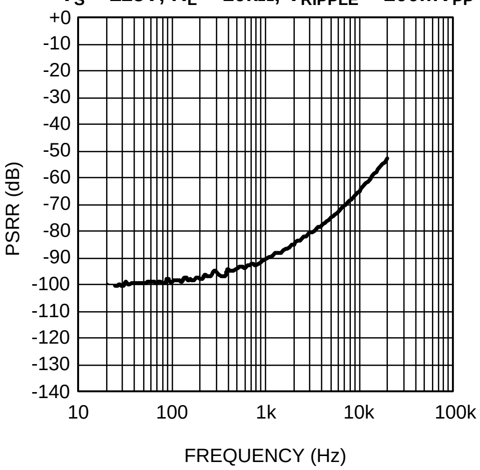


Figure 23.

CMRR vs Frequency
V_S = ±15V, R_L = 2kΩ, V_{IN} = 200mV_{PP}

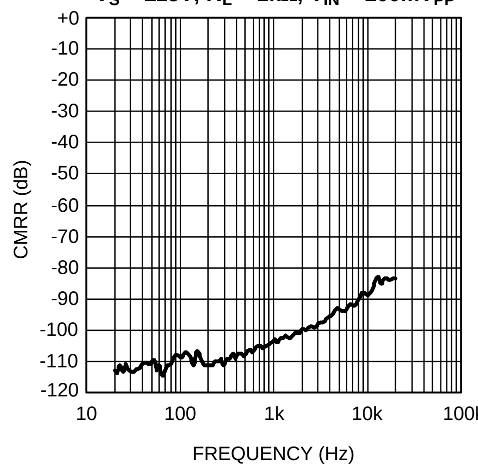


Figure 24.

CMRR vs Frequency
V_S = ±15V, R_L = 10kΩ, V_{IN} = 200mV_{PP}

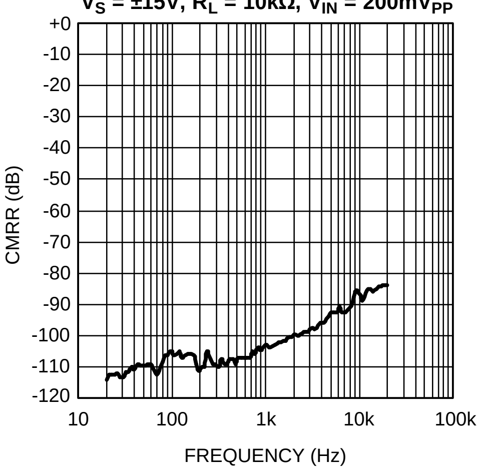


Figure 25.

CMRR vs Frequency
V_S = ±15V, R_L = 600Ω, V_{IN} = 200mV_{PP}

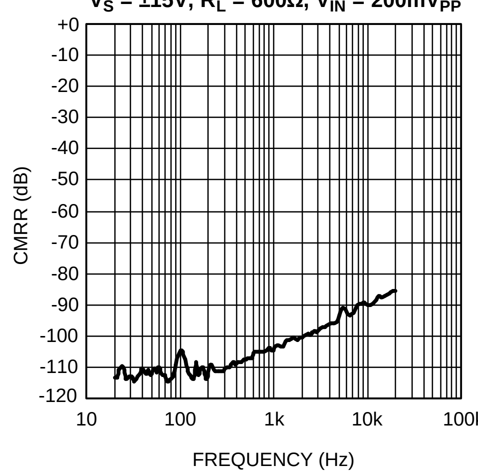
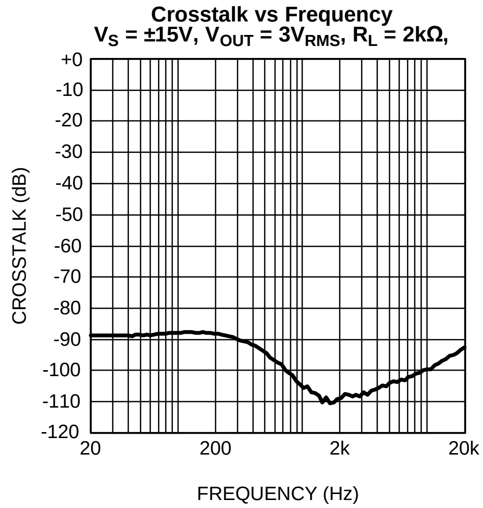


Figure 26.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)



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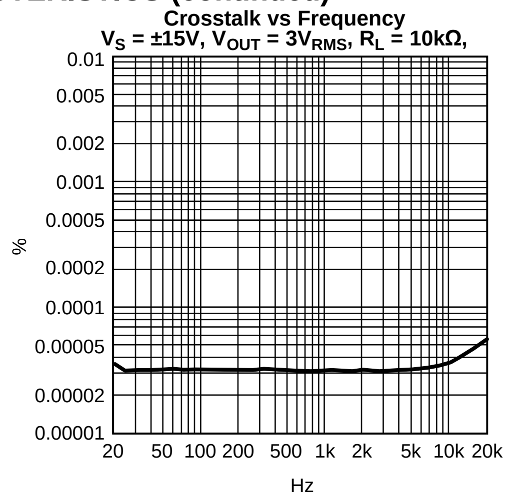
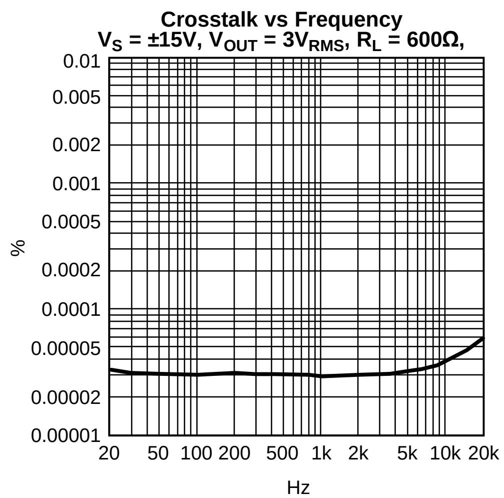


Figure 28.



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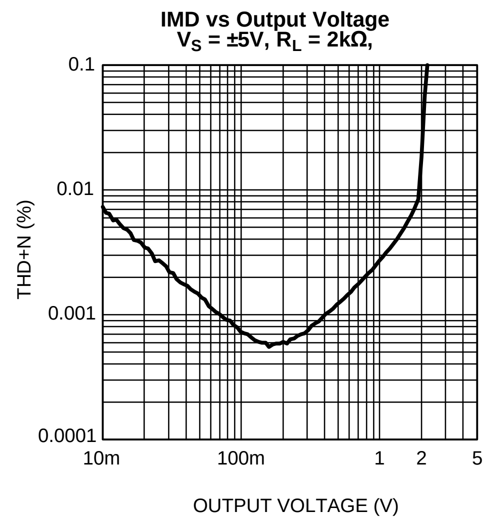

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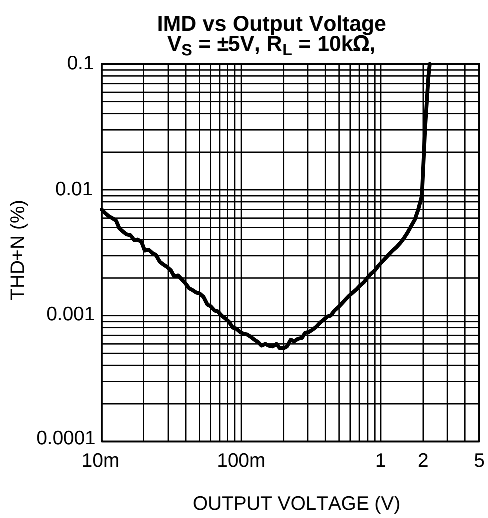

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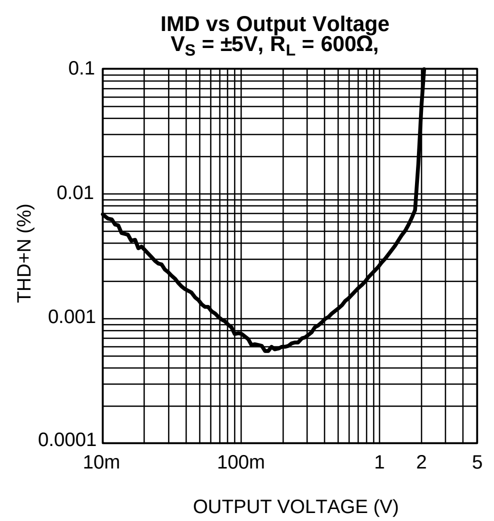


Figure 32.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

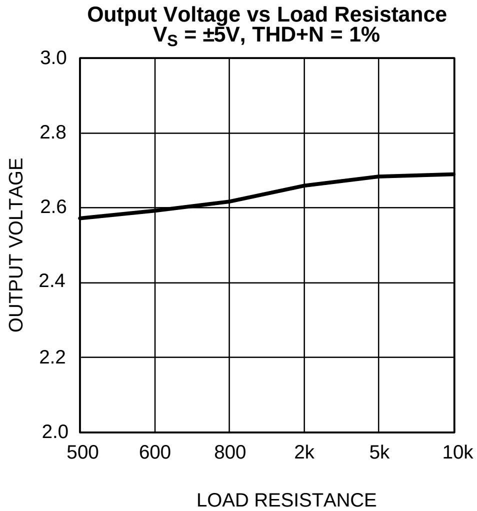
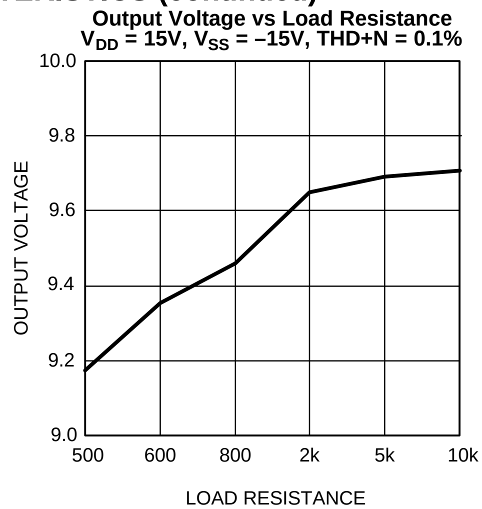


Figure 33.



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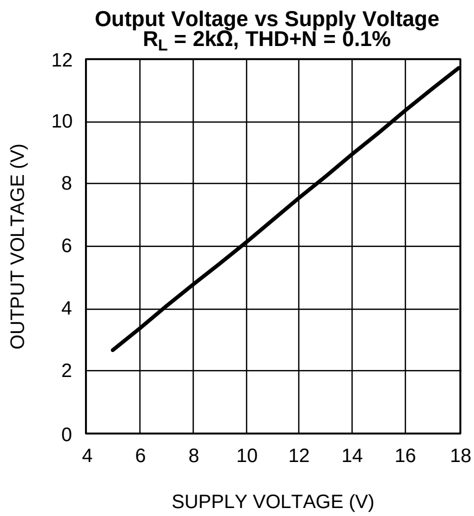
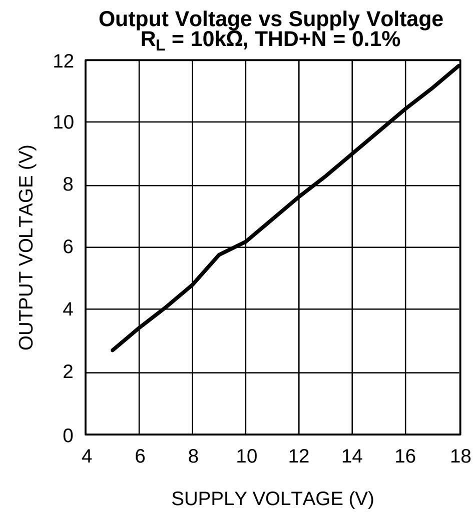


Figure 35.



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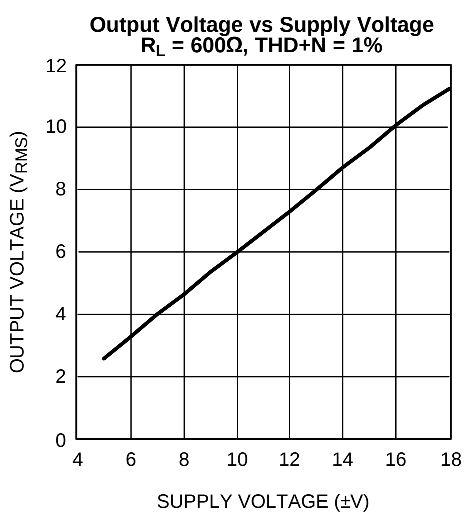


Figure 37.

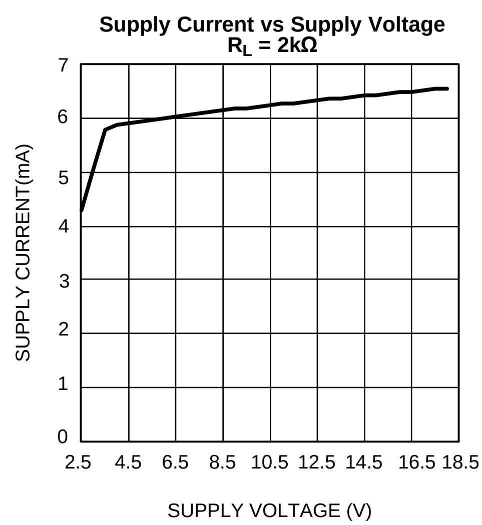


Figure 38.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Supply Current vs Supply Voltage
R_L = 10kΩ

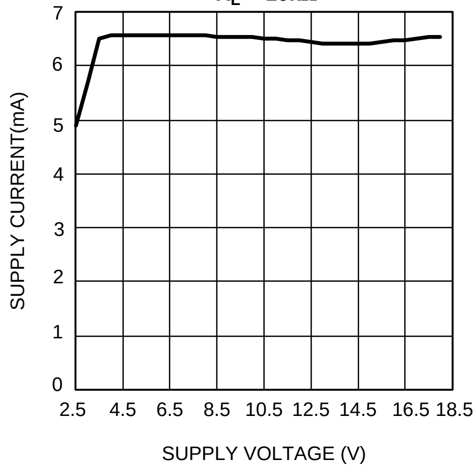


Figure 39.

Supply Current vs Supply Voltage
R_L = 600Ω

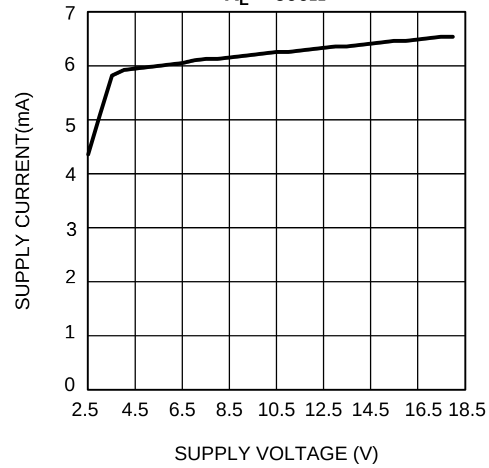


Figure 40.

Noninverting Amp

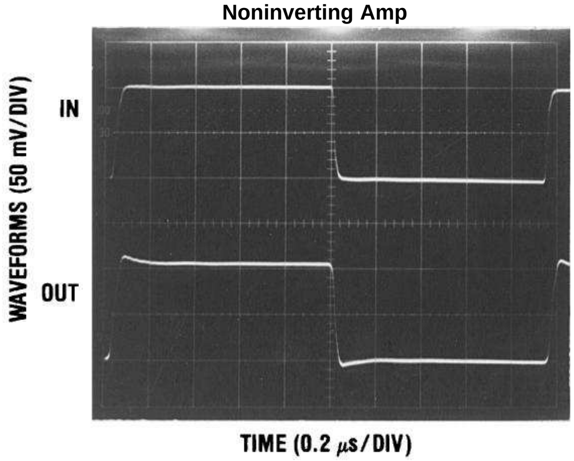


Figure 41.

Noninverting Amp

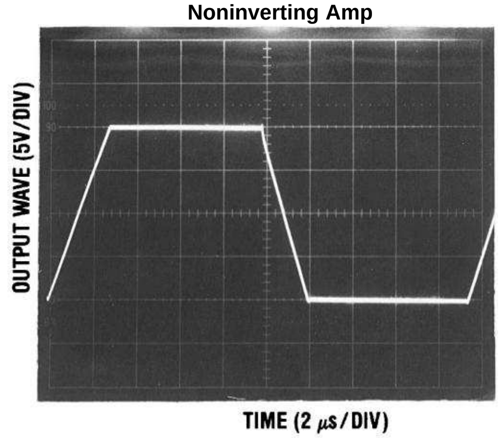


Figure 42.

Inverting Amp

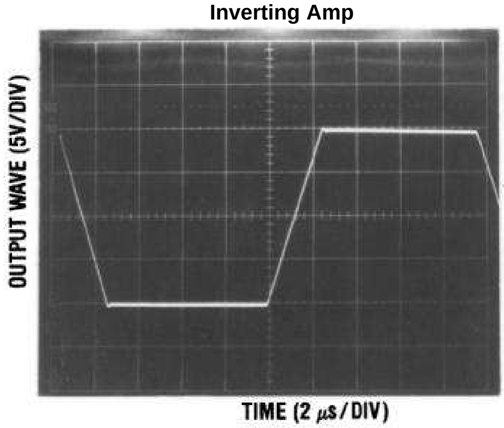


Figure 43.

Voltage Gain & Phase vs Frequency

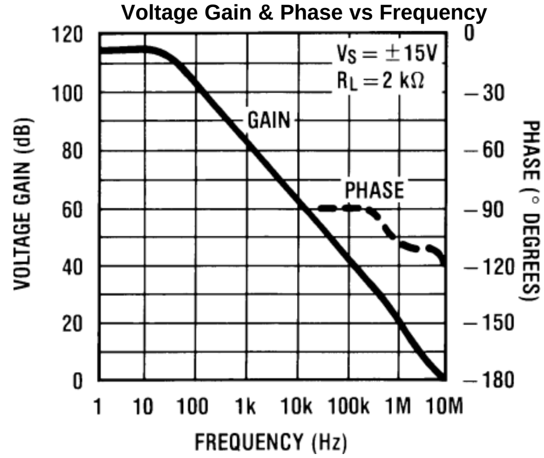


Figure 44.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Power Bandwidth

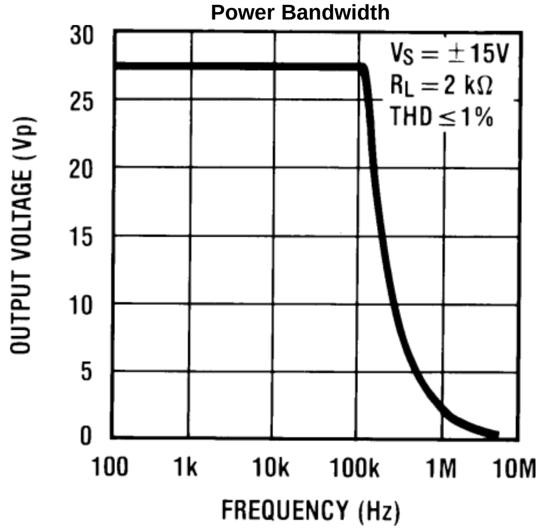


Figure 45.

Equivalent Input Noise vs Frequency

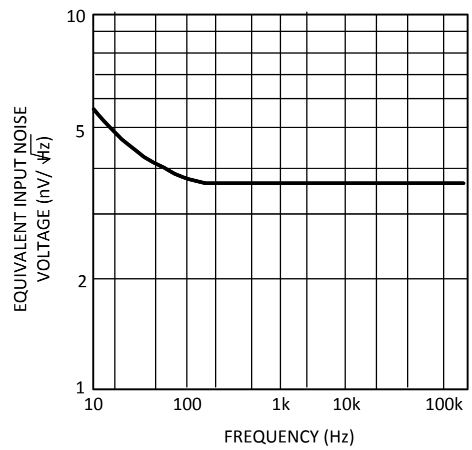


Figure 46.

APPLICATION INFORMATION

DISTORTION MEASUREMENTS

The vanishingly low residual distortion produced by LME49723 is below the capabilities of all commercially available equipment. This makes distortion measurements just slightly more difficult than simply connecting a distortion meter to the amplifier's inputs and outputs. The solution, however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49723's low residual distortion is an input referred internal error. As shown in Figure 47, adding the 10Ω resistor connected between the amplifier's inverting and non-inverting inputs changes the amplifier's noise gain. The result is that the error signal (distortion) is amplified by a factor of 101. Although the amplifier's closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced by 101, which means that measurement resolution increases by 101. To ensure minimum effects on distortion measurements, keep the value of R1 low as shown in Figure 47.

This technique is verified by duplicating the measurements with high closed loop gain and/or making the measurements at high frequencies. Doing so produces distortion components that are within the measurement equipment's capabilities. This datasheet's THD+N and IMD values were generated using the above described circuit connected to an Audio Precision System Two Cascade.

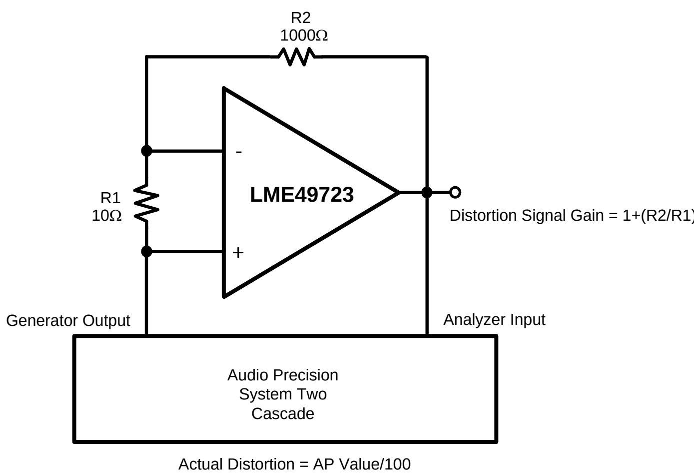
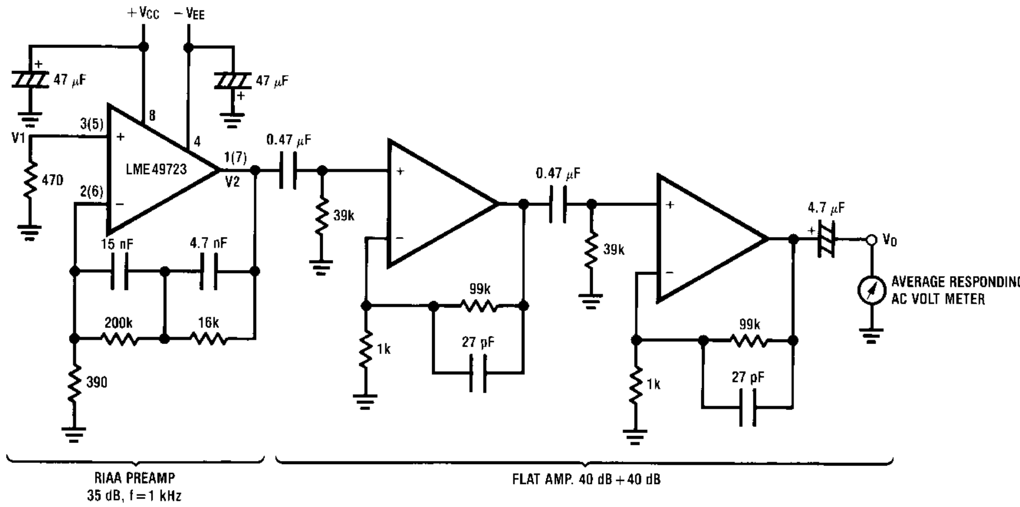


Figure 47. THD+N and IMD Distortion Test Circuit

The LME49723 is a high speed op amp with excellent phase margin and stability. Capacitive loads up to 100pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 100pF must be isolated from the output. The most straightforward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.



Complete shielding is required to prevent induced pick up from external sources. Always check with oscilloscope for power line noise.

Figure 48. Noise Measurement Circuit Total Gain: 115 dB @f = 1 kHz Input Referred Noise Voltage: e_n = V0/560,000 (V)

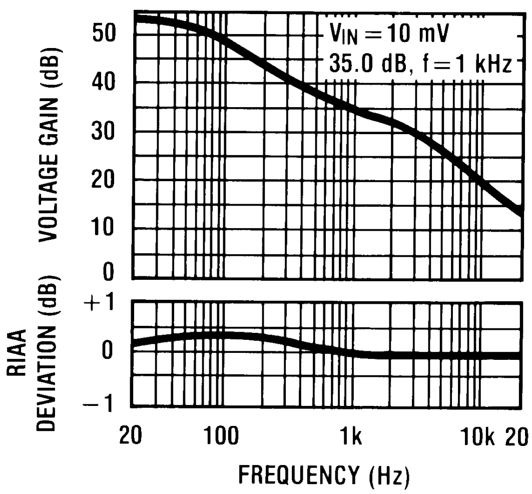


Figure 49. RIAA Preamp Voltage Gain, RIAA Deviation vs Frequency

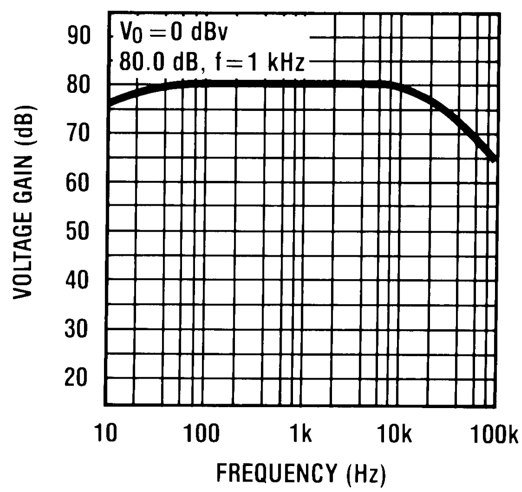
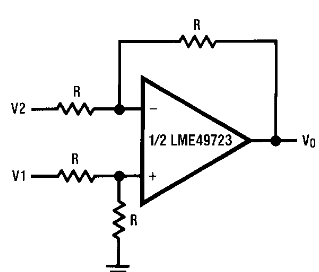


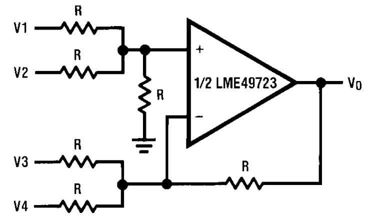
Figure 50. Flat Amp Voltage Gain vs Frequency

TYPICAL APPLICATIONS



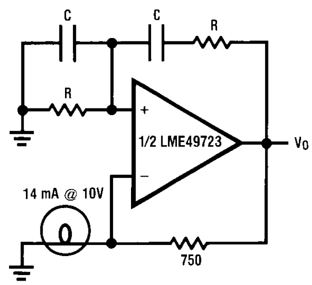
V_O = V1–V2

Figure 51. Balanced to Single Ended Converter



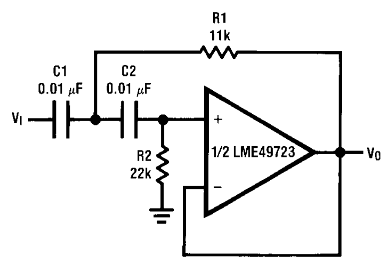
$V_O = V1 + V2 - V3 - V4$

Figure 52. Adder/Subtracter



$$f_o = \frac{1}{2\pi RC}$$

Figure 53. Sine Wave Oscillator



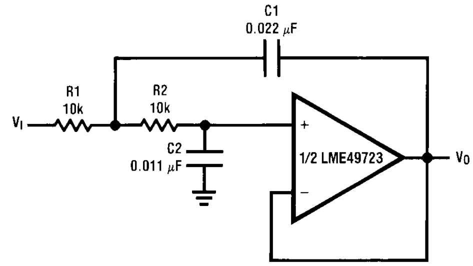
if C1 = C2 = C

$$R1 = \frac{\sqrt{2}}{2\omega_0 C}$$

R2 = 2•R1

Illustration is f_0 = 1 kHz

Figure 54. Second Order High Pass Filter (Butterworth)



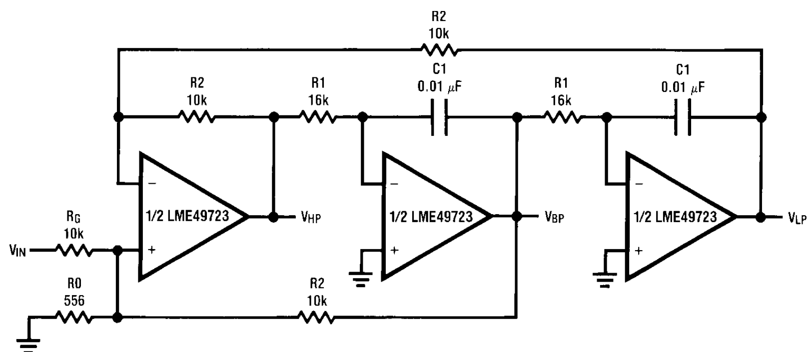
if R1 = R2 = R

$$C1 = \frac{\sqrt{2}}{\omega_0 R}$$

$$C2 = \frac{C1}{2}$$

Illustration is f_0 = 1 kHz

Figure 55. Second Order Low Pass Filter (Butterworth)



$$f_0 = \frac{1}{2\pi C1R1}, Q = \frac{1}{2}\left(1 + \frac{R2}{R0} + \frac{R2}{RG}\right), A_{BP} = QA_{LP} = QA_{LH} = \frac{R2}{RG}$$

Illustration is f_0 = 1 kHz, Q = 10, A_{BP} = 1

Figure 56. State Variable Filter

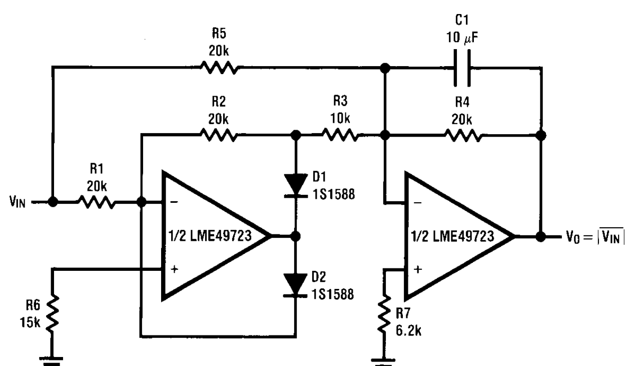


Figure 57. AC/DC Converter

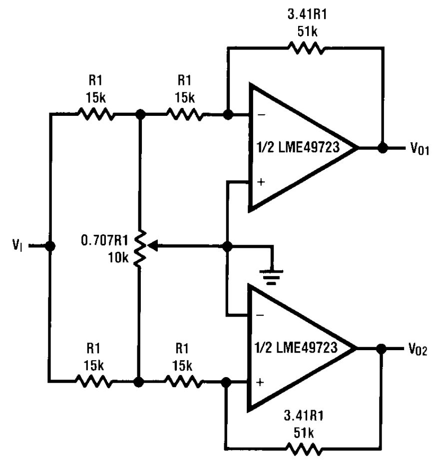


Figure 58. 2 Channel Panning Circuit (Pan Pot)

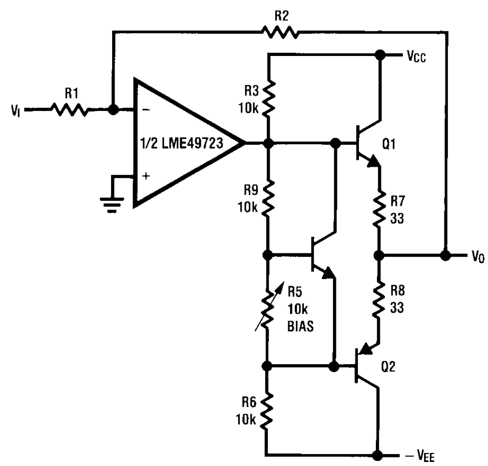
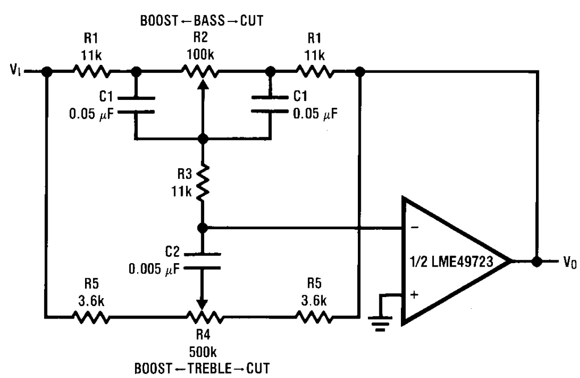


Figure 59. Line Driver



$$f_L = \frac{1}{2\pi R2C1},\ f_{LB} = \frac{1}{2\pi R1C1}$$

$$f_H = \frac{1}{2\pi R5C2},\ f_{HB} = \frac{1}{2\pi (R1 + R5 + 2R3)C2}$$

Illustration is:

f_L = 32 Hz, f_{LB} = 320 Hz

f_H =11 kHz, f_{HB} = 1.1 kHz

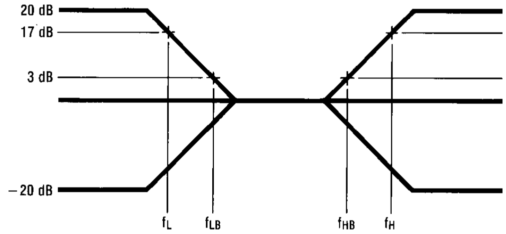
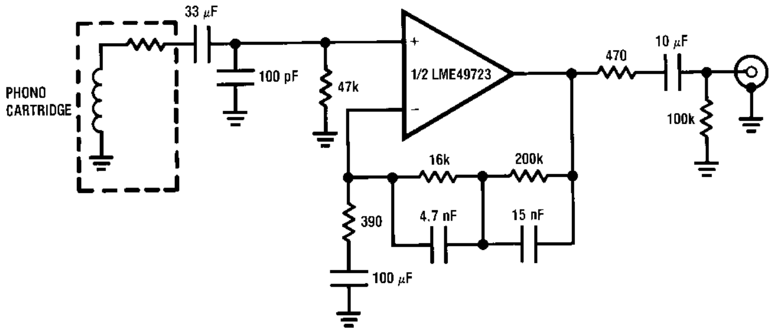
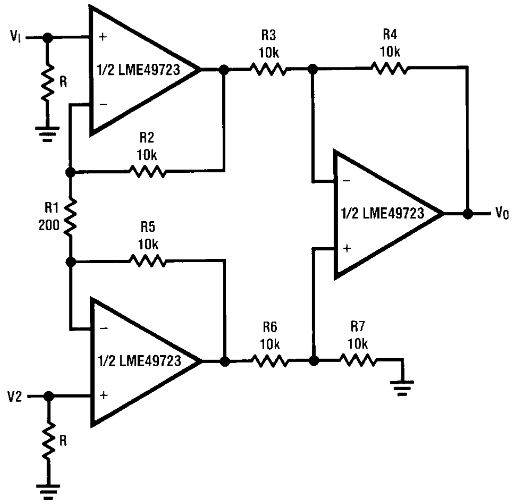


Figure 60. Tone Control



A_v = 35 dB
E_n = 0.33 µV
S/N = 90 dB
f = 1 kHz
A Weighted
A Weighted, V_{IN} = 10 mV
@f = 1 kHz

Figure 61. RIAA Preamp



If R2 = R5, R3 = R6, R4 = R7

$$V0 = \left(1 + \frac{2R2}{R1}\right)\frac{R4}{R3}(V2 - V1)$$

Illustration is:
V0 = 101(V2 − V1)

Figure 62. Balanced Input Mic Amp

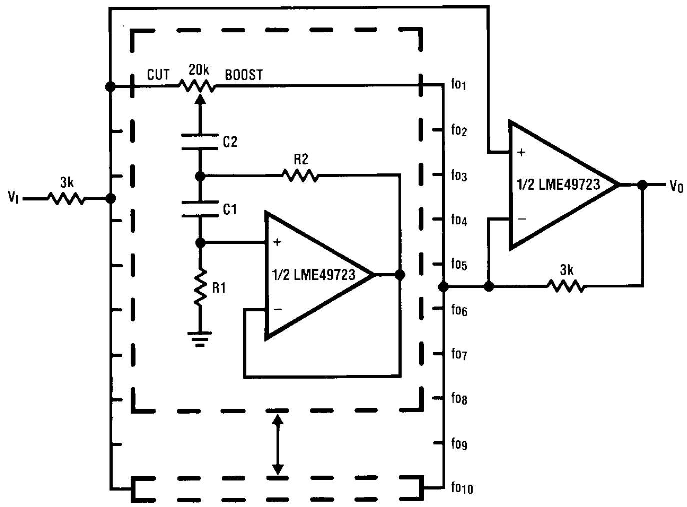


Figure 63. Band Graphic Equalizer

fo (Hz)	C_1	C_2	R_1	R_2
32	0.12µF	4.7µF	75kΩ	500Ω
64	0.056µF	3.3µF	68kΩ	510Ω
125	0.033µF	1.5µF	62kΩ	510Ω
250	0.015µF	0.82µF	68kΩ	470Ω
500	8200pF	0.39µF	62kΩ	470Ω
1k	3900pF	0.22µF	68kΩ	470Ω
2k	2000pF	0.1µF	68kΩ	470Ω
4k	1100pF	0.056µF	62kΩ	470Ω
8k	510pF	0.022µF	68kΩ	510Ω
16k	330pF	0.012µF	51kΩ	510Ω

REVISION HISTORY

Rev	Date	Description
1.0	01/07/08	Initial release.
1.01	02/11/08	Text edits.
B	04/04/13	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LME49723MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L49723 MA	Samples
LME49723MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L49723 MA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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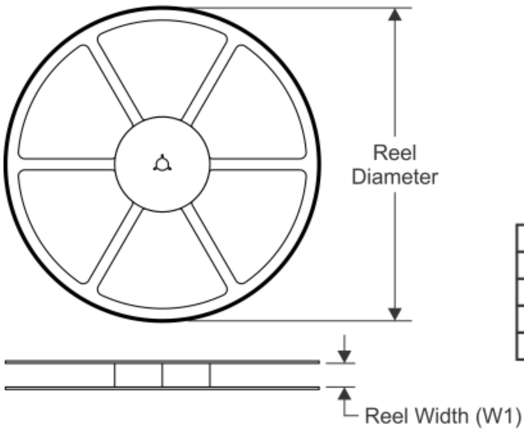
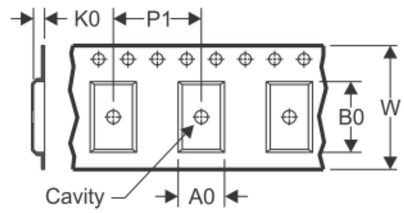
TAPE AND REEL INFORMATION

REEL DIMENSIONS

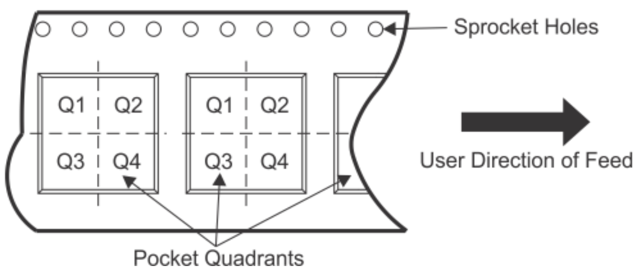


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

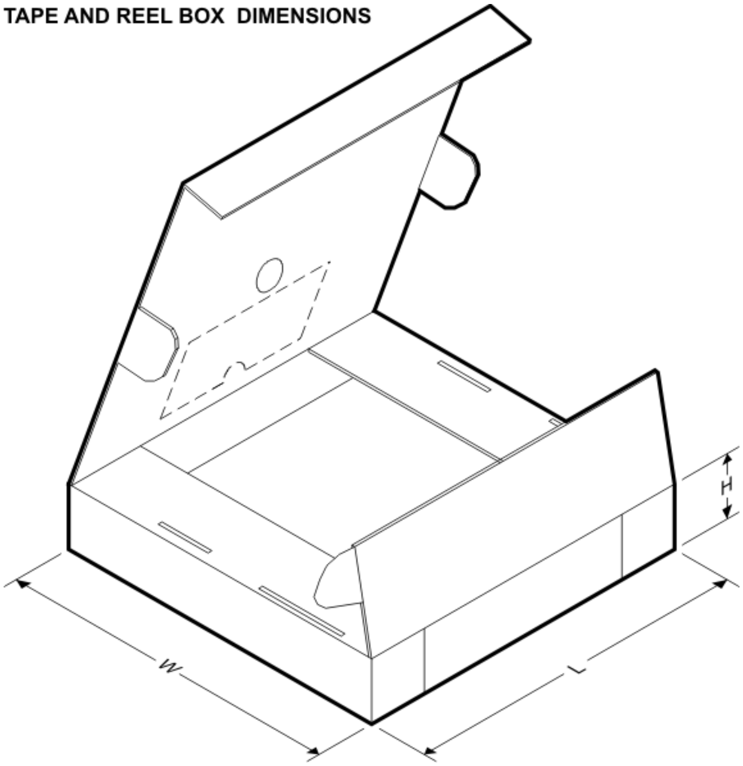
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LME49723MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

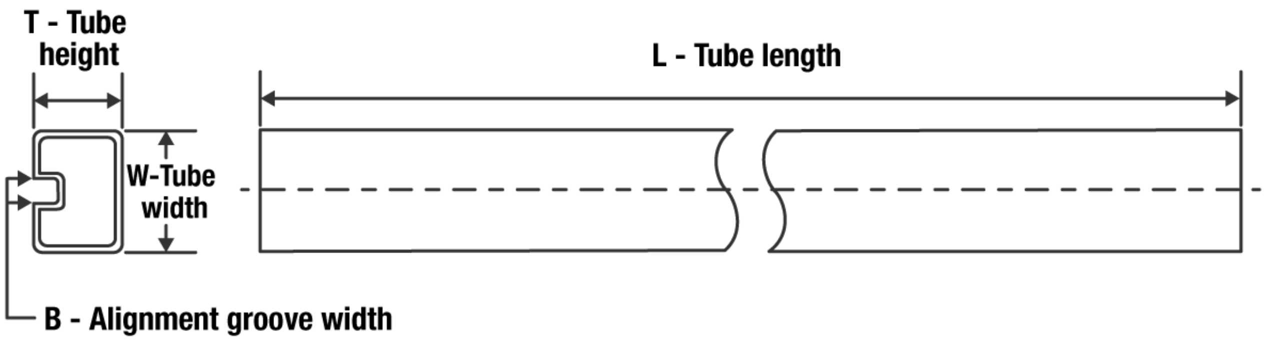
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

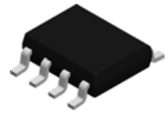
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LME49723MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LME49723MA/NOPB	D	SOIC	8	95	495	8	4064	3.05

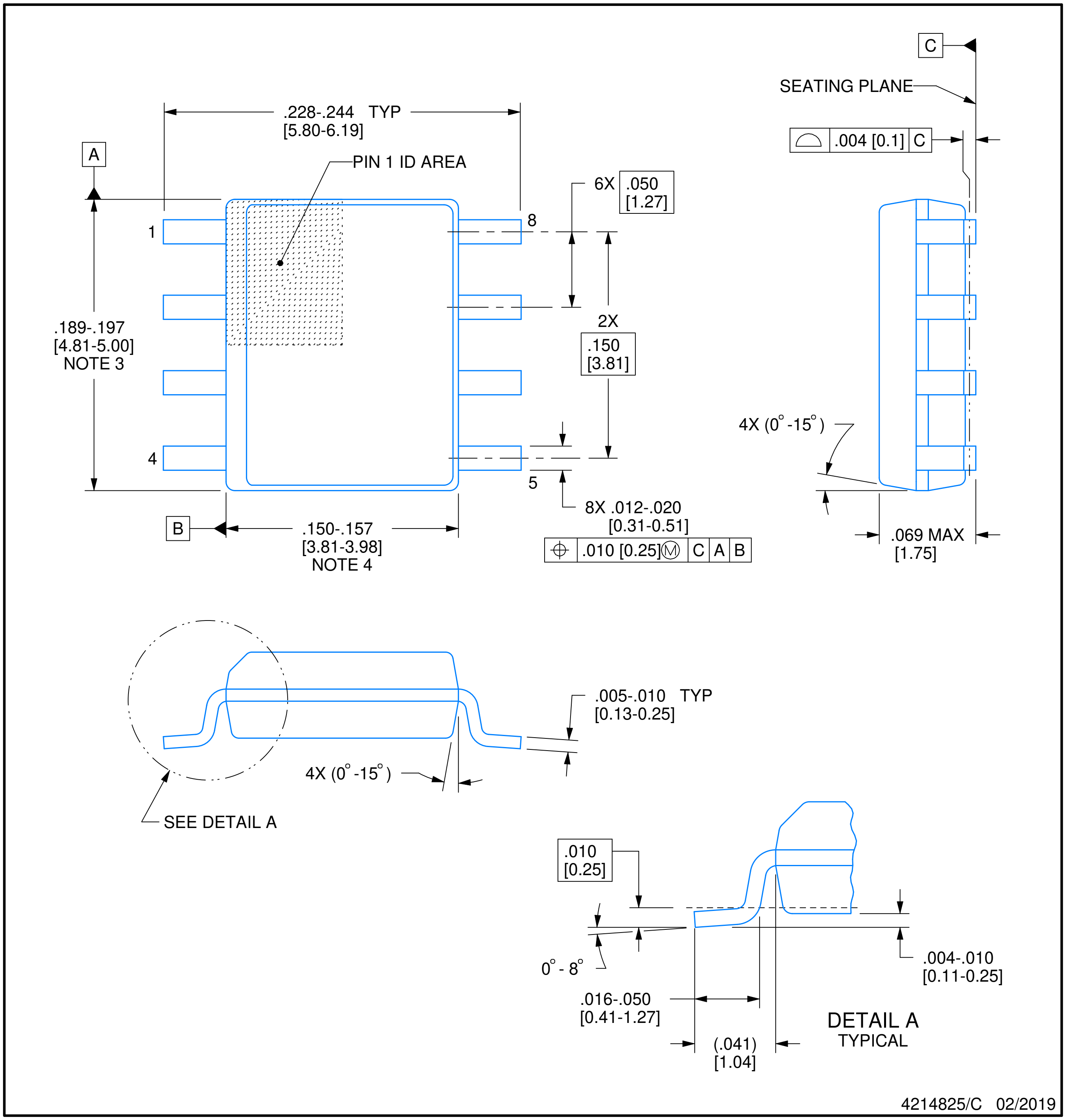


PACKAGE OUTLINE

D0008A

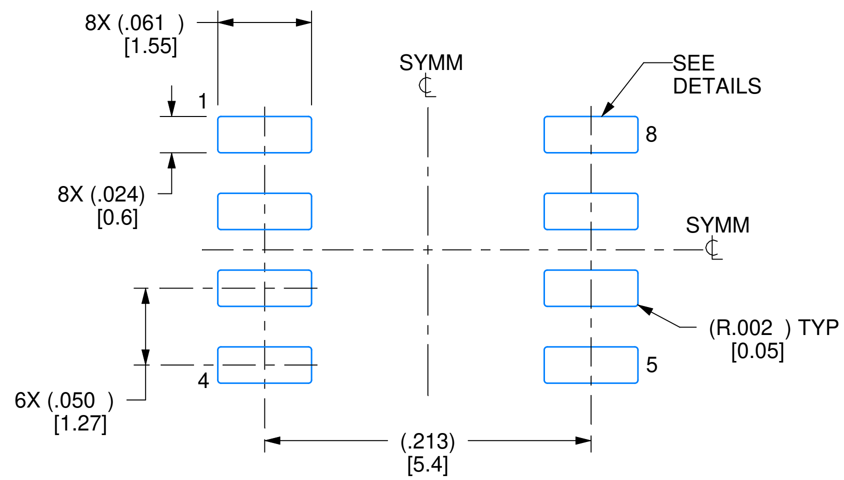
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

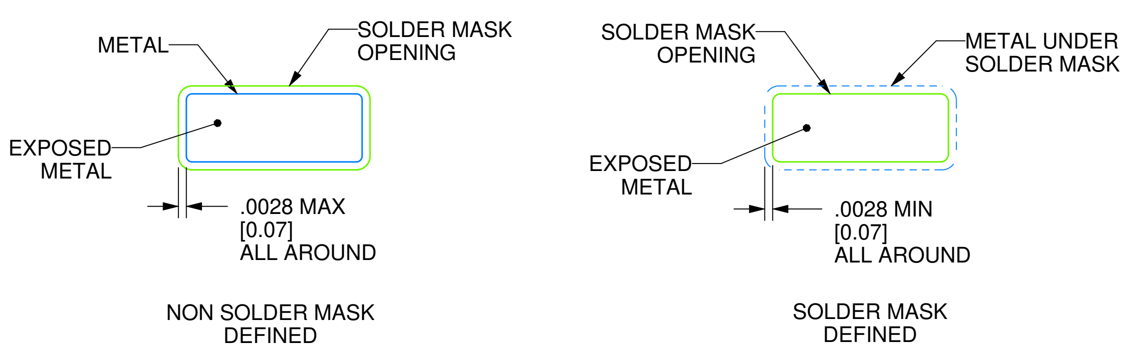


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

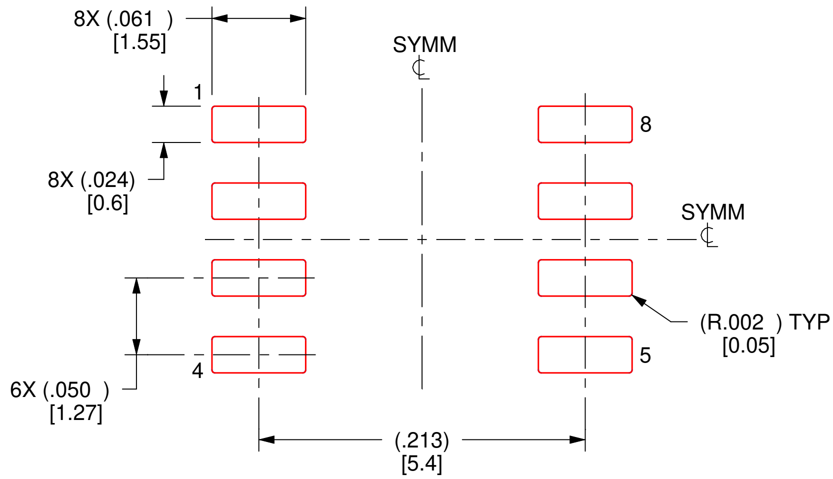


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.