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S6J311A, S6J3119

32-Bit TRAVEO™ T1G Family S6J3110 Series Microcontroller Datasheet

The S6J3110 series is a set of 32-bit microcontrollers designed for in-vehicle use. It uses the Arm® Cortex®-R5 CPU as a CPU.

Features

Cortex-R5 Core

This section explains the Cortex-R5 CPU core.

- Arm Cortex-R5
- 32-bit Arm architecture
  - 2-instruction issuance super scalar
  - 8-stage pipeline
- Armv7/Thumb®-2 instruction set
- MPU (memory protection) equipped
  - 16-area support
- ECC support for the TCM ports for RAM

  1-bit error correction and 2-bit error detection (SEC-DED)
- TCM ports

  2 TCM ports
  - ATCM port
  - BTCM port (B0TCM, B1TCM)
- Caches
  - Instruction cache 16 KB
  - Data cache 16 KB
- VIC port

  Low latency interrupt
- AXI master interface

  64-bit AXI interface (instruction/data access)

  32-bit AXI interface (I/O access)
- AXI slave interface

  64-bit AXI interface (TCM port access)
- ETM-R5 trace

Peripheral Functions

This section explains peripheral functions.

- Clock generation
  - Main clock oscillation (4 MHz)
  - No sub clock oscillation
  - CR oscillation (100 kHz)
  - CR oscillation (4 MHz)
- Built-in flash memory size
  - Program: 1024 K + 64 KB (S6J311AHAC) / 768 K + 64 KB (S6J3119HAC)
  - Work: 48 KB (S6J311AHAC) / 48 KB (S6J3119HAC)
- Built-in RAM size
  - TCRAM 64 KB (S6J311AHAC) / 48 KB (S6J3119HAC)
  - System SRAM 16 KB (S6J311AHAC) / 16 KB (S6J3119HAC)
  - Backup RAM 8 KB (S6J311AHAC) / Backup RAM 8 KB (S6J3119HAC)
- General-purpose ports: 116 channels (S6J311AHAC) / 116 channels (S6J3119HAC)
- DMA controller
  - Up to 16 channels can be activated simultaneously.
- A/D converter (successive approximation type)

  12-bit resolution, 2 units mounted: Max 56 channels (25 channels + 31 channels) (S6J311AHAC) / Max 56 channels (25 channels + 31 channels) (S6J3119HAC) / Max 56 channels (25 channels + 31 channels)
- External interrupt input: 16 channels
  - Level ("H"/"L") and edge (rising/falling) can be detected.
- Multi-function serial (transmission and reception FIFOs mounted) :Max 4 channels (S6J311AHAC) / Max 4 channels (S6J3119HAC)

  <I^2C>
- Full-duplex double buffering system, 64-byte transmission FIFO, 64-byte reception FIFO.
- Standard mode (Max. 100 kbps) is supported only.
- DMA transfer is supported.

  <UART (asynchronous serial interface) >
- Full duplex, double buffering system; 64-byte transmission FIFO, 64-byte reception FIFO
- Parity check can be enabled/disabled.
- Built-in dedicated baud rate generator
- An external clock can be used as a transfer clock.
- Parity, frame, overrun error detection functions are available.
- DMA transfer is supported.

<CSIO (synchronous serial interface) >

- Full duplex, double buffering system; 64-byte transmission FIFO, 64-byte reception FIFO
- Support for SPI. Both master and slave roles are supported. Data length in bits can be set to a value from 5 to 16 or one of the values of 20, 24, and 32.
- Built-in dedicated baud rate generator (master operation)
- External clock input is enabled (slave operation).
- Overrun error detection function is available.
- DMA transfer is supported.
- Serial chip select SPI function

<LIN-UART (asynchronous serial interface for LIN) >

- Full duplex, double buffering system; 64-byte transmission FIFO, 64-byte reception FIFO
- Support for LIN protocol revision 2.1
- Both master and slave roles are supported.
- Framing error and overrun error detection
- LIN Synch break generation and detection, LIN Synch Delimiter generation
- Built-in dedicated baud rate generator
- The external clock can be adjusted by the reload counter.

DMA transfer is supported.

- CAN controller: CAN-FD Max 1 channel
  - CAN-FD (V3.2.0)
  - CAN transfer speed :Max 5 Mbps
  - CAN Clock :Max 40 MHz
  - 192 message buffers/channel (reception message buffer size)
  - 32 message buffer/channel (transmission message buffer size)
- Base timer: Max 30 channels
  - 16-bit Timer.
  - It is selectable by 4 functions of the PWM/PPG/PWC/Reload Timer.
  - 2-channel cascade connection enables operation as a 32-bit timer.(PWC and Reload Timer)
- Free-run timer: Max 6 channels
  - 32-bit Timer.
  - Main clock oscillation and CR oscillation are available.
  - Free-run timer output can work in combination with an input capture and an output compare.
- Input capture: Max 12 channels
  - 32-bit Timer.
- Output compare: Max 12 channels
  - 32-bit Timer.
- Real time clock (RTC) (day/hour/minute/second)
  - Main clock oscillation or CR oscillation (100 kHz) can be selected as an operation clock.
- Calibration: Real time clock (RTC) driven by the CR clock
- Correction can be done by configuring the prescaler of the real time clock based on the ratio between the main clock and the CR clock.
- Clock supervisor
  - Abnormality (such as damaged crystal) of the main clock oscillation (4 MHz) can be monitored.
  - The clock can switch to the CR clock when an abnormality is detected.
  - PLL abnormality can be detected.
- CRC generation
  - Fixed-length CRC
  - CCITT CRC16 generator polynomial: 0x1021
  - IEEE-802.3 CRC32 generator polynomial: 0x04C11DB7
- Watchdog timer
  - Hardware watchdog
  - Software watchdog
- NMI
- I/O relocation
  - Peripheral function pin locations can be changed.
- Low-power consumption control
  - Standby function
  - Power-off function
  - Partial wakeup function
- Power-on reset
- Low-voltage detection reset
- Security
  - Flash security
  - Interface security (JTAG + test port)
  - SHE
  - Unique device ID
- Package: LEU144 (S6J311xHAC)

- CMOS 55 nm technology
- Power supply
  - 5 V single power supply
  - The voltage step-down circuit generates internal 1.2 V from 5 V.
  - 5 V power supply is used for I/O.

Contents

1. Product Lineup

The following table lists the product lineup of the S6J3110 series.

Table 1-1. Memory Size

		S6J311AHAC	S6J3119HAC
Flash	Program	1024 KBytes + Small sector (8 KB x 8)	768 KBytes + Small sector (8 KB x 8)
	Work	48 KBytes	48 KBytes
RAM	TCRAM	64 KBytes	48 KBytes
	System SRAM	16 KBytes	16 KBytes
	Backup RAM	8 KBytes	8 KBytes

Table 1-2. SHE option

	S6J311xHAC*
Security (SHE)	ON

* x: A/9

Table 1-3. Product Lineup

	S6J311xHAC*
CPU core	Coretex-R5
CMOS 55 nm technology	55 nm
Package	LEU144
Main clock	4 MHz
Built-in CR oscillator	100 kHz
	4 MHz
Maximum CPU operating frequency	96 MHz
Watchdog timer	1 channel (hardware) 1 channel (software)
Clock supervisor	YES
External power supply, low-voltage detection reset	YES
Internal power supply, low-voltage detection reset	YES
NMI request	YES
External interrupt	16 channels
DMA controller	16 channels
CAN-FD	1 channel (192 msg buffers/ch)
Multi-function serial	4 channels
A/D converter	12-bit (2 units) Unit 0 x 25 channels Unit 1 x 31 channels

	S6J311xHAC*
Free-run timer	6 channels
Input capture	12 channels
Output compare	12 channels
Base timer (16-bit)	30 channels
Real time clock (RTC)	1 channel
CR clock calibration	YES
CRC generation	YES
Low-power consumption mode	Standby function Power-off function Partial wakeup function
SHE	YES
General-purpose port GPIO	116 channels
Power supply	5 V + 5% to 10%
Operation assurance temperature (T_A)	-40 °C to +125 °C
On-chip debugger (JTAG)	YES

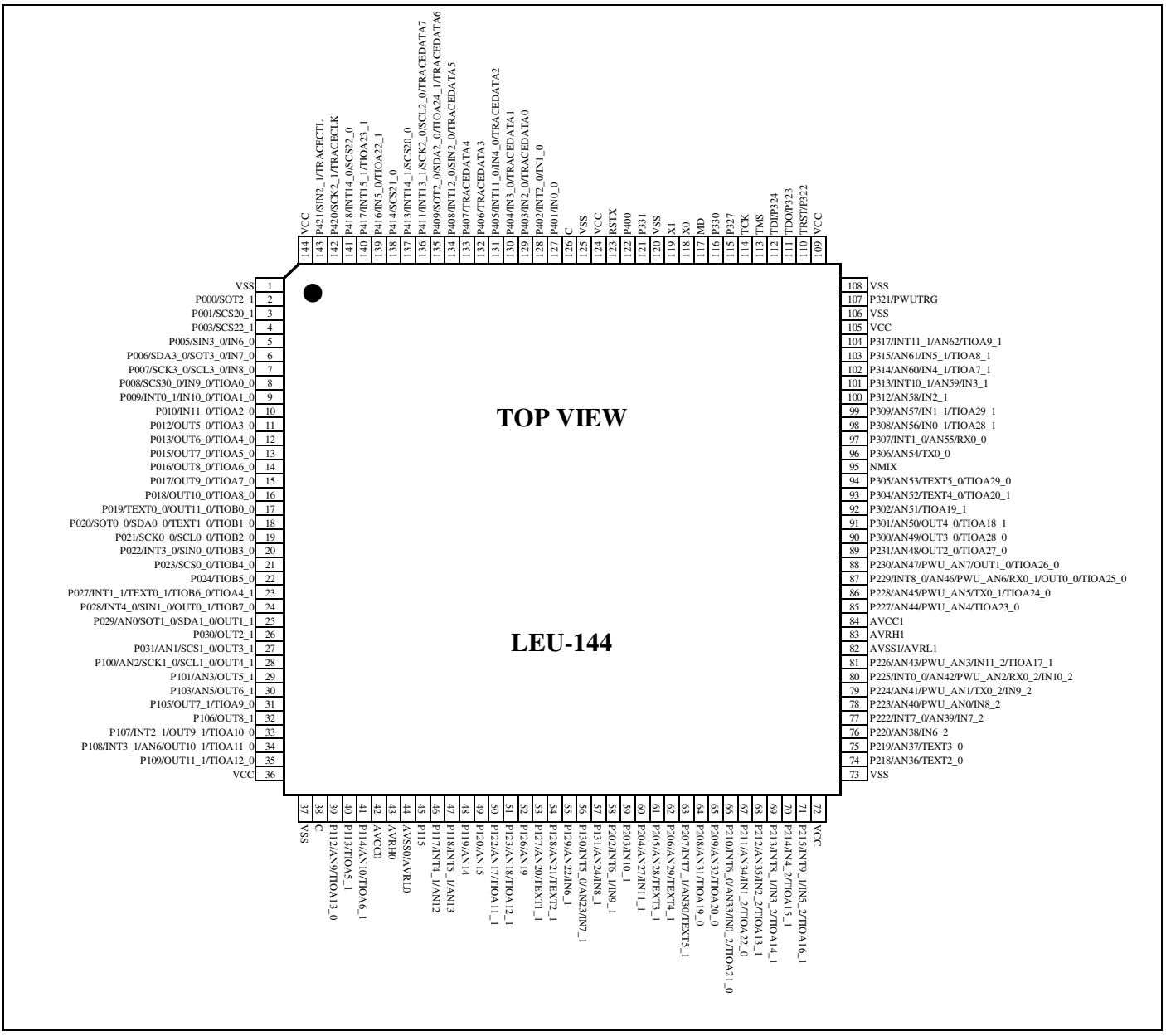
* x: A/9

2. Pin Assignment

The following figures show the pin assignment of the S6J3110 series.

Figure 2-1. Pin Assignment for S6J311xHAC*

* x: A/9



3. Pin Description

This section provides a list of the pin functions of the S6J3110 series

Table 3-1. S6J311xHAC* Pin Functions

* x: A/9

Pin No. S6J311xHAC	Pin Name	Polarity	I/O Circuit Type	Function
2	P000 SOT2_1	- -	P	General-purpose I/O port Multi-function serial ch.2 serial data output pin (1)
3	P001 SCS20_1	- -	P	General-purpose I/O port Multi-function serial ch.2 serial chip select 0 I/O pin (1)
4	P003 SCS22_1	- -	P	General-purpose I/O port Multi-function serial ch.2 serial chip select 2 output pin (1)
5	P005 IN6_0 SIN3_0	- - -	P	General-purpose I/O port Input capture ch.6 input pin (0) Multi-function serial ch.3 serial data input pin (0)
6	P006 IN7_0 SOT3_0 SDA3_0	- - - -	P	General-purpose I/O port Input capture ch.7 input pin (0) Multi-function serial ch.3 serial data output pin (0) I^2C bus ch.3 serial data I/O pin
7	P007 IN8_0 SCK3_0 SCL3_0	- - - -	P	General-purpose I/O port Input capture ch.8 input pin (0) Multi-function serial ch.3 clock I/O pin (0) I^2C bus ch.3 serial clock I/O pin
8	P008 IN9_0 SCS30_0 TIOA0_0	- - - -	P	General-purpose I/O port Input capture ch.9 input pin (0) Multi-function serial ch.3 serial chip select 0 I/O pin (0) Base timer ch.0 TIOA output pin (0)
9	P009 IN10_0 TIOA1_0 INT0_1	- - - -	P	General-purpose I/O port Input capture ch.10 input pin (0) Base timer ch.1 TIOA I/O pin (0) INT0 external interrupt input pin (1)
10	P010 IN11_0 TIOA2_0	- - -	P	General-purpose I/O port Input capture ch.11 input pin (0) Base timer ch.2 TIOA output pin (0)
11	P012 TIOA3_0 OUT5_0	- - -	P	General-purpose I/O port Base timer ch.3 TIOA I/O pin (0) Output compare ch.5 output pin (0)
12	P013 TIOA4_0 OUT6_0	- - -	P	General-purpose I/O port Base timer ch.4 TIOA output pin (0) Output compare ch.6 output pin (0)
13	P015 TIOA5_0 OUT7_0	- - -	P	General-purpose I/O port Base timer ch.5 TIOA I/O pin (0) Output compare ch.7 output pin (0)
14	P016 TIOA6_0 OUT8_0	- - -	P	General-purpose I/O port Base timer ch.6 TIOA output pin (0) Output compare ch.8 output pin (0)
15	P017 TIOA7_0 OUT9_0	- - -	P	General-purpose I/O port Base timer ch.7 TIOA I/O pin (0) Output compare ch.9 output pin (0)
16	P018 TIOA8_0 OUT10_0	- - -	P	General-purpose I/O port Base timer ch.8 TIOA output pin (0) Output compare ch.10 output pin (0)
17	P019 OUT11_0 TIOB0_0 TEXT0_0	- - - -	P	General-purpose I/O port Output compare ch.11 output pin (0) Base timer ch.0 TIOB input pin (0) Free-run timer 0 clock input pin (0)

Pin No. S6J311xHAC	Pin Name	Polarity	I/O Circuit Type	Function
18	P020 SOT0_0 SDA0_0 TIOB1_0 TEXT1_0	- - - - -	P	General-purpose I/O port Multi-function serial ch.0 serial data output pin (0) I²C bus ch.0 serial data I/O pin Base timer ch.1 TIOB input pin (0) Free-run timer 1 clock input pin (0)
19	P021 SCK0_0 SCL0_0 TIOB2_0	- - - -	P	General-purpose I/O port Multi-function serial ch.0 clock I/O pin (0) I²C bus ch.0 serial clock I/O pin Base timer ch.2 TIOB input pin (0)
20	P022 SIN0_0 TIOB3_0 INT3_0	- - - -	P	General-purpose I/O port Multi-function serial ch.0 serial data input pin (0) Base timer ch.3 TIOB input pin (0) INT3 external interrupt input pin (0)
21	P023 SCS0_0 TIOB4_0	- - -	P	General-purpose I/O port Multi-function serial ch.0 serial chip select I/O pin (0) Base timer ch.4 TIOB input pin (0)
22	P024 TIOB5_0	- -	P	General-purpose I/O port Base timer ch.5 TIOB input pin (0)
23	P027 TIOA4_1 TIOB6_0 INT1_1 TEXT0_1	- - - - -	P	General-purpose I/O port Base timer ch.4 TIOA output pin (1) Base timer ch.6 TIOB input pin (0) INT1 external interrupt input pin (1) Free-run timer 0 clock input pin (1)
24	P028 SIN1_0 TIOB7_0 INT4_0 OUT0_1	- - - - -	P	General-purpose I/O port Multi-function serial ch.1 serial data input pin (0) Base timer ch.7 TIOB input pin (0) INT4 external interrupt input pin (0) Output compare ch.0 output pin (1)
25	P029 SOT1_0 SDA1_0 AN0 OUT1_1	- - - - -	A	General-purpose I/O port Multi-function serial ch.1 serial data output pin (0) I²C bus ch.1 serial data I/O pin ADC analog 0 input pin Output compare ch.1 output pin (1)
26	P030 OUT2_1	- -	P	General-purpose I/O port Output compare ch.2 output pin (1)
27	P031 SCS1_0 AN1 OUT3_1	- - - -	A	General-purpose I/O port Multi-function serial ch.1 serial chip select I/O pin (0) ADC analog 1 input pin Output compare ch.3 output pin (1)
28	P100 SCK1_0 SCL1_0 AN2 OUT4_1	- - - - -	A	General-purpose I/O port Multi-function serial ch.1 clock I/O pin (0) I²C bus ch.1 serial clock I/O pin ADC analog 2 input pin Output compare ch.4 output pin (1)
29	P101 AN3 OUT5_1	- - -	A	General-purpose I/O port ADC analog 3 input pin Output compare ch.5 output pin (1)
30	P103 AN5 OUT6_1	- - -	A	General-purpose I/O port ADC analog 5 input pin Output compare ch.6 output pin (1)
31	P105 TIOA9_0 OUT7_1	- - -	P	General-purpose I/O port Base timer ch.9 TIOA I/O pin (0) Output compare ch.7 output pin (1)
32	P106 OUT8_1	- -	P	General-purpose I/O port Output compare ch.8 output pin (1)
33	P107 TIOA10_0 INT2_1 OUT9_1	- - - -	P	General-purpose I/O port Base timer ch.10 TIOA output pin (0) INT2 external interrupt input pin (1) Output compare ch.9 output pin (1)

Pin No. S6J311xHAC	Pin Name	Polarity	I/O Circuit Type	Function
34	P108 AN6 TIOA11_0 INT3_1 OUT10_1	- - - - -	A	General-purpose I/O port ADC analog 6 input pin Base timer ch.11 TIOA I/O pin (0) INT3 external interrupt input pin (1) Output compare ch.10 output pin (1)
35	P109 TIOA12_0 OUT11_1	- - -	P	General-purpose I/O port Base timer ch.12 TIOA output pin (0) Output compare ch.11 output pin (1)
39	P112 AN9 TIOA13_0	- - -	A	General-purpose I/O port ADC analog 9 input pin Base timer ch.13 TIOA I/O pin (0)
40	P113 TIOA5_1	- -	P	General-purpose I/O port Base timer ch.5 TIOA I/O pin (1)
41	P114 AN10 TIOA6_1	- - -	A	General-purpose I/O port ADC analog 10 input pin Base timer ch.6 TIOA output pin (1)
45	P115	-	P	General-purpose I/O port
46	P117 AN12 INT4_1	- - -	A	General-purpose I/O port ADC analog 12 input pin INT4 external interrupt input pin (1)
47	P118 AN13 INT5_1	- - -	A	General-purpose I/O port ADC analog 13 input pin INT5 external interrupt input pin (1)
48	P119 AN14	- -	A	General-purpose I/O port ADC analog 14 input pin
49	P120 AN15	- -	A	General-purpose I/O port ADC analog 15 input pin
50	P122 AN17 TIOA11_1	- - -	A	General-purpose I/O port ADC analog 17 input pin Base timer ch.11 TIOA I/O pin (1)
51	P123 AN18 TIOA12_1	- - -	A	General-purpose I/O port ADC analog 18 input pin Base timer ch.12 TIOA output pin (1)
52	P126 AN19	- -	A	General-purpose I/O port ADC analog 19 input pin
53	P127 AN20 TEXT1_1	- - -	A	General-purpose I/O port ADC analog 20 input pin Free-run timer 1 clock input pin (1)
54	P128 AN21 TEXT2_1	- - -	A	General-purpose I/O port ADC analog 21 input pin Free-run timer 2 clock input pin (1)
55	P129 IN6_1 AN22	- - -	A	General-purpose I/O port Input capture ch.6 input pin (1) ADC analog 22 input pin
56	P130 IN7_1 AN23 INT5_0	- - - -	A	General-purpose I/O port Input capture ch.7 input pin (1) ADC analog 23 input pin INT5 external interrupt input pin (0)
57	P131 IN8_1 AN24	- - -	A	General-purpose I/O port Input capture ch.8 input pin (1) ADC analog 24 input pin
58	P202 IN9_1 INT6_1	- - -	P	General-purpose I/O port Input capture ch.9 input pin (1) INT6 external interrupt input pin (1)
59	P203 IN10_1	- -	P	General-purpose I/O port Input capture ch.10 input pin (1)

Pin No. S6J311xHAC	Pin Name	Polarity	I/O Circuit Type	Function
60	P204 IN11_1 AN27	- - -	A	General-purpose I/O port Input capture ch.11 input pin (1) ADC analog 27 input pin
61	P205 AN28 TEXT3_1	- - -	A	General-purpose I/O port ADC analog 28 input pin Free-run timer 3 clock input pin (1)
62	P206 AN29 TEXT4_1	- - -	A	General-purpose I/O port ADC analog 29 input pin Free-run timer 4 clock input pin (1)
63	P207 AN30 INT7_1 TEXT5_1	- - - -	A	General-purpose I/O port ADC analog 30 input pin INT7 external interrupt input pin (1) Free-run timer 5 clock input pin (1)
64	P208 AN31 TIOA19_0	- - -	A	General-purpose I/O port ADC analog 31 input pin Base timer ch.19 TIOA I/O pin (0)
65	P209 AN32 TIOA20_0	- - -	A	General-purpose I/O port ADC analog 32 input pin Base timer ch.20 TIOA output pin (0)
66	P210 IN0_2 AN33 TIOA21_0 INT6_0	- - - - -	A	General-purpose I/O port Input capture ch.0 input pin (2) ADC analog 33 input pin Base timer ch.21 TIOA I/O pin (0) INT6 external interrupt input pin (0)
67	P211 IN1_2 AN34 TIOA22_0	- - - -	A	General-purpose I/O port Input capture ch.1 input pin (2) ADC analog 34 input pin Base timer ch.22 TIOA output pin (0)
68	P212 IN2_2 AN35 TIOA13_1	- - - -	A	General-purpose I/O port Input capture ch.2 input pin (2) ADC analog 35 input pin Base timer ch.13 TIOA I/O pin (1)
69	P213 IN3_2 TIOA14_1 INT8_1	- - - -	P	General-purpose I/O port Input capture ch.3 input pin (2) Base timer ch.14 TIOA output pin (1) INT8 external interrupt input pin (1)
70	P214 IN4_2 TIOA15_1	- - -	P	General-purpose I/O port Input capture ch.4 input pin (2) Base timer ch.15 TIOA I/O pin (1)
71	P215 IN5_2 TIOA16_1 INT9_1	- - - -	P	General-purpose I/O port Input capture ch.5 input pin (2) Base timer ch.16 TIOA output pin (1) INT9 external interrupt input pin (1)
74	P218 AN36 TEXT2_0	- - -	A	General-purpose I/O port ADC analog 36 input pin Free-run timer 2 clock input pin (0)
75	P219 AN37 TEXT3_0	- - -	A	General-purpose I/O port ADC analog 37 input pin Free-run timer 3 clock input pin (0)
76	P220 IN6_2 AN38	- - -	A	General-purpose I/O port Input capture ch.6 input pin (2) ADC analog 38 input pin
77	P222 IN7_2 AN39 INT7_0	- - - -	A	General-purpose I/O port Input capture ch.7 input pin (2) ADC analog 39 input pin INT7 external interrupt input pin (0)

Pin No. S6J311xHAC	Pin Name	Polarity	I/O Circuit Type	Function
78	P223 IN8_2 AN40 PWU_AN0	- - - -	A	General-purpose I/O port Input capture ch.8 input pin (2) ADC analog 40 input pin Partial wakeup ADC analog 0 input pin
79	P224 IN9_2 TX0_2 AN41 PWU_AN1	- - - - -	A	General-purpose I/O port Input capture ch.9 input pin (2) CAN transmission data 0 output pin (2) ADC analog 41 input pin Partial wakeup ADC analog 1 input pin
80	P225 IN10_2 RX0_2 AN42 PWU_AN2 INT0_0	- - - - - -	A	General-purpose I/O port Input capture ch.10 input pin (2) CAN reception data 0 input pin (2) ADC analog 42 input pin Partial wakeup ADC analog 2 input pin INT0 external interrupt input pin (0)
81	P226 IN11_2 AN43 PWU_AN3 TIOA17_1	- - - - -	A	General-purpose I/O port Input capture ch.11 input pin (2) ADC analog 43 input pin Partial wakeup ADC analog 3 input pin Base timer ch.17 TIOA I/O pin (1)
85	P227 AN44 PWU_AN4 TIOA23_0	- - - -	A	General-purpose I/O port ADC analog 44 input pin Partial wakeup ADC analog 4 input pin Base timer ch.23 TIOA I/O pin (0)
86	P228 TX0_1 AN45 PWU_AN5 TIOA24_0	- - - - -	A	General-purpose I/O port CAN transmission data 0 output pin (1) ADC analog 45 input pin Partial wakeup ADC analog 5 input pin Base timer ch.24 TIOA output pin (0)
87	P229 RX0_1 AN46 PWU_AN6 TIOA25_0 INT8_0 OUT0_0	- - - - - - -	A	General-purpose I/O port CAN reception data 0 input pin (1) ADC analog 46 input pin Partial wakeup ADC analog 6 input pin Base timer ch.25 TIOA I/O pin (0) INT8 external interrupt input pin (0) Output compare ch.0 output pin (0)
88	P230 AN47 PWU_AN7 TIOA26_0 OUT1_0	- - - - -	A	General-purpose I/O port ADC analog 47 input pin Partial wakeup ADC analog 7 input pin Base timer ch.26 TIOA output pin (0) Output compare ch.1 output pin (0)
89	P231 AN48 TIOA27_0 OUT2_0	- - - -	A	General-purpose I/O port ADC analog 48 input pin Base timer ch.27 TIOA I/O pin (0) Output compare ch.2 output pin (0)
90	P300 AN49 TIOA28_0 OUT3_0	- - - -	A	General-purpose I/O port ADC analog 49 input pin Base timer ch.28 TIOA output pin (0) Output compare ch.3 output pin (0)
91	P301 AN50 TIOA18_1 OUT4_0	- - - -	A	General-purpose I/O port ADC analog 50 input pin Base timer ch.18 TIOA output pin (1) Output compare ch.4 output pin (0)
92	P302 AN51 TIOA19_1	- - -	A	General-purpose I/O port ADC analog 51 input pin Base timer ch.19 TIOA I/O pin (1)

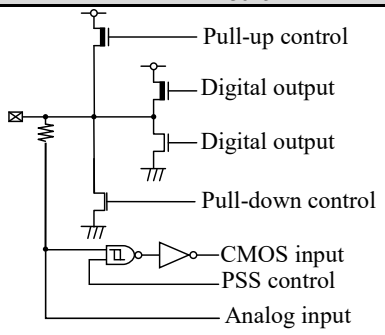
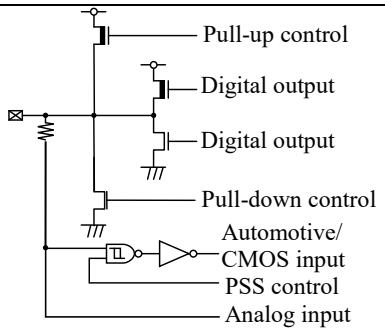
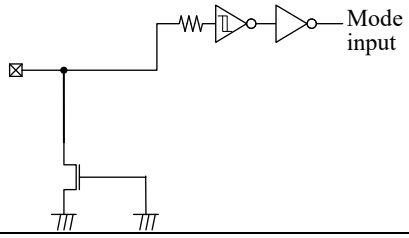
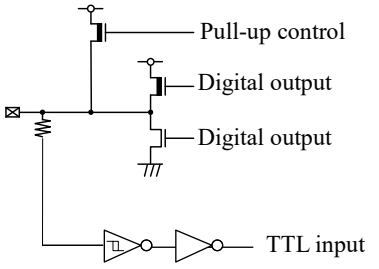
Pin No. S6J311xHAC	Pin Name	Polarity	I/O Circuit Type	Function
93	P304 AN52 TIOA20_1 TEXT4_0	- - - -	A	General-purpose I/O port ADC analog 52 input pin Base timer ch.20 TIOA output pin (1) Free-run timer 4 clock input pin (0)
94	P305 AN53 TIOA29_0 TEXT5_0	- - - -	A	General-purpose I/O port ADC analog 53 input pin Base timer ch.29 TIOA I/O pin (0) Free-run timer 5 clock input pin (0)
95	NMIX	N	F	Non-maskable interrupt input pin
96	P306 TX0_0 AN54	- - -	A	General-purpose I/O port CAN transmission data 0 output pin (0) ADC analog 54 input pin
97	P307 RX0_0 AN55 INT1_0	- - - -	A	General-purpose I/O port CAN reception data 0 input pin (0) ADC analog 55 input pin INT1 external interrupt input pin (0)
98	P308 IN0_1 AN56 TIOA28_1	- - - -	A	General-purpose I/O port Input capture ch.0 input pin (1) ADC analog 56 input pin Base timer ch.28 TIOA output pin (1)
99	P309 IN1_1 AN57 TIOA29_1	- - - -	A	General-purpose I/O port Input capture ch.1 input pin (1) ADC analog 57 input pin Base timer ch.29 TIOA I/O pin (1)
100	P312 IN2_1 AN58	- - -	A	General-purpose I/O port Input capture ch.2 input pin (1) ADC analog 58 input pin
101	P313 IN3_1 AN59 INT10_1	- - - -	A	General-purpose I/O port Input capture ch.3 input pin (1) ADC analog 59 input pin INT10 external interrupt input pin (1)
102	P314 IN4_1 AN60 TIOA7_1	- - - -	A	General-purpose I/O port Input capture ch.4 input pin (1) ADC analog 60 input pin Base timer ch.7 TIOA I/O pin (1)
103	P315 IN5_1 AN61 TIOA8_1	- - - -	A	General-purpose I/O port Input capture ch.5 input pin (1) ADC analog 61 input pin Base timer ch.8 TIOA output pin (1)
104	P317 AN62 TIOA9_1 INT11_1	- - - -	A	General-purpose I/O port ADC analog 62 input pin Base timer ch.9 TIOA I/O pin (1) INT11 external interrupt input pin (1)
107	P321 PWUTRG	- -	R	General-purpose output port Partial wakeup trigger output pin
110	TRST P322	N -	J	JTAG test reset input pin General-purpose output port
111	TDO P323	- -	I	JTAG test data output pin General-purpose output port
112	TDI P324	- -	D	JTAG test data input pin General-purpose output port
113	TMS	-	E	JTAG test mode state input pin
114	TCK	-	E	JTAG test clock input pin
115	P327	-	P	General-purpose I/O port
116	P330	-	P	General-purpose I/O port

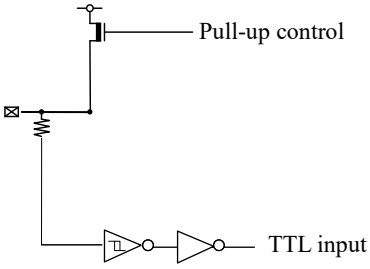
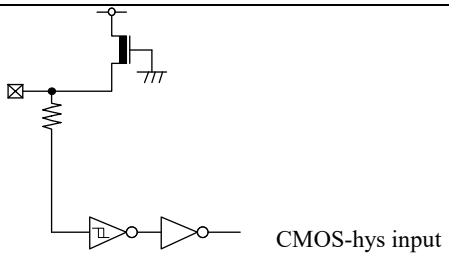
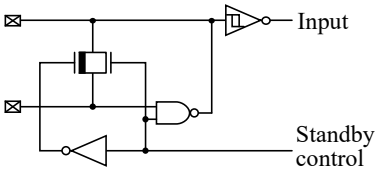
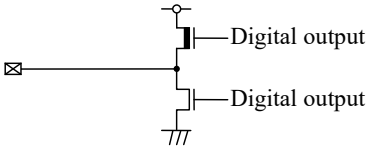
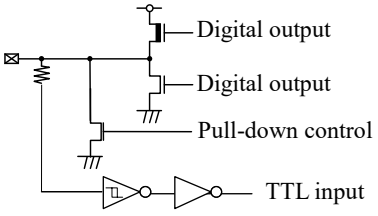
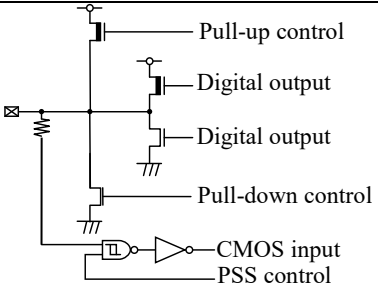
Pin No. S6J311xHAC	Pin Name	Polarity	I/O Circuit Type	Function
117	MD	-	C	Mode pin
118	X0	-	G	Main clock oscillation input pin
119	X1	-	G	Main clock oscillation output pin
121	P331	-	P	General-purpose I/O port
122	P400	-	P	General-purpose I/O port
123	RSTX	N	F	External reset input pin
127	P401 IN0_0	- -	Q	General-purpose I/O port Input capture ch.0 input pin (0)
128	P402 IN1_0 INT2_0	- - -	Q	General-purpose I/O port Input capture ch.1 input pin (0) INT2 external interrupt input pin (0)
129	P403 IN2_0 TRACEDATA0	- - -	Q	General-purpose I/O port Input capture ch.2 input pin (0) Trace data 0 output pin
130	P404 IN3_0 TRACEDATA1	- - -	Q	General-purpose I/O port Input capture ch.3 input pin (0) Trace data 1 output pin
131	P405 IN4_0 INT11_0 TRACEDATA2	- - - -	Q	General-purpose I/O port Input capture ch.4 input pin (0) INT11 external interrupt input pin (0) Trace data 2 output pin
132	P406 TRACEDATA3	- -	Q	General-purpose I/O port Trace data 3 output pin
133	P407 TRACEDATA4	- -	Q	General-purpose I/O port Trace data 4 output pin
134	P408 SIN2_0 INT12_0 TRACEDATA5	- - - -	Q	General-purpose I/O port Multi-function serial ch.2 serial data input pin (0) INT12 external interrupt input pin (0) Trace data 5 output pin
135	P409 SOT2_0 SDA2_0 TIOA24_1 TRACEDATA6	- - - - -	Q	General-purpose I/O port Multi-function serial ch.2 serial data output pin (0) I^2C bus ch.2 serial data I/O pin Base timer ch.24 TIOA output pin (1) Trace data 6 output pin
136	P411 SCK2_0 SCL2_0 INT13_1 TRACEDATA7	- - - - -	Q	General-purpose I/O port Multi-function serial ch.2 clock I/O pin (0) I^2C bus ch.2 serial clock I/O pin INT13 external interrupt input pin (1) Trace data 7 output pin
137	P413 SCS20_0 INT14_1	- - -	Q	General-purpose I/O port Multi-function serial ch.2 serial chip select 0 I/O pin (0) INT14 external interrupt input pin (1)
138	P414 SCS21_0	- -	Q	General-purpose I/O port Multi-function serial ch.2 serial chip select 1 output pin (0)
139	P416 IN5_0 TIOA22_1	- - -	Q	General-purpose I/O port Input capture ch.5 input pin (0) Base timer ch.22 TIOA output pin (1)
140	P417 TIOA23_1 INT15_1	- - -	Q	General-purpose I/O port Base timer ch.23 TIOA I/O pin (1) INT15 external interrupt input pin (1)
141	P418 SCS22_0 INT14_0	- - -	Q	General-purpose I/O port Multi-function serial ch.2 serial chip select 2 output pin (0) INT14 external interrupt input pin (0)

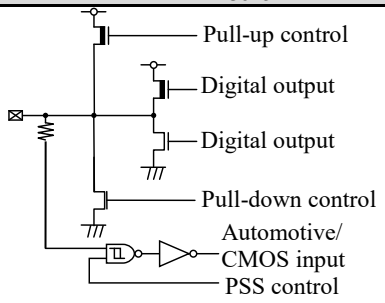
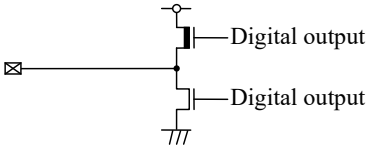
Pin No. S6J311xHAC	Pin Name	Polarity	I/O Circuit Type	Function
142	P420 SCK2_1 TRACECLK	- - -	Q	General-purpose I/O port Multi-function serial ch.2 clock I/O pin (1) Trace clock
143	P421 SIN2_1 TRACECTL	- - -	Q	General-purpose I/O port Multi-function serial ch.2 serial data input pin (1) Trace control
42	AVCC0	-	-	Analog power supply pin for AD converter unit 0
84	AVCC1	-	-	Analog power supply pin for AD converter unit 1
43	AVRH0	-	-	Upper-limit reference voltage pin for AD converter unit 0
83	AVRH1	-	-	Upper-limit reference voltage pin for AD converter unit 1
44	AVSS0 AVRL0	- -	-	GND pin for AD converter unit 0 Lower-limit reference voltage pin for AD converter unit 0
82	AVSS1 AVRL1	- -	-	GND pin for AD converter unit 1 Lower-limit reference voltage pin for AD converter unit 1
38	C	-	-	External capacity connection output pin
126				
36	VCC	-	-	Power supply pin
72				
105				
109				
124				
144				
1	VSS	-	-	GND
37				
73				
106				
108				
120				
125				

4. I/O Circuit Types

This section explains I/O circuit types.

Type	Circuit	Overview
A		General-purpose I/O port with analog input Output of 1 mA or 2 mA selectable 50 kΩ with pull-up resistor control 50 kΩ with pull-down resistor control CMOS hysteresis input
B		General-purpose I/O port with analog input Output of 1 mA or 2 mA selectable 50 kΩ with pull-up resistor control 50 kΩ with pull-down resistor control Automotive/CMOS hysteresis input selectable
C		Mode input CMOS hysteresis input
D		JTAG General-purpose output port Output of 2 mA 50 kΩ with pull-up resistor control TTL input

Type	Circuit	Overview
E		JTAG 50 kΩ with pull-up resistor control TTL input
F		CMOS hysteresis input 50 kΩ with pull-up resistor
G		Main oscillation I/O
I		JTAG Output of 2 mA
J		JTAG General-purpose output port Output of 2 mA 50 kΩ with pull-down resistor control TTL input
P		General-purpose I/O port Output of 1 mA or 2 mA selectable 50 kΩ with pull-up resistor control 50 kΩ with pull-down resistor control CMOS hysteresis input

Type	Circuit	Overview
Q		General-purpose I/O port Output of 1 mA or 2 mA selectable 50 kΩ with pull-up resistor control 50 kΩ with pull-down resistor control Automotive/CMOS hysteresis input selectable
R		Output of 2 mA

5. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

5.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

- Preventing Over-Voltage and Over-Current Conditions

  Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

- Protection of Output Pins

  Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

  Therefore, avoid this type of connection.

- Handling of Unused Input Pins

  Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

%○ Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

5.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product.
   Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 ˚C and 30 ˚C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125 ˚C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%.
   Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

5.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

6. Handling Devices

For Latch-up Prevention

The latch-up phenomenon may occur on a CMOS IC in the following cases: the voltage applied to an input or output pin is higher than V_{CC} or lower than V_{SS}; or the voltage applied between a VCC pin and a VSS pin exceeds the rating. A latch-up causes a rapid increase in the power supply current, possibly resulting in thermal damage to an element. When using the device, take sufficient care not to exceed the maximum rating.

Also be careful that analog power supplies (AVCC0, AVCC1, AVRH0, and AVRH1) and analog inputs do not exceed the digital power supply (VCC) at the analog system power-on and power-off times.
The power-on sequence is as follows. Simultaneously turn on the digital supply voltage (VCC) and analog supply voltages (AVCC0, AVCC1, AVRH0, and AVRH1), or turn on the digital supply voltage (VCC) and then the analog supply voltages (AVCC0, AVCC1, AVRH0, and AVRH1).

About Handling Unused Pins

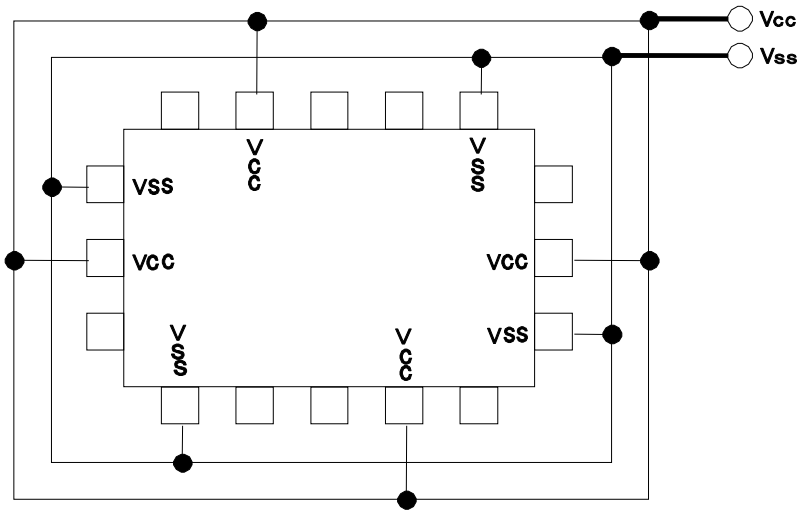
Leaving unused input pins open may cause permanent damage from a malfunction or latch-up. Take measures for unused pins, such as pulling up or pulling down the voltage with resistors of 2 kiloohms or higher.

If there are any unused input/output pins, set them to the output state and then open them, or set them to the input state and handle them in the same way as input pins.

About Power Supply Pins

If the device has multiple VCC and VSS pins, the device is designed in such a way that the pins that should be at the same potential are connected to each other inside the device to prevent malfunctions such as latch-up. However, to reduce unwanted emissions, prevent malfunctions of strobe signals caused by an increase of the ground level, and observe standards on total output current, be sure to connect all the VCC and VSS pins to the power source and ground externally. Also handle all the VSS power supply pins in this way as shown in the following diagram. If there are multiple VCC or VSS systems, the device does not operate normally even within the guaranteed operating range.

Figure 6-1. Pin Assignment



In addition, consider connecting with low impedance from the power supply source to the VCC and VSS of this device.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between the VCC pin and the VSS pin.

About the Crystal Oscillation Circuit

Noise entering the X0 or X1 pin may cause a malfunction. Design the printed circuit board in such a way that the X0 and X1 pins, the crystal oscillator (or ceramic resonator), and a bypass capacitor to ground are located very close to the device.

We recommend that the printed circuit board artwork have the X0 and X1 pins enclosed by ground.

About the Mode Pin (MD)
Use mode pin MD by directly connecting it to a VCC or VSS pin. To prevent noise from causing the device to accidentally enter test mode, reduce the pattern length between each mode pin and a VCC or VSS pin on the printed circuit board, and connect them with low impedance.

About the Power-on Time
To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic during power-on.

Point to Note during PLL Clock Operation
While a PLL clock is selected, if the oscillator breaks off or input stops, the PLL clock may continue operating with the free running frequency of the internal self-oscillator circuit. This operation is outside of the guaranteed range.

Power Supply Pin Processing of an A/D Converter
Even when no A/D converter is used, establish a connection such that AVCC = AVRH = VCC and AVSS/AVRL = VSS.

Points to Note about Using External Clocks
External clocks are not supported.

External direct clock input cannot be used.

Power-on Sequence of the Power Supply Analog Inputs of an A/D Converter
Be sure to turn on the digital power supply (VCC) before the application of the power supplies (AVCC, AVRH, and AVRL) and analog inputs (AN0 to AN3, AN5, AN6, AN9, AN10, AN12 to AN15, AN17 to AN24, and AN27 to AN62) of an A/D converter.
At the power-off time, turn off the power supplies and analog inputs of the A/D converter, and then turn off the digital power supply (VCC). Perform these power-on and power-off operations without AVRH exceeding AVCC. Even when using a pin shared with an analog input as an input port, do not allow the input voltage to exceed AVCC. (Turning on or off the analog supply voltage and digital supply voltage simultaneously is not a problem.)

About C Pin Processing
This device has a built-in voltage step-down circuit. Be sure to connect a capacitor to the C pin (pin 126 in S6J311xHAC* specifications) for internal stabilization of the device. For the standard values, see "Recommended operating conditions" in the latest data sheet.

*x: A/9

Precautions on Designing a Mounting Substrate
Measures against heat generation from the package must be taken for the mounting substrate to observe the absolute maximum rating (operating temperature). Design a mounting substrate with 4 or more layers. Connect the back of the package stage and the substrate pad with solder paste. Arrange thermal via holes on the substrate pad. For detailed information about mount conditions, contact your sales representative.

Notes on Writing to a Register Containing a Status Flag
In writing to a register containing a status flag (particularly an interrupt request flag, etc.) to control a function, it is important to take care not to accidentally clear the status flag.
Therefore, before the write operation, configure the status bit such that the flag is not cleared, and then set the control bit to the desired value.
Especially for control bits configured as a set of multiple bits, bit instructions cannot be used (bit instructions have only 1-bit access). In such cases, byte, half-word, or word access is used to write to the control bits and a status flag simultaneously. However, at this time, be careful not to accidentally clear bits other than the intended ones (the status flag bit in this case).

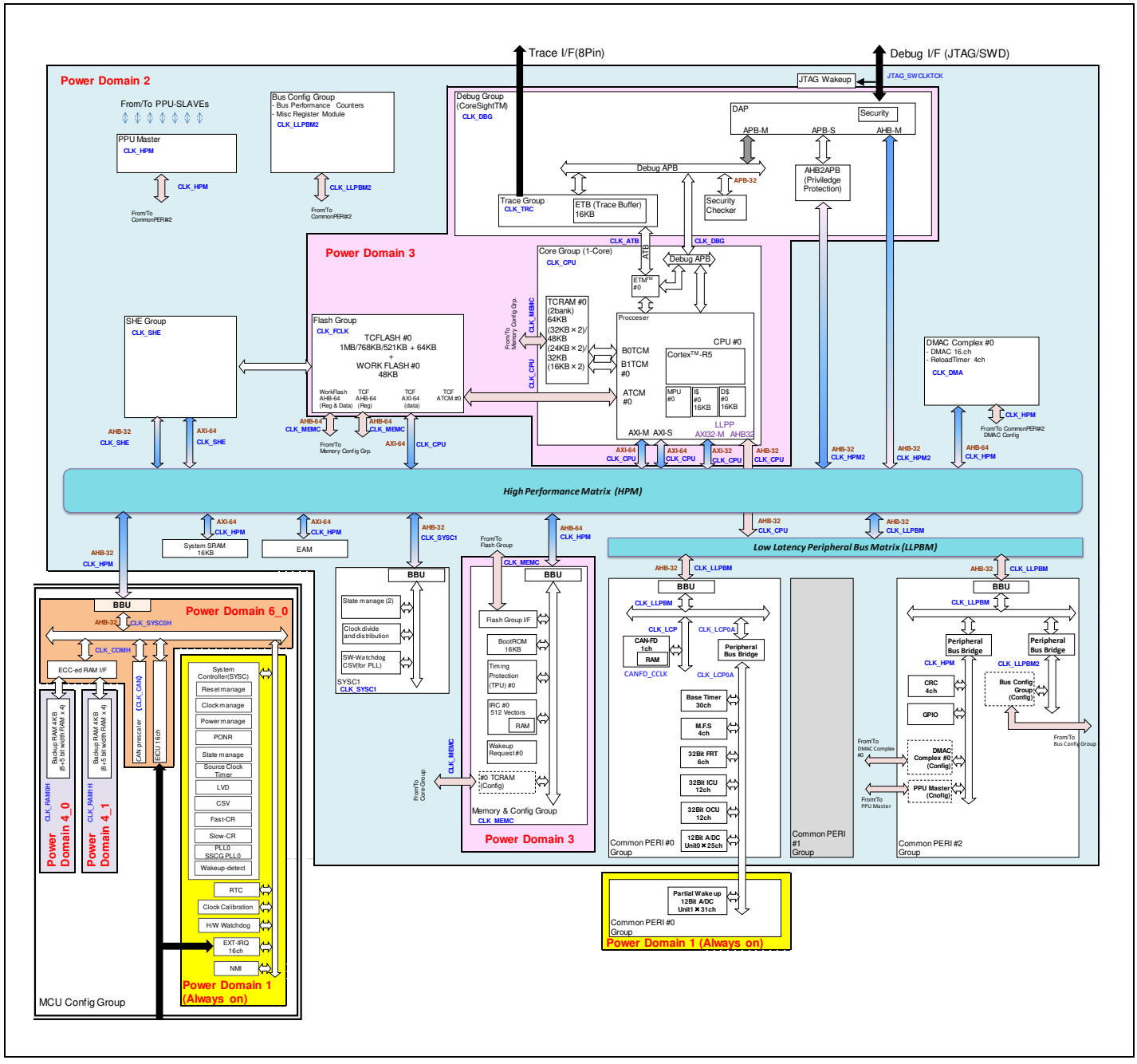
Note: Bit instructions take this point into account for registers that support bit-band units, so it does not need to be a concern. You need to take care when using bit instructions for registers that do not support bit-band units.

7. Block Diagram

This section provides block diagrams of the S6J3110 series.

Figure 7-1. S6J311xHAC* Block Diagram

* x: A/9



8. Memory Map

This section explains the memory map.

Figure 8-1. Memory Map (S6J311AHAC/9HAC)

*z:A

Address START	Address END	group	S6J311AHzC* part	S6J3119HzC* part
0x0000_0000	0x0000_7FFF		TCRAM (Main 64KByte)	TCRAM (Main 48KByte)
0x0000_8000	0x0000_BFFF			
0x0000_C000	0x0000_FFFF			Reserved
0x0001_0000	0x007F_FFFF		Reserved	Reserved
0x0080_0000	0x009E_FFFF		Reserved	Reserved
0x009F_0000	0x009F_FFFF		TCM_FLASH (Small Sector 8KByte×8)	TCM_FLASH (Small Sector 8KByte×8)
0x00A0_0000	0x00A7_FFFF		TCM_FLASH (Code 1MByte)	TCM_FLASH (Code 768KByte)
0x00A8_0000	0x00AB_FFFF			
0x00AC_0000	0x00AF_FFFF	Internal area for CR5 Complex		Reserved
0x00B0_0000	0x00DF_FFFF		Reserved	Reserved
0x00E0_0000	0x00FF_FFFF		Reserved	Reserved
0x0100_0000	0x019E_FFFF		Reserved	Reserved
0x019F_0000	0x019F_FFFF		AXI_FLASH_MEMORY (Small Sector 8KByte×8 *Mirror)	AXI_FLASH_MEMORY (Small Sector 8KByte×8 *Mirror)
0x01A0_0000	0x01A7_FFFF		AXI_FLASH_MEMORY (Code 1MByte *Mirror)	AXI_FLASH_MEMORY (Code 768KByte *Mirror)
0x01A8_0000	0x01AB_FFFF			
0x01AC_0000	0x01AF_FFFF			Reserved
0x01B0_0000	0x01DF_FFFF		Reserved	Reserved
0x01E0_0000	0x01FF_FFFF		Reserved	Reserved
0x0200_0000	0x0200_3FFF		SYSTEM SRAM (16KByte)	SYSTEM SRAM (16KByte)
0x0200_4000	0x0203_FFFF		Reserved	Reserved
0x0204_0000	0x027F_FFFF		Reserved	Reserved
0x0280_0000	0x0280_002F		Exclusive Access Memory	Exclusive Access Memory
0x0280_0030	0x03FF_FFFF		Reserved	Reserved
0x0400_0000	0x05FF_FFFF		AXI_SLAVE_CORE0	AXI_SLAVE_CORE0
0x0600_0000	0x0DFF_FFFF		Reserved	Reserved
0x0E00_0000	0x0E00_BFFF		WORK_FLASH (48KByte mirror area 1)	WORK_FLASH (48KByte mirror area 1)
0x0E00_C000	0x0E01_BFFF		Reserved	Reserved
0x0E01_C000	0x0E0F_FFFF		Reserved	Reserved
0x0E10_0000	0x0E1F_FFFF	Shared Flash and memory area	Reserved	Reserved
0x0E20_0000	0x0E20_BFFF		WORK_FLASH (48KByte mirror area 3)	WORK_FLASH (48KByte mirror area 3)
0x0E20_C000	0x0E21_BFFF		Reserved	Reserved
0x0E21_C000	0x0E2F_FFFF		Reserved	Reserved
0x0E30_0000	0x0E30_BFFF		WORK_FLASH (48KByte mirror area 4)	WORK_FLASH (48KByte mirror area 4)
0x0E30_C000	0x0E31_BFFF		Reserved	Reserved
0x0E31_C000	0x0E3F_FFFF		Reserved	Reserved
0x0E40_0000	0x0E7F_FFFF		Reserved	Reserved
0x0E80_0000	0x0E80_1FFF		Backup RAM 8KByte	Backup RAM 8KByte
0x0E80_2000	0x0E80_FFFF		Reserved	Reserved
0x0E81_0000	0x0E87_FFFF		Reserved	Reserved
0x0E88_0000	0x0FFF_FFFF		Reserved	Reserved
0x1000_0000	0xAFFF_FFFF	Reserved	Reserved	Reserved
0xB000_0000	0xB483_FFFF		Peri_area	Peri_area
0xB484_0000	0xB484_FFFF		APPS#5	APPS#5
0xB485_0000	0xB7FF_FFFF	Peri area	Peri_area	Peri_area
0xB800_0000	0xFFFE_DFFF	Reserved	Reserved	Reserved
0xFFFE_E000	0xFFFE_FFFF	ERRCFG	ERRCFG	ERRCFG
0xFFFF_0000	0xFFFF_3FFF	BootROM	BootROM	BootROM
0xFFFF_4000	0xFFFF_FFFF		Reserved	Reserved

Only the CPU core can access 0000_0000 ~ 01FF_FFFF. Bus masters other than the CPU core cannot access the region.

Internal area of CR5 complex (0000_0000 ~ 01FF_FFFF) is mapped to AXI_SLAVE_CORE0. All bus masters can access to internal area of CR5 complex via AXI_SLAVE_CORE0.

In each of the following memory area combinations, the areas are physically the same memory area.

1. TCM FLASH (0x00A0_0000 -) and AXI FLASH MEMORY (0x01A0_0000 -)

%○ TCM FLASH Small Sector (0x009F_0000 -) and AXI FLASH MEMORY Small Sector (0x019F_0000 -)

%○ WORKFLASH (0x0E00_0000 -), WORKFLASH (0x0E20_0000 -), and WORKFLASH (0x0E30_0000 -)

The ECC movement in TCM port is based on ECC setting inside the CPU.

■The differences between the TCM FLASH and AXI FLASH include the following.

Function	TCM FLASH	AXI FLASH
High-speed Access Using Dedicated Bus	Applicable	Not applicable
Write and Erase	Not applicable (Read-only)	Applicable
Read	Applicable	Applicable

■The differences between WORKFLASH areas include the following.

Area	Function
WORKFLASH Area 1	Used in write operation (with ECC)
WORKFLASH Area 3	Used in write operation (without ECC)
WORKFLASH Area 4	Used in read operation

■Terms are as follows.

Term	Description
TCM RAM	Main RAM
TCM FLASH	Program FLASH (TCM area)
AXI FLASH	Program FLASH (AXI area) This is physically the same as the TCM FLASH.
SYSTEM RAM	System RAM
AXI SLAVE CORE	AXI CPU control area
WORKFLASH	FLASH for work
BACKUP RAM	Backup RAM
Peri area	Entire area for peripheral functions
APPS#5	Part of area for peripheral functions
ERRCFG	Error configuration area
BootROM	ROM for reset boot

S6J311xHAC* Peripheral Map

* x: A/9

START Address	END Address	Group	Function	PPU No
B000_0000	B010_7FFF		Reserved	-
B010_8000	B010_80FF	SystemSRAM	SystemSRAM registers	-
B010_8100	B02F_FFFF		Reserved	-
B030_0000	B030_7FFF	SYSC1	System Controller #1	-
B030_8000	B03F_FFFF	SYSC1	SWDT	-
B040_0000	B040_7FFF	MEMORY_CONFIG_GROUP	IRC0	21
B040_8000	B040_FFFF	MEMORY_CONFIG_GROUP	TPU0	19
B041_0000	B041_0FFF	MEMORY_CONFIG_GROUP	TCRAM Control Status Register	16
B041_1000	B041_1FFF	MEMORY_CONFIG_GROUP	TCFlash Control Status Register	17
B041_2000	B041_20FF	MEMORY_CONFIG_GROUP	WFlash Control Status Register	18
B041_2100	B04F_FFFF		Reserved	-
B050_0000	B05F_FFFF		Reserved	-
B060_0000	B060_007F	MCU_CONFIG_GROUP	Protection register area	-
B060_0080	B060_00FF	MCU_CONFIG_GROUP	RUN profile register area	-
B060_0100	B060_017F	MCU_CONFIG_GROUP	PSS profile register area	-
B060_0180	B060_01FF	MCU_CONFIG_GROUP	APP profile register area	-
B060_0200	B060_027F	MCU_CONFIG_GROUP	STS profile register area	-
B060_0280	B060_02FF	MCU_CONFIG_GROUP	System register area	-
B060_0300	B060_037F	MCU_CONFIG_GROUP	CSV	-
B060_0380	B060_03FF	MCU_CONFIG_GROUP	RESET	-
B060_0400	B060_047F	MCU_CONFIG_GROUP	SCT(Fast CR)	34
B060_0480	B060_04FF	MCU_CONFIG_GROUP	SCT(Slow CR)	33
B060_0500	B060_05FF	MCU_CONFIG_GROUP	SCT(Main clock)	35
B060_0600	B060_067F	MCU_CONFIG_GROUP	Clock System	-
B060_0680	B060_06FF	MCU_CONFIG_GROUP	Special register area	-
B060_0700	B060_07FF	MCU_CONFIG_GROUP	Debug register area	-
B060_0800	B060_BFFF	MCU_CONFIG_GROUP	Mode	-
B060_C000	B060_FFFF	MCU_CONFIG_GROUP	HWDT	-
B061_0000	B061_7FFF		Reserved	-
B061_8000	B061_FFFF	MCU_CONFIG_GROUP	RTC	32
B062_0000	B063_FFFF	MCU_CONFIG_GROUP	EIC	-
B064_0000	B065_FFFF		Reserved	-
B066_0000	B067_FFFF		Reserved	-
B068_0000	B068_7FFF	MCU_CONFIG_GROUP	BURAMIF	-
B068_8000	B068_83FF	MCU_CONFIG_GROUP	EICU	37
B068_8400	B068_87FF	MCU_CONFIG_GROUP	CR_Calibration	38
B068_8800	B068_8BFF	MCU_CONFIG_GROUP	IRQ all	42
B068_8C00	B068_FFFF	MCU_CONFIG_GROUP	CAN Prescaler	43
B069_0000	B06F_FFFF		Reserved	-
B070_0000	B07F_FFFF		Reserved	-
B080_0000	B0FF_FFFF	Bit RMW alias	Bit RMW alias for MCU config Gr (Covers B060_0000 -- B06F_FFFF)	-
B100_0000	B10F_FFFF	Bit RMW alias	Bit RMW alias for SYSC1 (Covers B030_0000 -- B031_FFFF)	-
B110_0000	B11F_FFFF	Bit RMW alias	Bit RMW alias for MEMC (Covers B040_0000 -- B041_FFFF)	-
B120_0000	B1FF_FFFF		Reserved	-
B200_0000	B20F_FFFF	SHE	SHE configuration registers	63
B210_0000	B46F_FFFF		Reserved	-
B470_0000	B470_3FFF	CommonPERI #2	DMAC #0 registers	64
B470_4000	B470_FFFF		Reserved	-
B471_0000	B471_0FFF	CommonPERI #2	MPU for DMAC#0	66
B471_1000	B471_3FFF		Reserved	-
B471_4000	B471_4FFF	CommonPERI #2	DMA Complex #0 registers (Additional registers, RLTs)	68
B471_5000	B471_7FFF		Reserved	-
B471_8000	B471_83FF	CommonPERI #2	CRC#0	70
B471_8400	B471_87FF	CommonPERI #2	CRC#1	71
B471_8800	B471_8BFF	CommonPERI #2	CRC#2	72
B471_8C00	B471_8FFF	CommonPERI #2	CRC#3	73
B471_9000	B473_7FFF		Reserved	-
B473_8000	B473_FFFF	CommonPERI #2	GPIO	74
B474_0000	B474_7FFF	CommonPERI #2	PPC	75
B474_8000	B474_FFFF	CommonPERI #2	RIC	76
B475_0000	B475_7FFF	CommonPERI #2	PPU	-
B475_8000	B478_FBFF		Reserved	-
B478_FC00	B478_FFFF		Reserved	-
B479_0000	B47F_FFFF		Reserved	-

START Address	END Address	Group	Function	PPU No
B480_0000	B480_03FF	CommonPERI #0	M.F.Serial ch.0	176
B480_0400	B480_07FF	CommonPERI #0	M.F.Serial ch.1	177
B480_0800	B480_0BFF	CommonPERI #0	M.F.Serial ch.2	178
B480_0C00	B480_0FFF	CommonPERI #0	M.F.Serial ch.3	179
B480_1000	B480_7FFF		Reserved	-
B480_8000	B480_83FF	CommonPERI #0	BaseTimer ch.0	88
B480_8400	B480_87FF	CommonPERI #0	BaseTimer ch.1	89
B480_8800	B480_8BFF	CommonPERI #0	BaseTimer ch.2	90
B480_8C00	B480_8FFF	CommonPERI #0	BaseTimer ch.3	91
B480_9000	B480_93FF	CommonPERI #0	BaseTimer ch.4	92
B480_9400	B480_97FF	CommonPERI #0	BaseTimer ch.5	93
B480_9800	B480_9BFF	CommonPERI #0	BaseTimer ch.6	94
B480_9C00	B480_9FFF	CommonPERI #0	BaseTimer ch.7	95
B480_A000	B480_A3FF	CommonPERI #0	BaseTimer ch.8	96
B480_A400	B480_A7FF	CommonPERI #0	BaseTimer ch.9	97
B480_A800	B480_ABFF	CommonPERI #0	BaseTimer ch.10	98
B480_AC00	B480_AFFF	CommonPERI #0	BaseTimer ch.11	99
B480_B000	B481_FFFF		Reserved	-
B482_0000	B482_03FF	CommonPERI #0	FRT ch.0	208
B482_0400	B482_07FF	CommonPERI #0	FRT ch.1	209
B482_0800	B482_0BFF	CommonPERI #0	FRT ch.2	210
B482_0C00	B482_0FFF	CommonPERI #0	FRT ch.3	211
B482_1000	B482_13FF	CommonPERI #0	FRT ch.4	212
B482_1400	B482_17FF	CommonPERI #0	FRT ch.5	213
B482_1800	B482_7FFF		Reserved	-
B482_8000	B482_83FF	CommonPERI #0	ICU ch.0 / ch.1	224
B482_8400	B482_87FF	CommonPERI #0	ICU ch.2 / ch.3	225
B482_8800	B482_8BFF	CommonPERI #0	ICU ch.4 / ch.5	226
B482_8C00	B482_8FFF	CommonPERI #0	ICU ch.6 / ch.7	227
B482_9000	B482_93FF	CommonPERI #0	ICU ch.8 / ch.9	228
B482_9400	B482_97FF	CommonPERI #0	ICU ch.10 / ch.11	229
B482_9800	B482_FFFF		Reserved	-
B483_0000	B483_03FF	CommonPERI #0	OCU ch.0 / ch.1	240
B483_0400	B483_07FF	CommonPERI #0	OCU ch.2 / ch.3	241
B483_0800	B483_0BFF	CommonPERI #0	OCU ch.4 / ch.5	242
B483_0C00	B483_0FFF	CommonPERI #0	OCU ch.6 / ch.7	243
B483_1000	B483_13FF	CommonPERI #0	OCU ch.8 / ch.9	244
B483_1400	B483_17FF	CommonPERI #0	OCU ch.10 / ch.11	245
B483_1800	B483_FBFF		Reserved	-
B483_FC00	B483_FFFF		Reserved	-
B484_0000	B484_FFFF	APPS #5	APPS#5 area	-
B485_0000	B489_FFFF		Reserved	-
B48A_0000	B48B_0FFF		Reserved	-
B48B_1000	B48B_FBFF		Reserved	-
B48B_FC00	B48B_FFFF		Reserved	-
B48C_0000	B48F_FFFF		Reserved	-
B490_0000	B490_FFFF	CommonPERI #0	CAN_FD ch.0	256
B491_0000	B4BF_FFFF		Reserved	-
B4C0_0000	B4FF_FFFF	Bit RMW alias	Bit RMW alias for CPERI#0(Covers B490_0000 -- B497_FFFF)	-
B500_0000	B5FF_FFFF		Reserved	-
B600_0000	B6FF_FFFF		Reserved	-
B700_0000	B77F_FFFF	Bit RMW alias	Bit RMW alias for CPERI#2 (Covers B470_0000 -- B47F_FFFF)	-
B780_0000	B7BF_FFFF	Bit RMW alias	Bit RMW alias for CPERI#0 (Covers B480_0000 -- B487_FFFF)	-
B7C0_0000	B7FF_FFFF		Reserved	-
B800_0000	FFFE_DFFF		Reserved	-
FFFE_E000	FFFE_FBFC	Error Config	IRC	-
FFFE_FC00	FFFE_FFFF	Error Config	BootROM I/F	20

■APPS#5 area

START Address	END Address	Group	Function	PPU No
B484_0000	B484_37FF		Reserved	-
B484_3800	B484_3BFF	APPS #5	BaseTimer ch.12	278
B484_3C00	B484_3FFF	APPS #5	BaseTimer ch.13	279
B484_4000	B484_43FF	APPS #5	BaseTimer ch.14	280
B484_4400	B484_47FF	APPS #5	BaseTimer ch.15	281
B484_4800	B484_4BFF	APPS #5	BaseTimer ch.16	282
B484_4C00	B484_4FFF	APPS #5	BaseTimer ch.17	283
B484_5000	B484_53FF	APPS #5	BaseTimer ch.18	284
B484_5400	B484_57FF	APPS #5	BaseTimer ch.19	285
B484_5800	B484_5BFF	APPS #5	BaseTimer ch.20	286
B484_5C00	B484_5FFF	APPS #5	BaseTimer ch.21	287
B484_6000	B484_63FF	APPS #5	BaseTimer ch.22	288
B484_6400	B484_67FF	APPS #5	BaseTimer ch.23	289
B484_6800	B484_6BFF	APPS #5	BaseTimer ch.24	290
B484_6C00	B484_6FFF	APPS #5	BaseTimer ch.25	291
B484_7000	B484_73FF	APPS #5	BaseTimer ch.26	292
B484_7400	B484_77FF	APPS #5	BaseTimer ch.27	293
B484_7800	B484_7BFF	APPS #5	BaseTimer ch.28	294
B484_7C00	B484_7FFF	APPS #5	BaseTimer ch.29	295
B484_8000	B484_83FF	APPS #5	A/D unit0	296
B484_8400	B484_87FF	APPS #5	A/D unit1 , Partial Wake Up	297
B484_8800	B484_8BFF	APPS #5	A/D analog input control	298
B484_8C00	B484_8FFF		Reserved	-
B484_9000	B484_93FF	APPS #5	Global Timer	300
B484_9400	B484_FFFF		Reserved	-

When MPU attribute of Cortex®-R5 is configured as "Normal", store buffer inside Cortex®-R5 can operate and write data can be merged. To avoid influence of this data merger, MPU attribute "Device" or "Strongly Ordered" should be used.

MPU attribute "Device" or "Strongly Ordered" must be used for areas below, to avoid this influence.

- Backup RAM area (BACKUP_RAM) [0E80_0000 ~ 0E87_FFFF]
- Peripheral area (Peri area) [B000_0000 ~ B7FF_FFFF]
- Error Config area (ERRCFG) [FFFE_E000 ~ FFFE_FFFF]

MPU attribute "Device" or "Strongly Ordered" is required for accesses to areas below, in particular situation.

- FLASH Memory (when writing commands)

SHE OFF product is prohibited to access SHE area (B200_0000 to B20F_FFFF)

9. Pin Status in CPU Status

Table 9-1. Pin State Table (1/2)

Pin No.	Pin Name	GPORTEN Control	External Reset Factor 1			External Reset Factor 2				External Reset Factor 3		Internal Reset Factor *2	Sleep mode	Stop mode *4		Timer mode *4	
			External factor generation in progress	After external factor releasing		While Generating External Factor		After Releasing External Factor									
			Internal reset issuance in progress	Internal reset issuance in progress	After internal reset issuance (Before GPORT setting)	Before internal reset issuance	Internal reset issuance in progress	Internal reset issuance in progress	After internal reset issuance (Before GPORT setting)	Internal reset issuance in progress	After internal reset issuance (Before GPORT setting)		CPU Sleep	High impedance disabled (SYSCI0_SPECFGR: PSSPADCTRL=0)	High impedance enabled (SYSCI0_SPECFGR: PSSPADCTRL=1)	High impedance disabled (SYSCI0_SPECFGR: PSSPADCTRL=0)	High impedance enabled (SYSCI0_SPECFGR: PSSPADCTRL=1)
2	P000/SOT2_1	With control	Hi-Z/Input blocked			Hi-Z/ Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Status immediately before the shutdown retaine	Last state retained	Last state retained (*3)	Hi-Z/Input blocked	Last state retained (*3)	Hi-Z/Input blocked
3	P001/SCS20_1																
4	P003/SCS22_1																
5	P005/IN6_0/SIN3_0														Hi-Z/Input blocked		Hi-Z/Input blocked
6	P006/SOT3_0/SDA3_0/IN7_0																
7	P007/SCK3_0/SCL3_0/IN8_0																
8	P008/IN9_0/SCS30_0/TIOA0_0																
9	P009/IN10_0/TIOA1_0/INT0_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
10	P010/IN11_0/TIOA2_0														Hi-Z/Input blocked		Hi-Z/Input blocked
11	P012/OUT5_0/TIOA3_0																
12	P013/OUT6_0/TIOA4_0																
13	P015/OUT7_0/TIOA5_0																
14	P016/OUT8_0/TIOA6_0																
15	P017/OUT9_0/TIOA7_0																
16	P018/OUT10_0/TIOA8_0																
17	P019/OUT11_0/TIOB0_0/TEXT0_0																
18	P020/SOT0_0/SDA0_0/TEXT1_0/TIOB1_0																
19	P021/SCK0_0/SCL0_0/TIOB2_0																
20	P022/SIN0_0/TIOB3_0/INT3_0														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
21	P023/SCS0_0/TIOB4_0														Hi-Z/Input blocked		Hi-Z/Input blocked
22	P024/TIOB5_0																
23	P027/TIOA4_1/TIOB6_0/INT1_1/TEXT0_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
24	P028/OUT0_1/SIN1_0/TIOB7_0/INT4_0																
25	P029/AN0/SOT1_0/SDA1_0/OUT1_1														Hi-Z/Input blocked		Hi-Z/Input blocked
26	P030/OUT2_1																
27	P031/OUT3_1/SCS1_0/AN1																
28	P100/AN2/SCK1_0/SCL1_0/OUT4_1																
29	P101/OUT5_1/AN3																
30	P103/OUT6_1/AN5																
31	P105/OUT7_1/TIOA9_0																
32	P106/OUT8_1																
33	P107/OUT9_1/TIOA10_0/INT2_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
34	P108/OUT10_1/AN6/TIOA11_0/INT3_1																
35	P109/OUT11_1/TIOA12_0																
39	P112/AN9/TIOA13_0														Hi-Z/Input blocked		Hi-Z/Input blocked
40	P113/TIOA5_1																
41	P114/AN10/TIOA6_1																
45	P115																
46	P117/AN12/INT4_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
47	P118/AN13/INT5_1																
48	P119/AN14														Hi-Z/Input blocked		Hi-Z/Input blocked
49	P120/AN15																
50	P122/AN17/TIOA11_1																
51	P123/AN18/TIOA12_1																
52	P126/AN19																
53	P127/AN20/TEXT1_1																
54	P128/AN21/TEXT2_1																
55	P129/IN6_1/AN22																
56	P130/IN7_1/AN23/INT5_0														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
57	P131/IN8_1/AN24														Hi-Z/Input blocked		Hi-Z/Input blocked
58	P202/IN9_1/INT6_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
59	P203/IN10_1																
60	P204/IN11_1/AN27														Hi-Z/Input blocked		Hi-Z/Input blocked
61	P205/AN28/TEXT3_1																
62	P206/AN29/TEXT4_1																
63	P207/AN30/INT7_1/TEXT5_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
64	P208/AN31/TIOA19_0														Hi-Z/Input blocked		Hi-Z/Input blocked
65	P209/AN32/TIOA20_0																
66	P210/IN0_2/AN33/TIOA21_0/INT6_0														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
67	P211/IN1_2/AN34/TIOA22_0														Hi-Z/Input blocked		Hi-Z/Input blocked
68	P212/IN2_2/AN35/TIOA13_1																
69	P213/IN3_2/TIOA14_1/INT8_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
70	P214/IN4_2/TIOA15_1														Hi-Z/Input blocked		Hi-Z/Input blocked
71	P215/IN5_2/TIOA16_1/INT9_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)

Table 9-2. Pin State Table (2/2)

Pin No.	Pin Name	GPORTEN Control	External Reset Factor 1			External Reset Factor 2				External Reset Factor 3		Internal Reset Factor *2	Sleep mode	Stop mode *4		Timer mode *4	
			External factor generation in progress	After external factor releasing		While Generating External Factor		After Releasing External Factor									
			Internal reset issuance in progress	Internal reset issuance in progress	After internal reset issuance (Before GPORT setting)	Before internal reset issuance	Internal reset issuance in progress	Internal reset issuance in progress	After internal reset issuance (Before GPORT setting)	Internal reset issuance in progress	After internal reset issuance (Before GPORT setting)		CPU Sleep	High impedance disabled (SYSC0_SPECFGR. PSSPADCTRL=0)	High impedance enabled (SYSC0_SPECFGR. PSSPADCTRL=1)	High impedance disabled (SYSC0_SPECFGR. PSSPADCTRL=0)	High impedance enabled (SYSC0_SPECFGR. PSSPADCTRL=1)
74	P218/AN36/TEXT2_0	With control	Hi-Z/Input blocked			Hi-Z/ Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Status immediately before the shutdown retaine	Last state retained	Last state retained (*3)	Hi-Z/Input blocked	Last state retained (*3)	Hi-Z/Input blocked
75	P219/AN37/TEXT3_0																
76	P220/IN6_2/AN38																
77	P222/IN7_2/AN39/INT7_0														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
78	P223/IN8_2/AN40/PWU_AN0														Hi-Z/Input blocked		Hi-Z/Input blocked
79	P224/IN9_2/TX0_2/AN41/PWU_AN1																
80	P225/IN10_2/RX0_2/AN42/INT0_0/PWU_AN2														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
81	P226/IN11_2/AN43/TIOA17_1/PWU_AN3																
85	P227/AN44/TIOA23_0/PWU_AN4														Hi-Z/Input blocked		Hi-Z/Input blocked
86	P228/TX0_1/AN45/TIOA24_0/PWU_AN5																
87	P229/OUT0_0/RX0_1/AN46/TIOA25_0/INT8_0/PWU_AN6														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
88	P230/OUT1_0/AN47/TIOA26_0/PWU_AN7																
89	P231/OUT2_0/AN48/TIOA27_0														Hi-Z/Input blocked		Hi-Z/Input blocked
90	P300/OUT3_0/AN49/TIOA28_0																
91	P301/OUT4_0/AN50/TIOA18_1																
92	P302/AN51/TIOA19_1																
93	P304/AN52/TIOA20_1/TEXT4_0																
94	P305/AN53/TIOA29_0/TEXT5_0																
95	NMIX	-	Input enabled			Input enabled		Input enabled		Input enabled		Input enabled	Input enabled	Input enabled		Input enabled	
96	P306/TX0_0/AN54	With control	Hi-Z/Input blocked			Hi-Z /Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Status immediately before the shutdown retaine	Last state retained	Last state retained (*3)	Hi-Z/Input blocked	Last state retained (*3)	Hi-Z/Input blocked
97	P307/RX0_0/AN55/INT1_0														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
98	P308/IN0_1/AN56/TIOA28_1																
99	P309/IN1_1/AN57/TIOA29_1														Hi-Z/Input blocked		Hi-Z/Input blocked
100	P312/IN2_1/AN58																
101	P313/IN3_1/AN59/INT10_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
102	P314/IN4_1/AN60/TIOA7_1														Hi-Z/Input blocked		Hi-Z/Input blocked
103	P315/IN5_1/AN61/TIOA8_1																
104	P317/AN62/TIOA9_1/INT11_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
107	P321/PWUTRG	-	Hi-Z/Input blocked			Hi-Z/Input blocked		Hi-Z/Input blocked		Hi-Z/Input blocked		Hi-Z/Input blocked *7 (Status immediately before the shutdown retaine) *6 (PWUTRG output/Input blocked *5)	Hi-Z/Input blocked *7 (Last state retained) *6 (PWUTRG output/Input blocked *5)	Hi-Z/Input blocked *7 (Last state retained) *6 (PWUTRG output/Input blocked *5)	Hi-Z/Input blocked	Hi-Z/Input blocked *7 (Last state retained) *3 *6 (*5)	Hi-Z/Input blocked
110	TRST/P322		Input enabled			Input enabled		Input enabled		Input enabled		Input enabled (Status immediately before the shutdown retaine) *6	Input enabled (Last state retained) *6	Input enabled (Last state retained (*3)) *6	Input enabled (Hi-Z/Input blocked) (*6)	Input enabled (Last state retained (*3)) *6	Input enabled (Hi-Z/Input blocked) (*6)
111	TDO/P323		-			-		-		-							
112	TDI/P324		Input enabled			Input enabled		Input enabled		Input enabled							
113	TMS											Input enabled	Input enabled	Input enabled		Input enabled	
114	TCK																
115	P327	With control	Hi-Z/Input blocked			Hi-Z /Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Status immediately before the shutdown retaine	Last state retained	Last state retained (*3)	Hi-Z/Input blocked	Last state retained (*3)	Hi-Z/Input blocked
116	P330																
117	MD	-	Input enabled			Input enabled		Input enabled		Input enabled		Input enabled	Input enabled	Input enabled		Input enabled	
118	X0		-			-		-		-		-	-	-		-	
119	X1																
121	P331	With control	Hi-Z/Input blocked			Hi-Z /Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Status immediately before the shutdown retaine	Last state retained	Last state retained (*3)	Hi-Z/Input blocked	Last state retained (*3)	Hi-Z/Input blocked
122	P400																
123	RSTX	-	Input enabled			Input enabled		Input enabled		Input enabled		Input enabled	Input enabled	Input enabled		Input enabled	
127	P401/IN0_0	With control	Hi-Z/Input blocked			Hi-Z /Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Status immediately before the shutdown retaine	Last state retained	Last state retained (*3)	Hi-Z/Input blocked	Last state retained (*3)	Hi-Z/Input blocked
128	P402/IN1_0/INT2_0														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
129	P403/IN2_0/TRACEDATA0														Hi-Z/Input blocked		Hi-Z/Input blocked
130	P404/IN3_0/TRACEDATA1																
131	P405/IN4_0/INT11_0/TRACEDATA2														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
132	P406/TRACEDATA3														Hi-Z/Input blocked		Hi-Z/Input blocked
133	P407/TRACEDATA4																
134	P408/SIN2_0/INT12_0/TRACEDATA5														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
135	P409/SOT2_0/SDA2_0/TIOA24_1/TRACEDATA6														Hi-Z/Input blocked		Hi-Z/Input blocked
136	P411/INT13_1/SCK2_0/SCL2_0/TRACEDATA7														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
137	P413/SCS20_0/INT14_1																
138	P414/SCS21_0														Hi-Z/Input blocked		Hi-Z/Input blocked
139	P416/IN5_0/TIOA22_1																
140	P417/TIOA23_1/INT15_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
141	P418/SCS22_0/INT14_0																
142	P420/SCK2_1/TRACECLK														Hi-Z/Input blocked		Hi-Z/Input blocked
143	P421/SIN2_1/TRACECTL																

*1: Input disable is not valid when external interrupts are enabled.

*2: Recovery from standby (power off) becomes a factor.

*3: The pin state from the time that HOLDIO_PD2 was set (SYSC0_SPECFGR.HOLDIO_PD2 = 1) is retained. If power-off has not occurred and HOLDIO_PD2 has not been set (SYSC0_SPECFGR.HOLDIO_PD2 = 0), the last state is retained.

*4: To power off power domains 2 and 3, be sure to set HOLDIO_PD2 (SYSC0_SPECFGR.HOLDIO_PD2 = 1).

*5: When the PWU function is enabled, a change to output occurs.

*6: The pin state when the PORT function is enabled is shown.

*7: When PPC_PCFGRijj:POF[2:0] is set to initial value.

■External Reset Factor 1

Power-on reset (PONR)

RAM retention low-voltage detection reset (RVD)

Internal power supply low-voltage detection reset (LVDL1R)

RSTX pin + MD pin simultaneous assert reset (INITX)

■External Reset Factor 2

RSTX pin input reset (RSTX)

■External Reset Factor 3

Hardware watchdog reset (HWDR)

Software watchdog reset (SWDR)

PLL clock supervisor reset (CSVPRn)

SSCG clock supervisor reset (CSVSRn)

Profile error reset (PRFERR)

Software trigger hard reset (SHRST)

Software reset (SRST)

■Internal Reset Factor

Standby transition reset/ Power domain reset

10. Electrical Characteristics

10.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	
Analog supply voltage*1, *2	AV_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	$AV_{CC} = V_{CC}$
Analog reference voltage*1	AVRH	V_{SS}-0.3	V_{SS}+6.0	V	$AVRH \leq AV_{CC}$
Input voltage*1	V_I	V_{SS}-0.3	V_{CC}+0.3	V	
Analog pin input voltage*1	V_{IA}	V_{SS}-0.3	V_{CC}+0.3	V	
Output voltage*1	V_O	V_{SS}-0.3	V_{CC}+0.3	V	
Maximum clamp current	$\|I_{CLAMP}\|$	-	4	mA	*7
Total maximum clamp current	$\Sigma\|I_{CLAMP}\|$	-	20	mA	*7
"L"-level maximum output current*3	I_{OL1}	-	3.5	mA	When setting is 1 mA*6
	I_{OL2}	-	7	mA	When setting is 2 mA
"L"-level average output current*4	I_{OLAV1}	-	1	mA	When setting is 1 mA*6
	I_{OLAV2}	-	2	mA	When setting is 2 mA
"L"-level total output current*5	ΣI_{OL}	-	40	mA	*6
"H"-level maximum output current*3	I_{OH1}	-	-3.5	mA	When setting is 1 mA*6
	I_{OH2}	-	-7	mA	When setting is 2 mA
"H"-level average output current*4	I_{OHAV1}	-	-1	mA	When setting is 1 mA*6
	I_{OHAV2}	-	-2	mA	When setting is 2 mA
"H"-level total output current*5	ΣI_{OH}	-	-40	mA	*6
Power consumption	P_D	-	1300	mW	S6J311xHAC*8
Operating temperature	T_A	-40	+125	°C	
Storage temperature	Tstg	-55	+150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0.0$ V.

*2: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current X the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

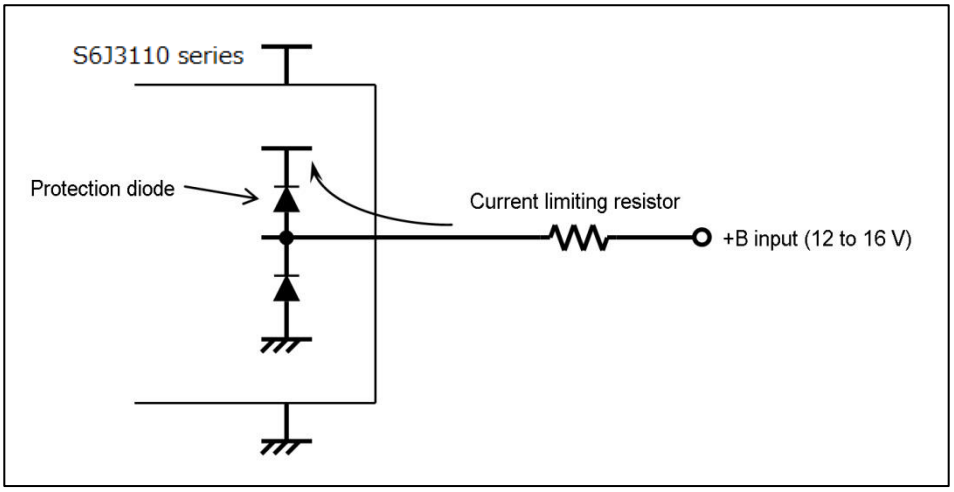
*6: Corresponding pins: general-purpose ports

*7: Corresponding pins: All general-purpose ports and analog input pins

- Use the device within the recommended operating conditions.
- Use the device with direct voltage (current).
- The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
- Note that when the microcontroller drive current is low, such as in the low-power consumption modes, the + B input potential can increase the potential at the VCC pin via a protective diode, possibly affecting other devices.
- Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave + B input pins open.

*8: It is standard when four-layer substrate is used. x : A/9

Example of a recommended circuit



WARNING:

- Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

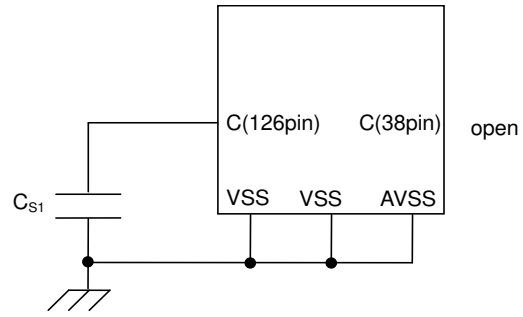
10.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Supply voltage	V_{CC}	4.5	5.25	V	Recommended operation assurance range
	AV_{CC}	4.5	5.25	V	
	V_{CC}	3.5	5.25	V	Operation assurance range
	AV_{CC}	3.5	5.25	V	
Smoothing capacitor*	C_{S1}	4.7		µF	Tolerance of up to ±40%, 126-pin Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than CS as the smoothing capacitor on the VCC pin.
Operating temperature	T_A	-40	+125	°C	S6J311xHAC* * x:A/9

*: For the connections of smoothing capacitor C_{S1}, see the following diagram.

· ***C pin connection diagram***



WARNING:

1. The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
2. Any use of semiconductor devices will be under their recommended operating condition.
3. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
4. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

Notes:

- *The following condition should be satisfied in order to facilitate heat dissipation.*

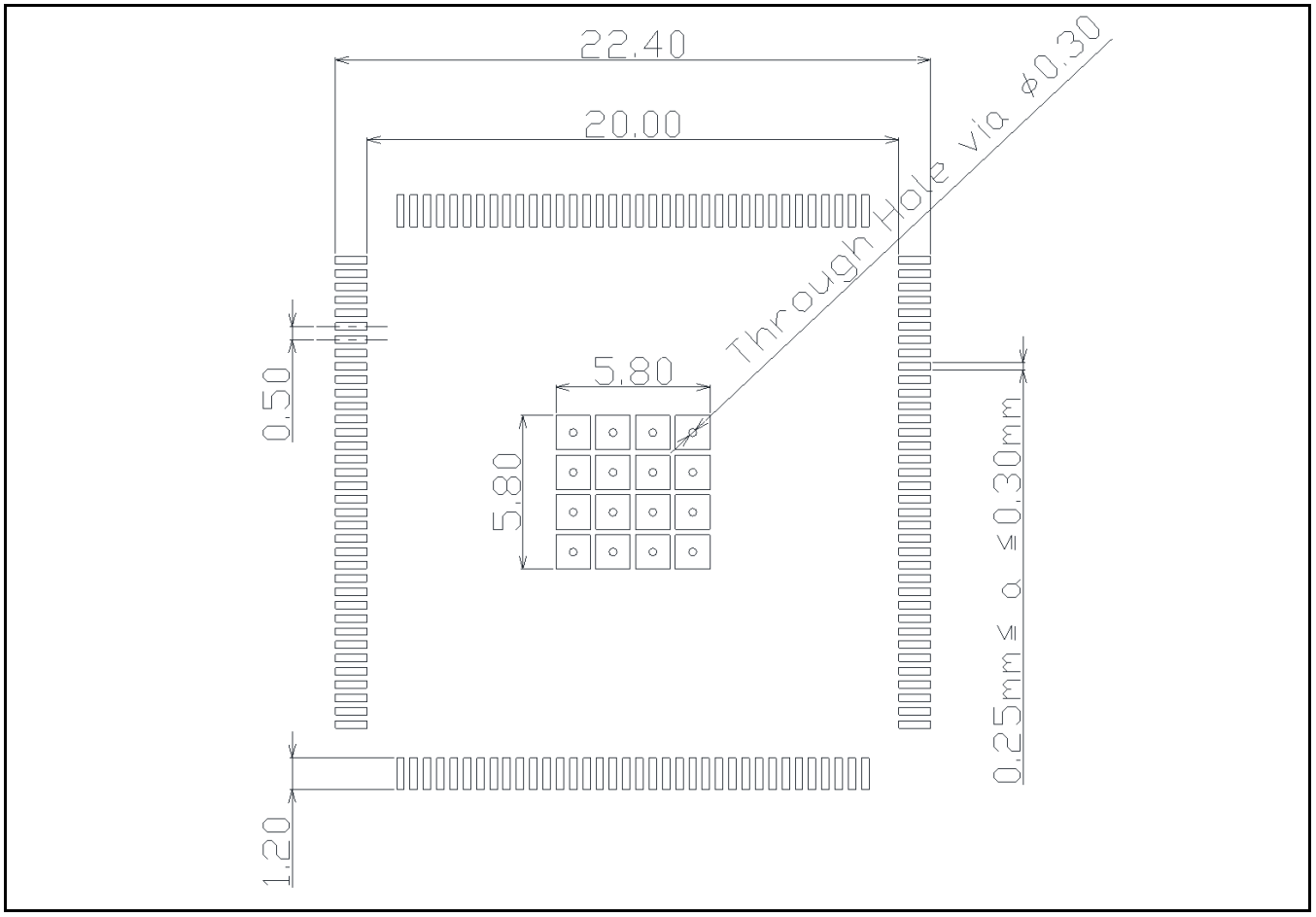
1. *4 or more layers PCB should be used.*
2. *The area of PCB should be 114.3 mm x 76.2 mm or more, and the thickness should be 1.6 mm or more. (JEDEC standard)*
3. *1 layer of middle layers at least should be used for dedicated layer to radiate heat with residual copper rate 90% or more. The layer can be used for system ground.*
4. *35~50% of the die stage area which is exposed at back surface of package should be soldered to a part of 1st layer.*
5. *The part of 1st layer should be connected to the dedicated heat radiation layer with more than 10 thermal via holes.*

Figure10.2-1: Example thermal via holes on PCB.

Notes:

- *Figure 10.2-1 is a schematic diagram showing PCB in section.*
- *Figure 10.2-2 in the following pages are recommended land patterns for each package series. Thermal via holes should closely be placed and aligned with lands.*
- *If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.*

Figure 10.2-2: Land Pattern and Thermal Via LEU144



10.3 DC Characteristics

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	P000 to P001, P003, P005 to P010, P012 to P013, P015 to P024, P027 to P031, P100 to P101, P103, P105 to P109, P112 to P115, P117 to P120, P122 to P123, P126 to P131, P202 to P215, P218 to P220, P222 to P231, P300 to P302, P304 to P309, P312 to P315, P317, P327, P330 to P331, P400 to P409, P411, P413 to P414, P416 to P418, P420 to P421	CMOS Schmitt input level selected	0.7×V_{CC}	-	V_{CC}+0.3	V	
	V_{IH2}	P401 to P409, P411, P413 to P414, P416 to P418, P420 to P421	Automotive input level selected	0.8×V_{CC}	-	V_{CC}+0.3	V	
	V_{IH4}	RSTX, NMIX	-	0.7×V_{CC}	-	V_{CC}+0.3	V	
	V_{IH5}	MD	-	0.7×V_{CC}	-	V_{CC}+0.3	V	
	V_{IH6}	TRST, TCK, TDI, TMS	TTL input level	2.3	-	V_{CC}+0.3	V	
"L" level input voltage	V_{IL1}	P000 to P001, P003, P005 to P010, P012 to P013, P015 to P024, P027 to P031, P100 to P101, P103, P105 to P109, P112 to P115, P117 to P120, P122 to P123, P126 to P131, P202 to P215, P218 to P220, P222 to P231, P300 to P302, P304 to P309, P312 to P315, P317, P327, P330 to P331, P400 to P409, P411, P413 to P414, P416 to P418, P420 to P421	CMOS Schmitt input level selected	V_{SS}-0.3	-	0.3×V_{CC}	V	
	V_{IL2}	P401 to P409, P411, P413 to P414, P416 to P418, P420 to P421	Automotive input level selected	V_{SS}-0.3	-	0.5×V_{CC}	V	
	V_{IL4}	RSTX, NMIX	-	V_{SS}-0.3	-	0.3×V_{CC}	V	
	V_{IL5}	MD	-	V_{SS}-0.3	-	0.3×V_{CC}	V	
	V_{IL6}	TRST, TCK, TDI, TMS	TTL input level	V_{SS}-0.3	-	0.8	V	

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH1}	P000 to P001, P003, P005 to P010, P012 to P013, P015 to P024, P027 to P031, P100 to P101, P103, P105 to P109, P112 to P115, P117 to P120, P122 to P123, P126 to P131, P202 to P215, P218 to P220, P222 to P231, P300 to P302, P304 to P309, P312 to P315, P317, P321 to P324, P327, P330 to P331, P400 to P409, P411, P413 to P414, P416 to P418, P420 to P421	V_{CC} = 4.5 V I_{OH} = -2.0 mA	V_{CC}-0.5	-	V_{CC}	V	
"H" level output voltage	V_{OH2}	P000 to P001, P003, P005 to P010, P012 to P013, P015 to P024, P027 to P031, P100 to P101, P103, P105 to P109, P112 to P115, P117 to P120, P122 to P123, P126 to P131, P202 to P215, P218 to P220, P222 to P231, P300 to P302, P304 to P309, P312 to P315, P317, P321 to P324, P327, P330 to P331, P400 to P409, P411, P413 to P414, P416 to P418, P420 to P421	V_{CC} = 4.5 V I_{OH} = -1.0 mA	V_{CC}-0.5	-	V_{CC}	V	
"L" level output voltage	V_{OL1}	P000 to P001, P003, P005 to P010, P012 to P013, P015 to P024, P027 to P031, P100 to P101, P103, P105 to P109, P112 to P115, P117 to P120, P122 to P123, P126 to P131, P202 to P215, P218 to P220, P222 to P231, P300 to P302, P304 to P309, P312 to P315, P317, P321 to P324, P327, P330 to P331, P400 to P409, P411, P413 to P414, P416 to P418, P420 to P421	V_{CC} = 4.5 V I_{OL} = 2.0 mA	0	-	0.4	V	
"L" level output voltage	V_{OL2}	P000 to P001, P003, P005 to P010, P012 to P013, P015 to P024, P027 to P031, P100 to P101, P103, P105 to P109, P112 to P115, P117 to P120, P122 to P123, P126 to P131, P202 to P215, P218 to P220, P222 to P231, P300 to P302, P304 to P309, P312 to P315, P317, P321 to P324, P327, P330 to P331, P400 to P409, P411, P413 to P414, P416 to P418, P420 to P421	V_{CC} = 4.5 V I_{OL} = 1.0 mA	0	-	0.4	V	

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current	I_{IL}	All input pins	V_{CC} = AV_{CC} = 5.25 V V_{SS} < VI < V_{CC}	-5	-	+5	µA	
Pull-up resistor	R_{UP1}	RSTX, NMIX	-	25	-	100	kΩ	
	R_{UP2}	P000 to P001, P003, P005 to P010, P012 to P013, P015 to P024, P027 to P031, P100 to P101, P103, P105 to P109, P112 to P115, P117 to P120, P122 to P123, P126 to P131, P202 to P215, P218 to P220, P222 to P231, P300 to P302, P304 to P309, P312 to P315, P317 P327, P330 to P331, P400 to P409, P411, P413 to P414, P416 to P418, P420 to P421	Pull-up resistor selected	25	-	100	kΩ	
	R_{UP3}	TDI(P324), TMS, TCK	-	25	-	100	kΩ	
Pull-down resistor	R_{DOWN1}	P000 to P001, P003, P005 to P010, P012 to P013, P015 to P024, P027 to P031, P100 to P101, P103, P105 to P109, P112 to P115, P117 to P120, P122 to P123, P126 to P131, P202 to P215, P218 to P220, P222 to P231, P300 to P302, P304 to P309, P312 to P315, P317 P327, P330 to P331, P400 to P409, P411, P413 to P414, P416 to P418, P420 to P421	Pull-down resistor selected	25	-	100	kΩ	
	R_{DOWN2}	TRST(P322)	-	25	-	100	kΩ	
Input capacitance	C_{IN}	Pins other than VCC, VSS, AVCC0, AVCC1, AVSS0, AVSS1	-	-	5	15	pF	

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current S6J311xHAC* *x: A/9	I_{CC5}	VCC	Normal operation	-	80	175	mA	Operating at 96 MHz
			Flash write/erase	-	100	200	mA	Operating at 96 MHz
	I_{CCS5}		CPU Sleep	-	65	150	mA	Operating at 96 MHz
	I_{CCT5}		Timer mode	-	480	1450	µA	T_A = 25 °C Slow-CR source Oscillation
	I_{CCH5}		Stop mode	-	480	1450	µA	T_A = 25 °C
	I_{CCP}		PWU mode (Shutdown)	-	52.5	129.7	µA	T_A = 25 °C (PWU operation cycle 16 ms)
				-	46.2	115.5	µA	T_A = 25 °C (PWU operation cycle 32 ms)
	I_{CCT52}		Timer mode (Shutdown)	-	40	100	µA	T_A = 25 °C Slow-CR source Oscillation
	I_{CCH52}		Stop mode (Shutdown)	-	40	100	µA	T_A = 25 °C

Refer to Hardware manual "APPENDIX State transition" for Internal clock frequency setting / Setting of the power domain / Regulator setting.

10.4 AC Characteristics

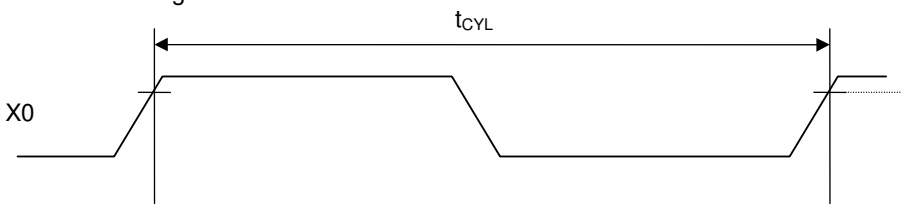
10.4.1 Source Clock Timing

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_C	X0, X1	-	-	4	-	MHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1	-	-	250	-	ns	
CAN PLL jitter (during lock)	t_{PJ}	-	-	-10	-	+10	ns	*
Built-in slow-CR oscillation frequency	F_{CRS}	-	-	50	100	150	kHz	
Built-in fast-CR oscillation frequency	F_{CRF}	-	-	2.4	4	6.0	MHz	
PLL input clock frequency	F_{PLLI}	-	-	-	4	-	MHz	
PLL macro oscillation clock frequency	F_{PLLO}	-	-	400	-	576	MHz	
SSCG-PLL input clock frequency	$F_{SSCGPLLI}$	-	-	-	4	-	MHz	
SSCG-PLL macro oscillation clock frequency	$F_{SSCGPLLO}$	-	-	400	-	576	MHz	

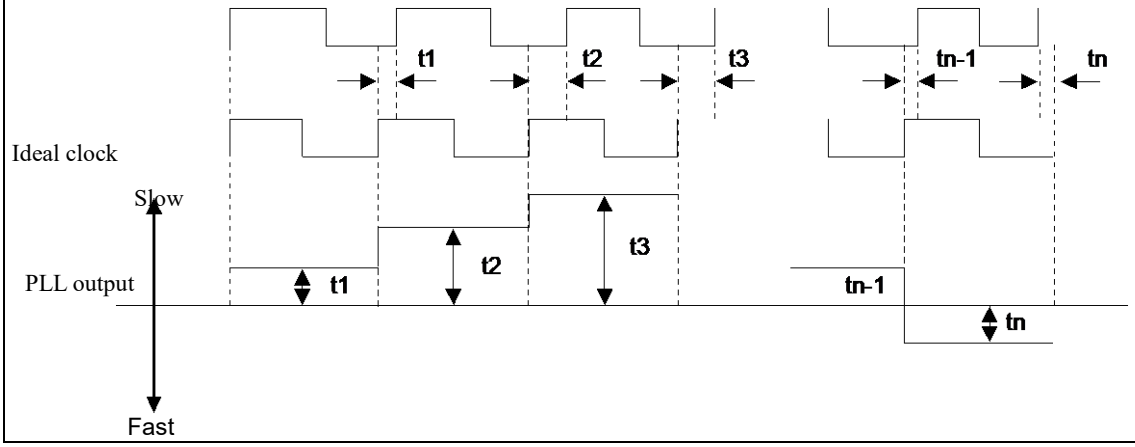
*: The maximum/minimum values have been standardized with the main clock and PLL clock in use.

• X0 and X1 clock timing



• CAN PLL jitter

A time difference from the ideal clock is guaranteed for each cycle period within 20,000 cycles.



10.4.2 Internal Clock Timing

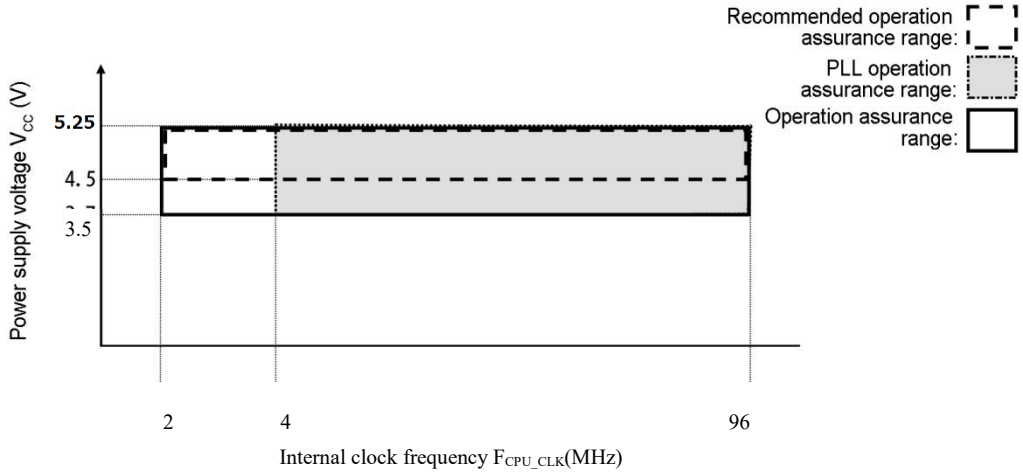
(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	S6J311xHAC* Value * x:A/9			Unit	Remarks
				Min	Typ	Max		
Internal Clock Frequency	F_{CLK_CPU}	-	-	-	-	96	MHz	CLK_CPU
	F_{CLK_FCLK}	-	-	-	-	48	MHz	CLK_FCLK
	F_{CLK_ATB}	-	-	-	-	48	MHz	CLK_ATB
	F_{CLK_DBG}	-	-	-	-	48	MHz	CLK_DBG
	F_{CLK_HPM}	-	-	-	-	24	MHz	CLK_HPM
	F_{CLK_HPM2}	-	-	-	-	12	MHz	CLK_HPM2
	F_{CLK_DMA}	-	-	-	-	24	MHz	CLK_DMA
	F_{CLK_MEMC}	-	-	-	-	24	MHz	CLK_MEMC
	F_{CLK_EXTBUS}	-	-	-	-	24	MHz	CLK_EXTBUS
	F_{CLK_SYSC1}	-	-	-	-	24	MHz	CLK_SYSC1
	$F_{CLK\_HAPP0A0}$	-	-	-	-	24	MHz	CLK_HAPP0A0
	$F_{CLK\_HAPP0A1}$	-	-	-	-	24	MHz	CLK_HAPP0A1
	$F_{CLK\_HAPP1B0}$	-	-	-	-	24	MHz	CLK_HAPP1B0
	$F_{CLK\_HAPP1B1}$	-	-	-	-	24	MHz	CLK_HAPP1B1
	F_{CLK_LLPBM}	-	-	-	-	96	MHz	CLK_LLPBM
	F_{CLK_LLPBM2}	-	-	-	-	48	MHz	CLK_LLPBM2
	F_{CLK_LCP}	-	-	-	-	48	MHz	CLK_LCP
	F_{CLK_LCP0}	-	-	-	-	24	MHz	CLK_LCP0
	F_{CLK_LCP0A}	-	-	-	-	24	MHz	CLK_LCP0A
	F_{CLK_LCP1}	-	-	-	-	24	MHz	CLK_LCP1
	F_{CLK_LCP1A}	-	-	-	-	24	MHz	CLK_LCP1A
	F_{CLK_LAPP0}	-	-	-	-	24	MHz	CLK_LAPP0
	F_{CLK_LAPP0A}	-	-	-	-	24	MHz	CLK_LAPP0A
	F_{CLK_LAPP1}	-	-	-	-	24	MHz	CLK_LAPP1
	F_{CLK_LAPP1A}	-	-	-	-	24	MHz	CLK_LAPP1A
	F_{CLK_TRC}	-	-	-	-	48	MHz	CLK_TRC
	F_{CLK_HSSPI}	-	-	-	-	24	MHz	CLK_HSSPI
	F_{CLK_SYSC0H}	-	-	-	-	24	MHz	CLK_SYSC0H
	F_{CLK_COMH}	-	-	-	-	24	MHz	CLK_COMH
	F_{CLK_RAM0H}	-	-	-	-	24	MHz	CLK_RAM0H
	F_{CLK_RAM1H}	-	-	-	-	24	MHz	CLK_RAM1H
	F_{CLK_SYSC0P}	-	-	-	-	24	MHz	CLK_SYSC0P
	F_{CLK_COMP}	-	-	-	-	24	MHz	CLK_COMP
	F_{CANFD_CCLK}	-	-	-	-	40	MHz	CANFD_CCLK
Internal Clock Cycle Time	t_{CLK_CPU}	-	-	10.4	-	-	ns	CLK_CPU
	t_{CLK_FLASH}	-	-	20.8	-	-	ns	CLK_FCLK
	t_{CLK_ATB}	-	-	20.8	-	-	ns	CLK_ATB
	t_{CLK_DBG}	-	-	20.8	-	-	ns	CLK_DBG
	t_{CLK_HPM}	-	-	41.6	-	-	ns	CLK_HPM
	t_{CLK_HPM2}	-	-	83.3	-	-	ns	CLK_HPM2
	t_{CLK_DMA}	-	-	41.6	-	-	ns	CLK_DMA

Parameter	Symbol	Pin Name	Conditions	S6J311xHAC* Value * x:A/9			Unit	Remarks
				Min	Typ	Max		
Internal Clock Cycle Time	t_{CLK_MEMC}	-	-	41.6	-	-	ns	CLK_MEMC
	t_{CLK_EXTBUS}	-	-	41.6	-	-	ns	CLK_EXTBUS
	t_{CLK_SYSC1}	-	-	41.6	-	-	ns	CLK_SYSC1
	$t_{CLK\_HAPP0A0}$	-	-	41.6	-	-	ns	CLK_HAPP0A0
	$t_{CLK\_HAPP0A1}$	-	-	41.6	-	-	ns	CLK_HAPP0A1
	$t_{CLK\_HAPP1B0}$	-	-	41.6	-	-	ns	CLK_HAPP1B0
	$t_{CLK\_HAPP1B1}$	-	-	41.6	-	-	ns	CLK_HAPP1B1
	t_{CLK_LLPBM}	-	-	10.4	-	-	ns	CLK_LLPBM
	t_{CLK_LLPBM2}	-	-	20.8	-	-	ns	CLK_LLPBM2
	t_{CLK_LCP}	-	-	20.8	-	-	ns	CLK_LCP
	t_{CLK_LCP0}	-	-	41.6	-	-	ns	CLK_LCP0
	t_{CLK_LCP0A}	-	-	41.6	-	-	ns	CLK_LCP0A
	t_{CLK_LCP1}	-	-	41.6	-	-	ns	CLK_LCP1
	t_{CLK_LCP1A}	-	-	41.6	-	-	ns	CLK_LCP1A
	t_{CLK_LAPP0}	-	-	41.6	-	-	ns	CLK_LAPP0
	t_{CLK_LAPP0A}	-	-	41.6	-	-	ns	CLK_LAPP0A
	t_{CLK_LAPP1}	-	-	41.6	-	-	ns	CLK_LAPP1
	t_{CLK_LAPP1A}	-	-	41.6	-	-	ns	CLK_LAPP1A
	t_{CLK_TRC}	-	-	20.8	-	-	ns	CLK_TRC
	t_{CLK_HSSPI}	-	-	41.6	-	-	ns	CLK_HSSPI
	t_{CLK_SYSC0H}	-	-	41.6	-	-	ns	CLK_SYSC0H
	t_{CLK_COMH}	-	-	41.6	-	-	ns	CLK_COMH
	t_{CLK_RAM0H}	-	-	41.6	-	-	ns	CLK_RAM0H
	t_{CLK_RAM1H}	-	-	41.6	-	-	ns	CLK_RAM1H
	t_{CLK_SYSC0P}	-	-	41.6	-	-	ns	CLK_SYSC0P
	t_{CLK_COMP}	-	-	41.6	-	-	ns	CLK_COMP
	t_{CANFD_CCLK}	-	-	25.0	-	-	ns	CANFD_CCLK

• Guaranteed operation range

Internal operation clock frequency vs. Power supply voltage

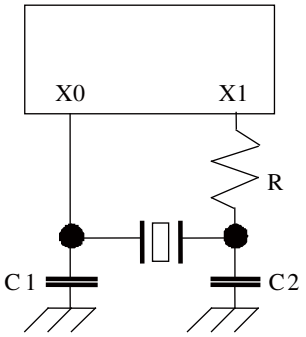


Note: A supply voltage that is equal to or less than the set voltage for low-voltage detection causes a reset.

Relationship between the oscillation clock frequency and internal clock frequency

Oscillation Clock Frequency	Main Clock	PLL Multiplier Setting	PLL Output Division Setting	PLL Clock
4 MHz	4 MHz	144	6	96 MHz
4 MHz	4 MHz	120	6	80 MHz

- Oscillation circuit example

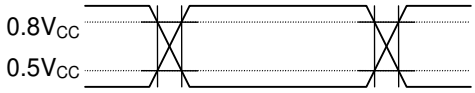


Notes:
· When configuring the oscillator circuit, it is recommended to ask matching evaluation of the circuit to oscillator manufacturers for the design.
· The maximum PLL clock frequency must be 96 MHz.
Output division configuration can be set by the following.
- PLLDIVM bit in SYSC0_RUNPLL0CNTR register
- PLLDIVM bit in SYSC0_PSSPLL0CNTR register
- SSCGDIVM bit in SYSC0_RUNSSCG0CNTR0 register
- SSCGDIVM bit in SYSC0_PSSSSCG0CNTR0 register
(e.g. If PLLout is 576 MHz, these settings must be configured as "multiply by 6" and over multiplication setting)

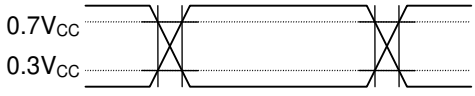
AC characteristics are specified by the following measurement reference voltage values.

- Input signal waveform

Hysteresis input pin (Automotive)



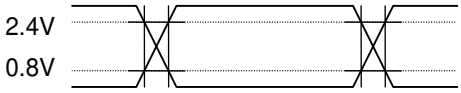
Hysteresis input pin (CMOS Schmitt)



Hysteresis input pin (TTL)

- Output signal waveform

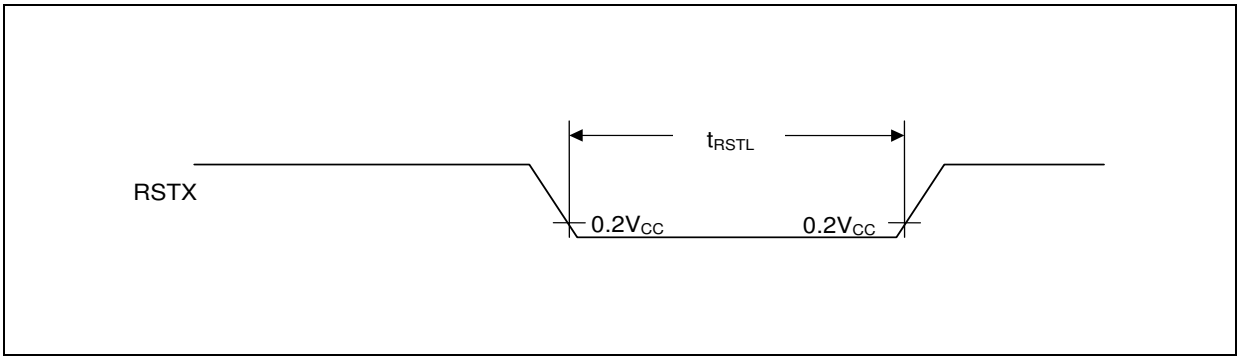
Output pin



10.4.3 Reset Input

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	RSTX	-	10	-	µs	
Width for reset input removal				1	-	µs	



10.4.4 Power-on Conditions

(T_A: Recommended operating conditions, V_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	-	VCC	-	2.15	2.35	2.55	V	
Level release voltage	-	VCC	-	2.25	2.45	2.65	V	
Level detection hysteresis width	-	VCC	-	-	100	-	mV	
Level detection time	-	-	-	-	-	540	µs	*1
Power off time	t_{OFF}	VCC	-	1	-	-	ms	*2
Power ramp rate	dV/dt	VCC	VCC: 0.2 V to 2.55 V	–	–	6	mV/µs	*3
Maximum ramp rate guaranteed to not generate power-on reset	|dV/dt|	VCC	VCC: Between 2.6 V and 4.5 V	–	–	50	mV/µs	*4

*1: If a power fluctuation precedes the low-voltage detection time, the detection may occur or be canceled after the supply voltage passes the detection voltage range.

*2: If VCC is held below 0.2 V for a minimum period of tOFF, power-on reset will occur. If tOFF is not satisfied, power-on reset will still occur if the power ramp rate is kept below 6 mV/µs.

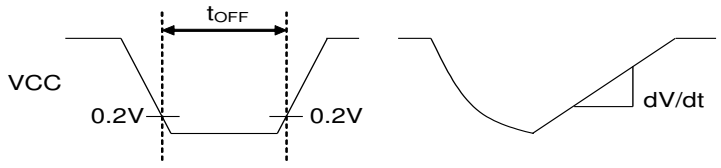
*3: This is the power ramp rate with which power-on reset will always occur regardless of power-off time, as mentioned in *2.

*4: When VCC is within 2.6 V - 4.5 V, and VCC fluctuation is below 50 mV/us, the power-on reset is suppressed. Between 4.5 V - 5.5 V, the power-on reset does not occur with any VCC fluctuation.

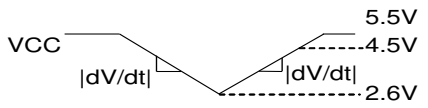
Note:

When neither *2 nor *3 can be satisfied, assert external reset (RSTX) at power-up and at any brownout event.

・Power off time, Power ramp rate at Power-on



・Maximum ramp rate guaranteed to not generate power-on reset



10.4.5 Multi-function Serial

10.4.5.1 CSIO Timing (SMR:MD[2:0] = 010_B)

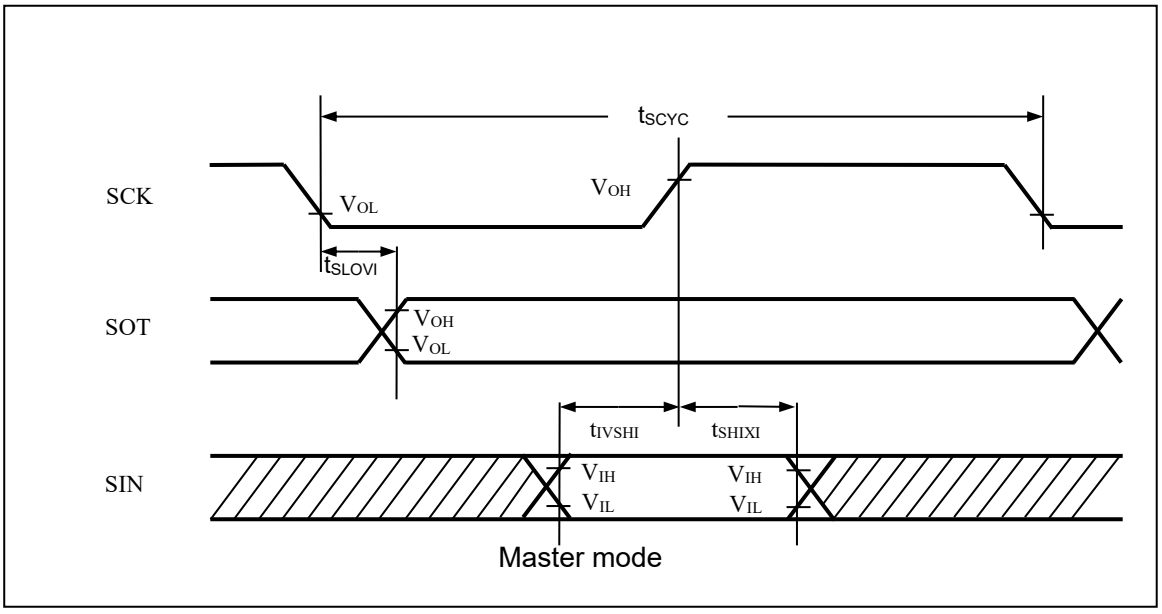
(5-1-1) Normal Synchronous Transfer (SCR:SPI = 0) and Serial Clock Output Signal Detect Level "H" (SMR:SCINV = 0)

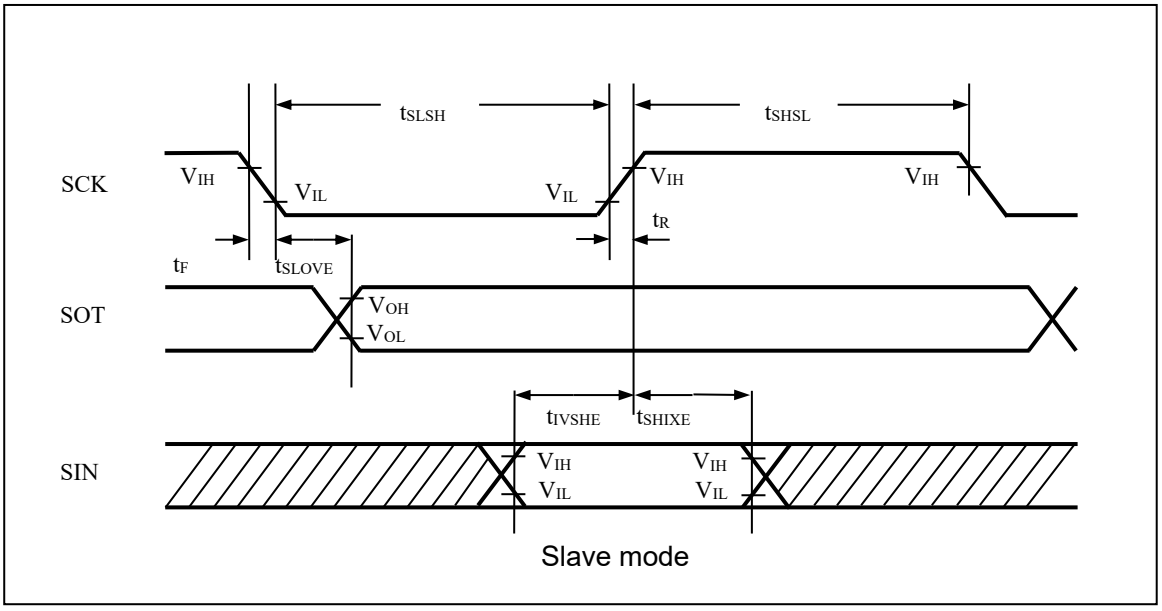
(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Master mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	$4t_{CLK\_LCP0A}$	-	ns	
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		-30	+30	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		30	-	ns	
SCK ↑→ Valid SIN hold time	t_{SHIXI}			0	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK3	Slave mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CLK_LCP0A} +10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CLK\_LCP0A}$ -10	-	ns	
SCK ↓→ SOT delay time	t_{SLOVE}	SCK0 to SCK3, SOT0 to SOT3		-	45	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		10	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK3		-	5	ns	
SCK rise time	t_R	SCK0 to SCK3		-	5	ns	

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.


tSCYC
SCK
VOL
VOH
tSLOVI
SOT
VOH
VOL
tIVSHI
tSHIXI
SIN
VIH
VIL
VIH
VIL
Master mode


tSLSH
tSHSL
SCK
VIH
VIL
VIL
VIH
VIH
tR
tF
tSLOVE
SOT
VOH
VOL
tIVSHE
tSHIXE
SIN
VIH
VIL
VIH
VIL
Slave mode

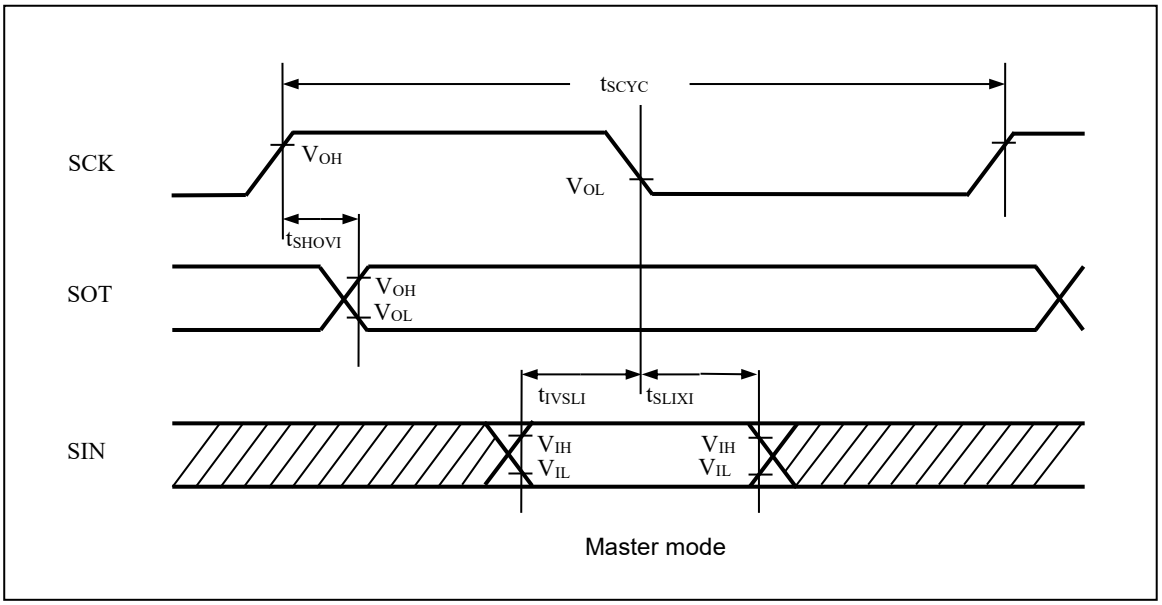
(5-1-2) Normal Synchronous Transfer (SCR:SPI = 0) and Serial Clock Output Signal Detect Level "L" (SMR:SCINV = 1)

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

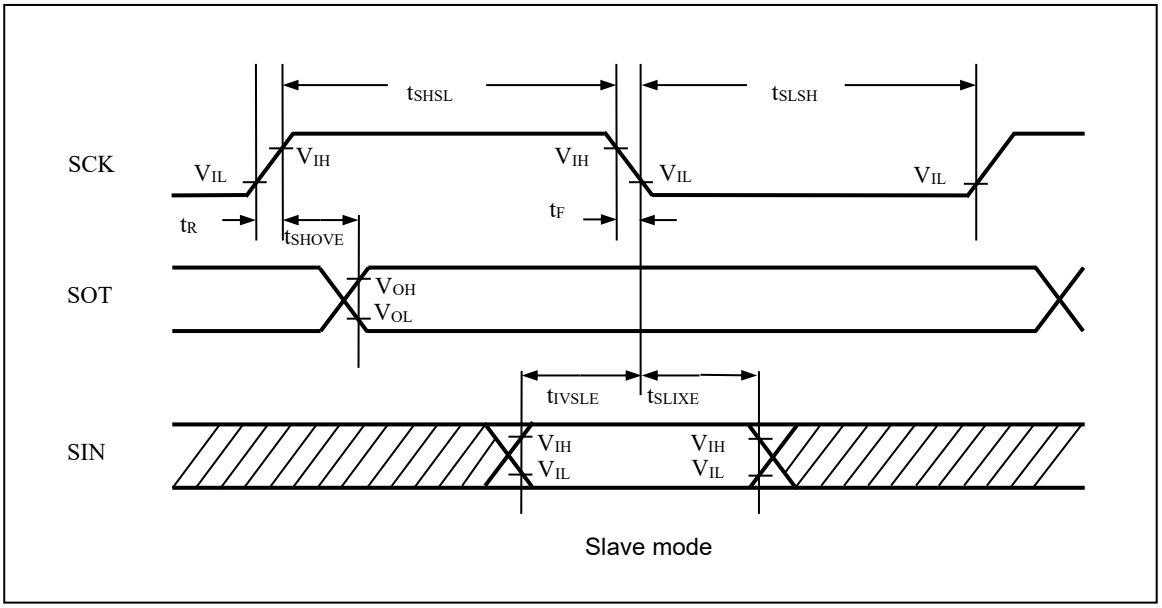
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Master mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	$4t_{CLK\_LCP0A}$	-	ns	
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		-30	+30	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		30	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}			0	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK3	Slave mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CLK_LCP0A} +10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CLK\_LCP0A}$ -10	-	ns	
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0 to SCK3, SOT0 to SOT3		-	45	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLE}	SCK0 to SCK3, SIN0 to SIN3		10	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK3		-	5	ns	
SCK rise time	t_R	SCK0 to SCK3		-	5	ns	

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



Master mode



Slave mode

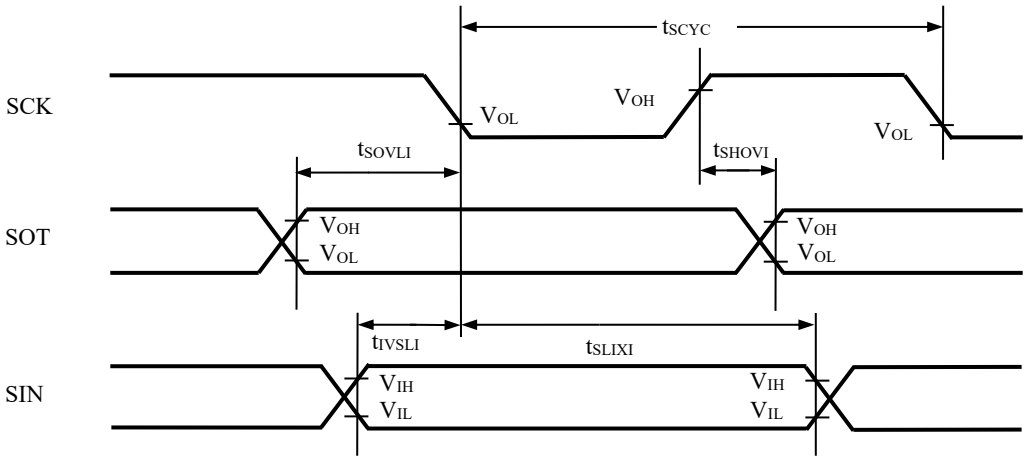
(5-1-3) SPI Supported (SCR:SPI = 1), and Serial Clock Output Signal Detect Level "H" (SMR:SCINV = 0)

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

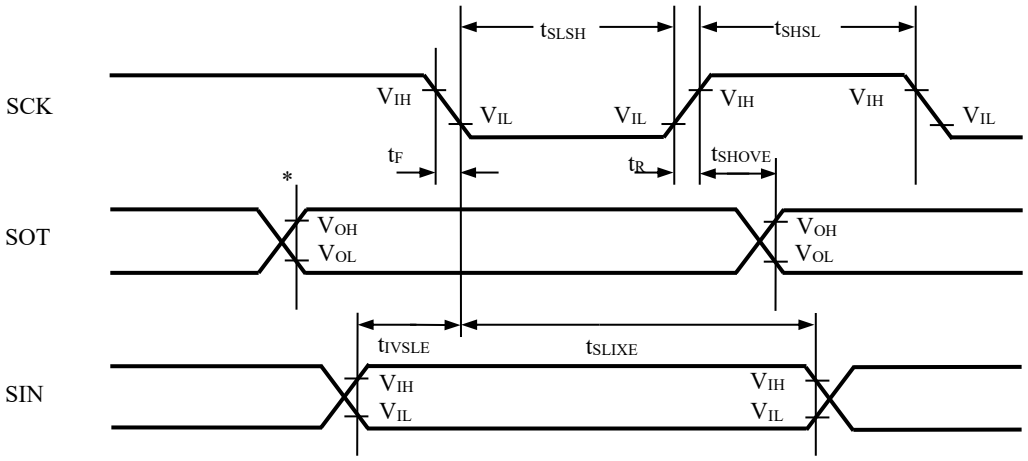
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Master mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	$4t_{CLK\_LCP0A}$	-	ns	
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		-30	+30	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		30	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}			0	-	ns	
SOT → SCK ↓ delay time	t_{SOVLI}	SCK0 to SCK3, SOT0 to SOT3		$2t_{CLK\_LCP0A}$ -30	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK3	Slave mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CLK_LCP0A} +10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CLK\_LCP0A}$ -10	-	ns	
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0 to SCK3, SOT0 to SOT3		-	45	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLE}	SCK0 to SCK3, SIN0 to SIN3		10	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK3		-	5	ns	
SCK rise time	t_R	SCK0 to SCK3		-	5	ns	

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



Master mode



* Changes when writing to the TDR register

Slave mode

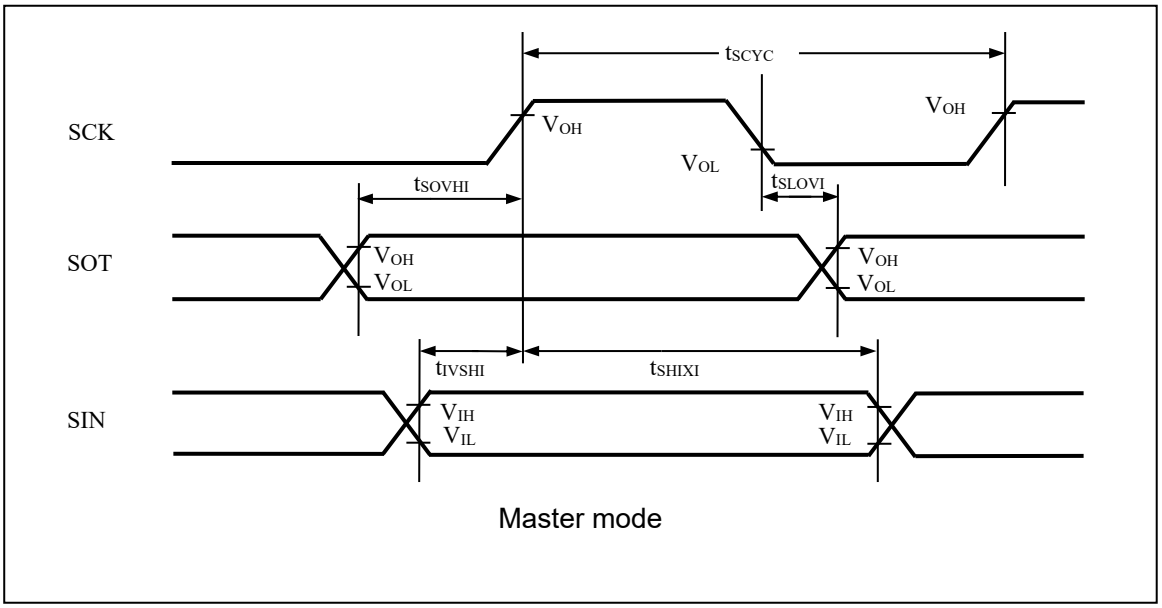
(5-1-4) SPI Supported (SCR:SPI = 1), and Serial Clock Output Signal Detect Level "L" (SMR:SCINV = 1)

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

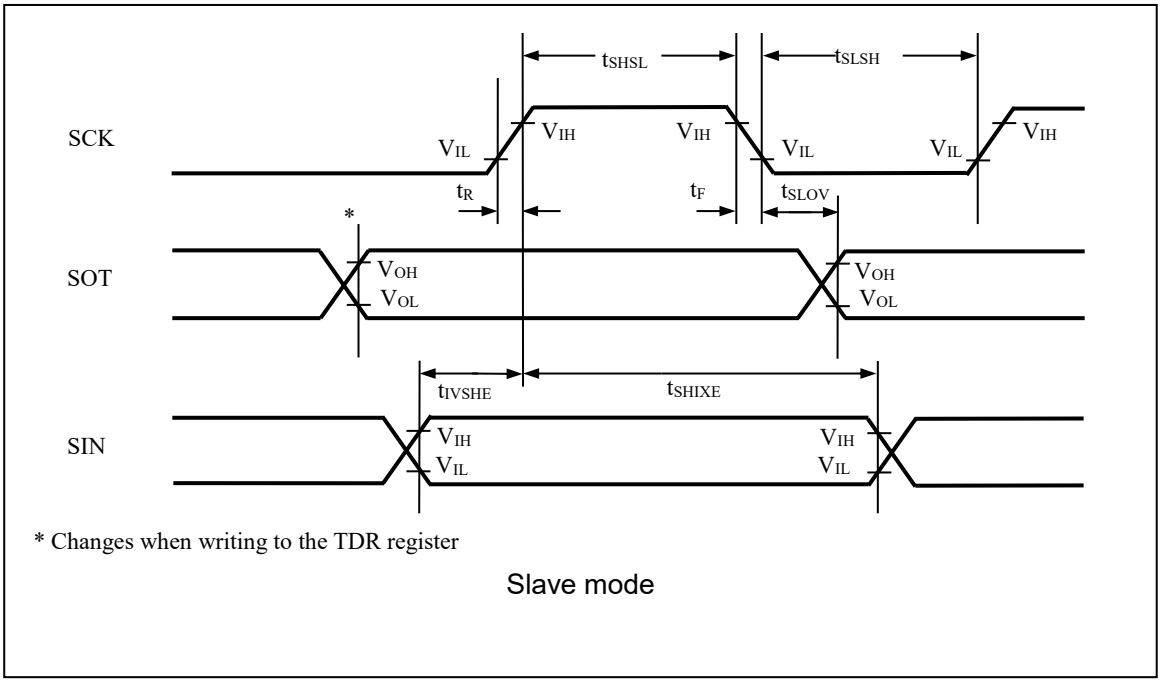
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Master mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	$4t_{CLK\_LCP0A}$	-	ns	
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		-30	+30	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		30	-	ns	
SCK ↑→ Valid SIN hold time	t_{SHIXI}			0	-	ns	
SOT → SCK ↑ delay time	t_{SOVHI}	SCK0 to SCK3, SOT0 to SOT3		$2t_{CLK\_LCP0A}$ -30	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK3	Slave mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CLK_LCP0A} +10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CLK\_LCP0A}$ -10	-	ns	
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK3, SOT0 to SOT3		-	45	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		10	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK3		-	5	ns	
SCK rise time	t_R	SCK0 to SCK3		-	5	ns	

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



Master mode



* Changes when writing to the TDR register

Slave mode

(5-1-5) Serial Chip Select Used (SCSCR:CSEN = 1)

■Mark level "H" of serial clock output (SMR, SCSFR:SCINV = 0)

■Inactive level "H" of serial chip select (SCSCR, SCSFR:CSLVL = 1)

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↓ → SCK ↓ setup time	t_{CSSI}	SCK0 to SCK3, SCS0x to SCS3x	Master mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CSSU}*1-50	-	ns	
SCK ↑ → SCS ↑ hold time	t_{CSHI}			t_{CSHD}*2+0	-	ns	
SCS deselect time	t_{CSDI}	SCS0x to SCS3x		t_{CSDS}*3-50 +5t_{CLK_LCP0A}	-	ns	
SCS ↓ → SCK ↓ setup time	t_{CSSE}	SCK0 to SCK3, SCS0x to SCS3x	Slave mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	3t_{CLK_LCP0A} +30	-	ns	
SCK ↑ → SCS ↑ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}	SCS0x to SCS3x		3t_{CLK_LCP0A} +30	-	ns	
SCS ↓ → SOT delay time	t_{DSE}	SCS0x to SCS3x, SOT0 to SOT3		-	50	ns	
SCS ↑ → SOT delay time	t_{DEE}			0	-	ns	
SCK ↓ → SCS ↓ clock switching time	t_{SCC}	SCK0 to SCK3, SCS0x to SCS3x	Master mode round operation (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	3t_{CLK_LCP0A} +0	3t_{CLK_LCP0A} +50	ns	

*1: t_{CSSU} = SCSTR:CSSU[7:0] x serial chip select timing operating clock

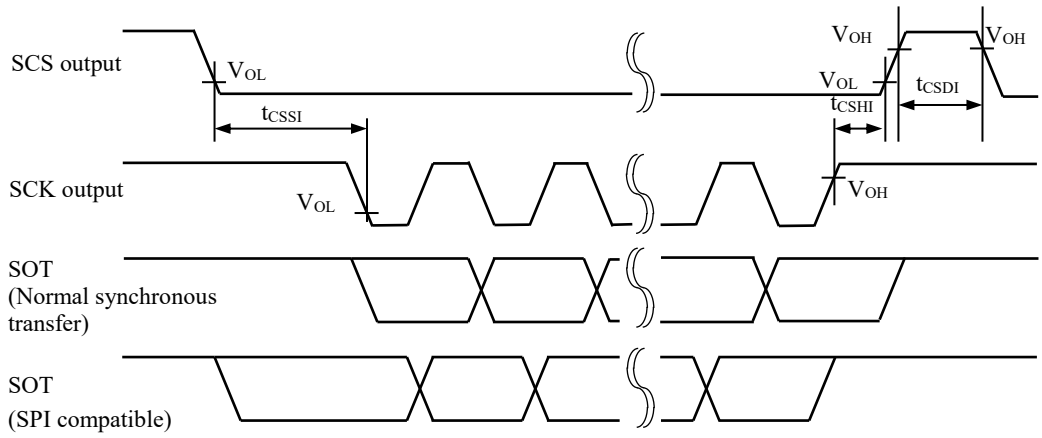
*2: t_{CSHD} = SCSTR:CSHD[7:0] x serial chip select timing operating clock

*3: t_{CSDS} = SCSTR:CSDS[15:0] x serial chip select timing operating clock

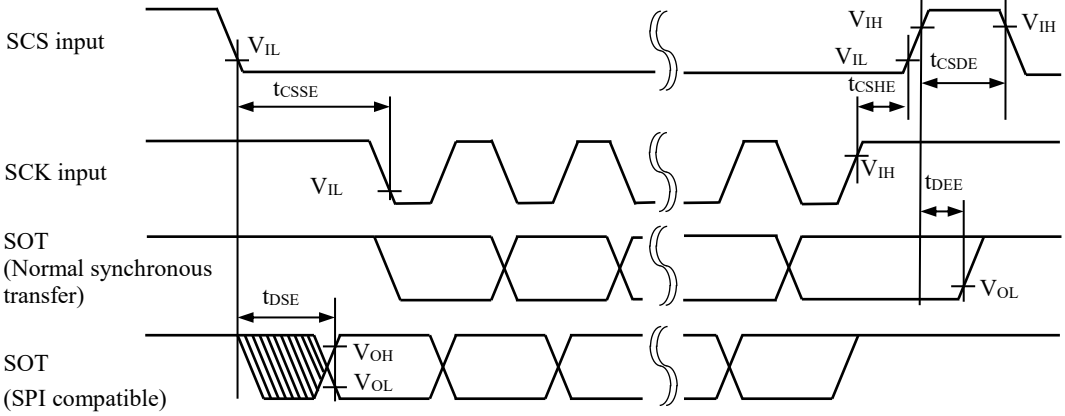
For details on *1, *2, and *3 above, see the hardware manual.

Notes:

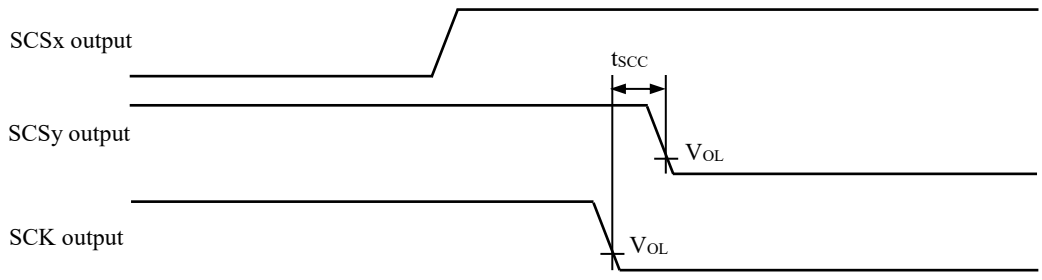
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



Master mode



Slave mode



Clock switching example by master mode round operation
(x,y=0,1,2 : x and y are different value)

(5-1-6) Serial Chip Select Used (SCSCR:CSEN = 1)

■Serial clock output signal detect level "L" (SMR, SCSFR:SCINV = 1)

■Serial chip select inactive level "H" (SCSCR, SCSFR:CSLVL = 1)

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↓→ SCK ↑ setup time	t_{CSSI}	SCK0 to SCK3, SCS0x to SCS3x	Master mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CSSU}*1-50	-	ns	
SCK ↓→ SCS ↑ hold time	t_{CSHI}			t_{CSHD}*2+0	-	ns	
SCS deselect time	t_{CSDI}	SCS0x to SCS3x		t_{CSDS}*3-50+ 5 t_{CLK_LCP0A}	-	ns	
SCS ↓ → SCK ↑ setup time	t_{CSSE}	SCK0 to SCK3, SCS0x to SCS3x	Slave mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	3t_{CLK_LCP0A} +30	-	ns	
SCK ↓ → SCS ↑ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}	SCS0x to SCS3x		3t_{CLK_LCP0A} +30	-	ns	
SCS ↓ → SOT delay time	t_{DSE}	SCS0x to SCS3x, SOT0 to SOT3		-	50	ns	
SCS ↑ → SOT delay time	t_{DEE}			0	-	ns	
SCK ↑ → SCS ↓ clock switching time	t_{SCC}	SCK0 to SCK3, SCS0x to SCS3x	Master mode round operation (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	3t_{CLK_LCP0A} +0	3t_{CLK_LCP0A} +50	ns	

*1: t_{CSSU} = SCSTR:CSSU[7:0] x serial chip select timing operating clock

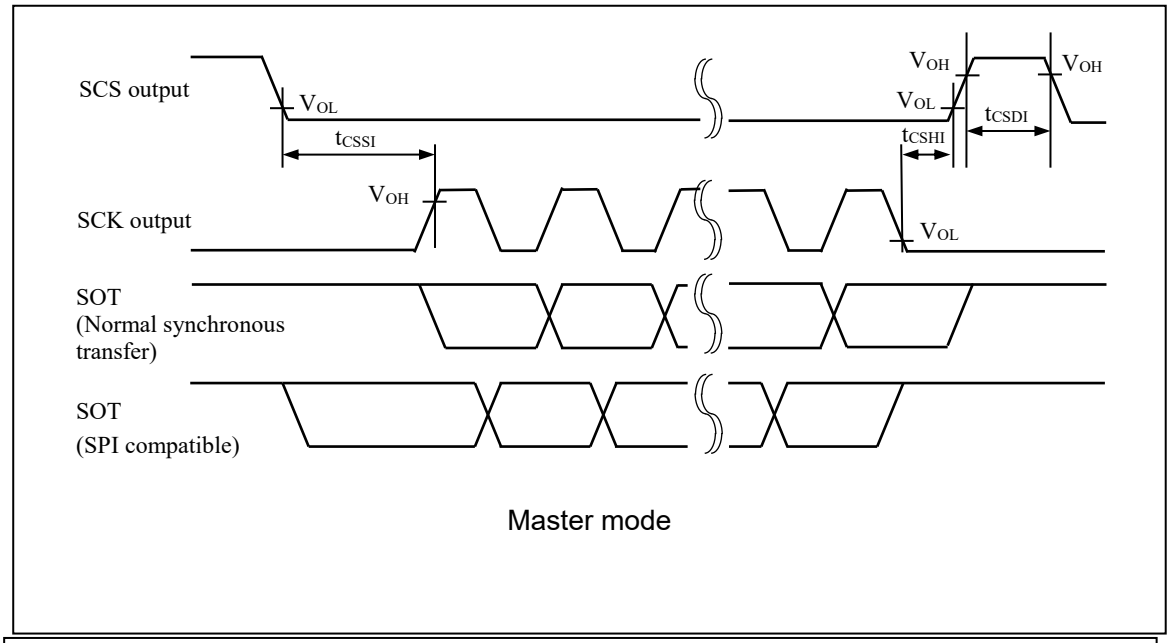
*2: t_{CSHD} = SCSTR:CSHD[7:0] x serial chip select timing operating clock

*3: t_{CSDS} = SCSTR:CSDS[15:0] x serial chip select timing operating clock

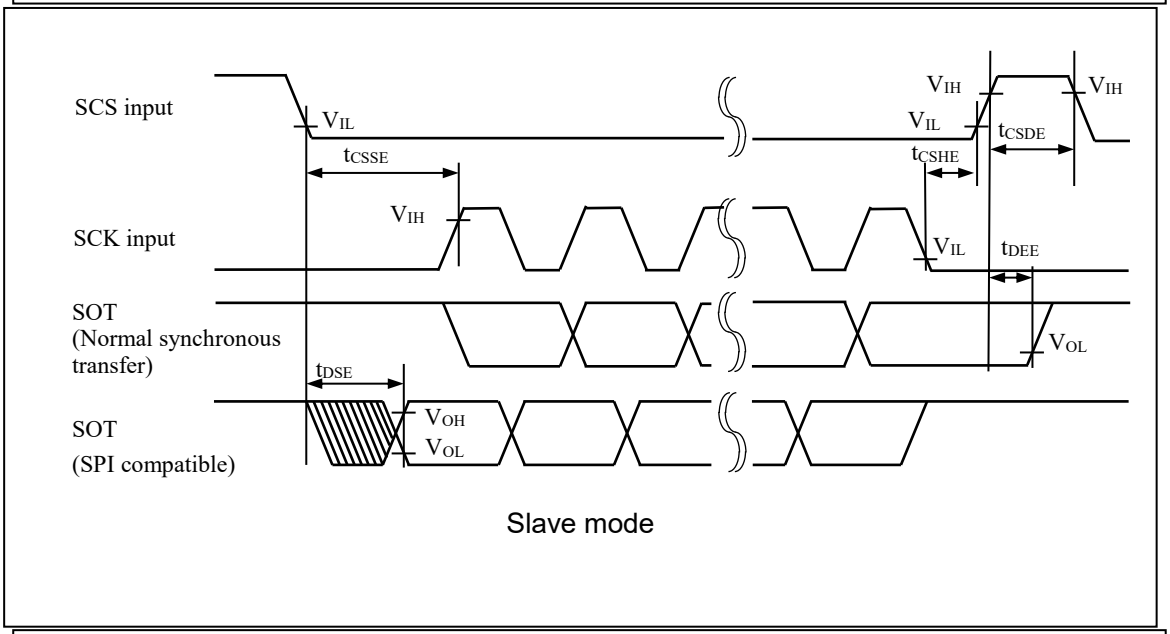
For details on *1, *2, and *3 above, see the hardware manual.

Notes:

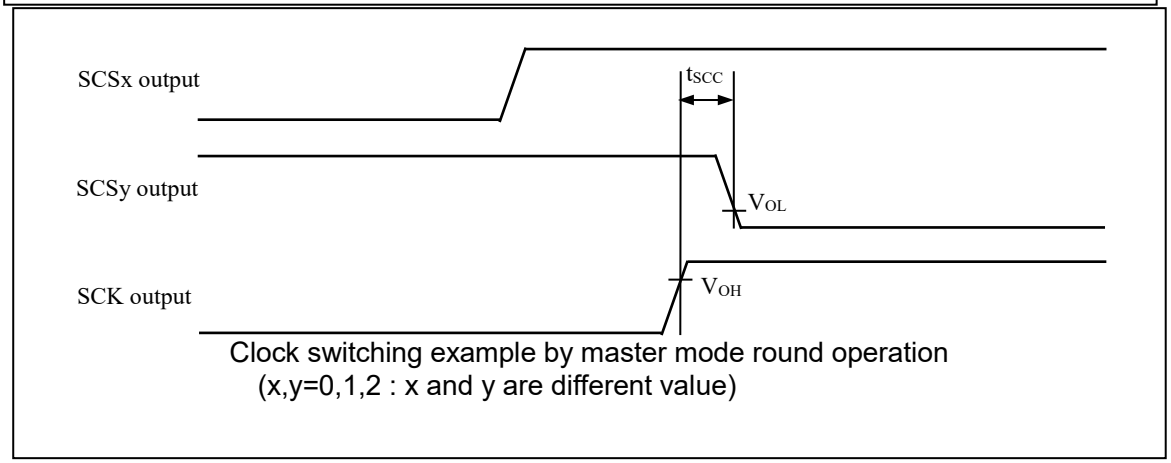
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



Master mode



Slave mode



Clock switching example by master mode round operation
(x,y=0,1,2 : x and y are different value)

(5-1-7) Serial Chip Select Used (SCSCR:CSEN = 1)

■Serial clock output signal detect level "H" (SMR, SCSFR:SCINV = 0)

■Serial Chip select inactive level "L" (SCSCR, SCSFR:CSLVL = 0

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ → SCK ↓ setup time	t_{CSSI}	SCK0 to SCK3, SCS0x to SCS3x	Master mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CSSU} *1-50	-	ns	
SCK ↑ → SCS ↓ hold time	t_{CSHI}			t_{CSHD} *2+0	-	ns	
SCS deselect time	t_{CSDI}	SCS0x to SCS3x		t_{CSDS} *3-50+ 5 t_{CLK_LCP0A}	-	ns	
SCS ↑ → SCK ↓ setup time	t_{CSSE}	SCK0 to SCK3, SCS0x to SCS3x	Slave mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	$3t_{CLK\_LCP0A}$ +30	-	ns	
SCK ↑ → SCS ↓ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}	SCS0x to SCS3x		$3t_{CLK\_LCP0A}$ +30	-	ns	
SCS ↑ → SOT delay time	t_{DSE}	SCS0x to SCS3x, SOT0 to SOT3		-	50	ns	
SCS ↓ → SOT delay time	t_{DEE}			0	-	ns	
SCK ↓ → SCS ↑ clock switching time	t_{SCC}	SCK0 to SCK3, SCS0x to SCS3x	Master mode round operation (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	$3t_{CLK\_LCP0A}$ +0	$3t_{CLK\_LCP0A}$ +50	ns	

*1: t_{CSSU} = SCSTR:CSSU[7:0] x serial chip select timing operating clock

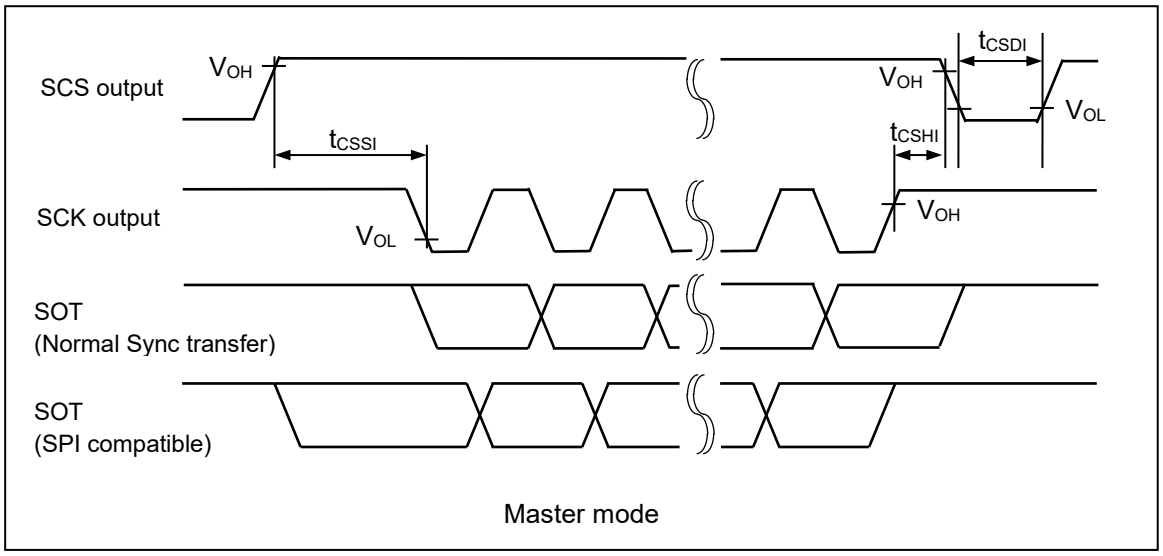
*2: t_{CSHD} = SCSTR:CSHD[7:0] x serial chip select timing operating clock

*3: t_{CSDS} = SCSTR:CSDS[15:0] x serial chip select timing operating clock

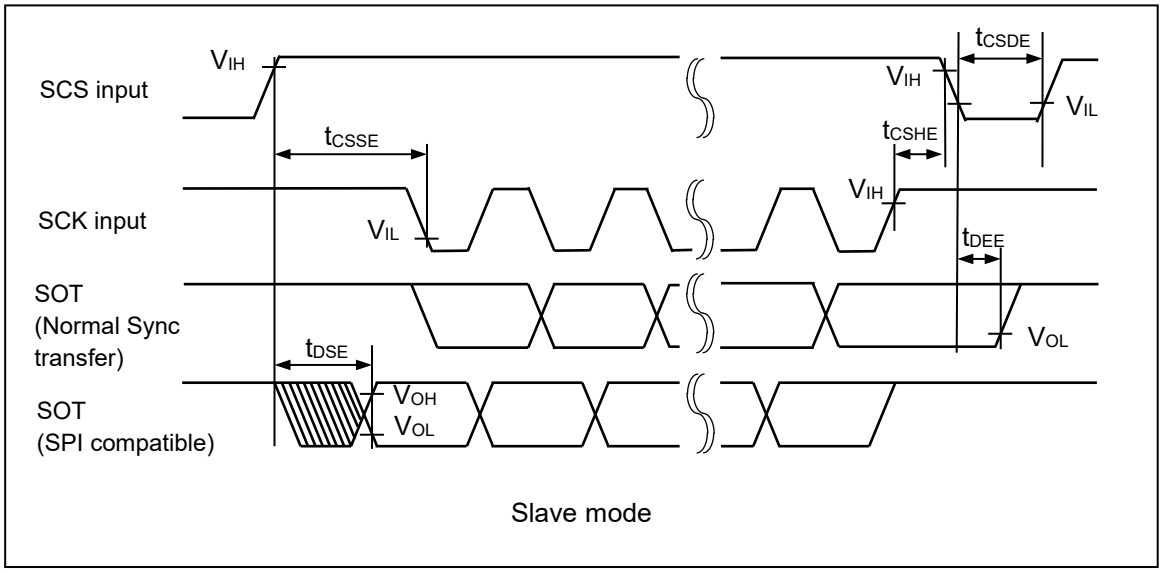
For details on *1, *2, and *3 above, see the hardware manual.

Notes:

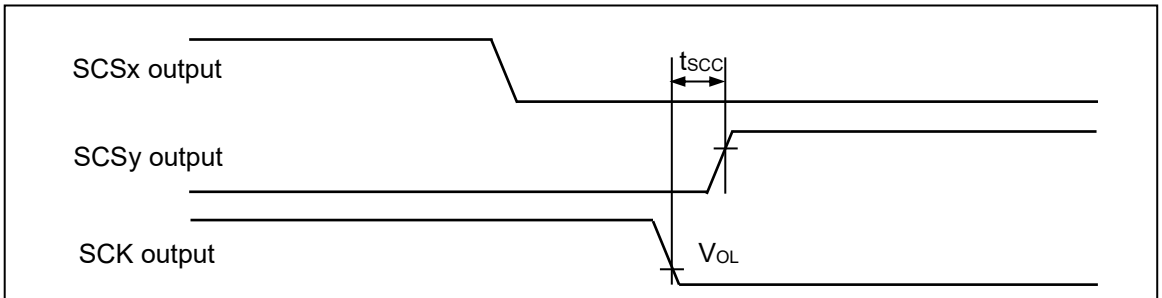
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual



Master mode



Slave mode



Clock switching example by master mode round operation
(x,y=0,1,2 : x and y are different value.)

(5-1-8) Serial Chip Select Used (SCSCR:CSEN = 1)

■Serial clock output signal detect level "L" (SMR, SCSFR:SCINV = 1)

■Serial Chip select inactive level "L" (SCSCR, SCSFR:CSLVL = 0)

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ → SCK ↑ setup time	t_{CSSI}	SCK0 to SCK3, SCS0x to SCS3x	Master mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CSSU} *1-50	-	ns	
SCK ↓ → SCS ↓ hold time	t_{CSHI}			t_{CSHD} *2+0	-	ns	
SCS deselect time	t_{CSDI}	SCS0x to SCS3x		t_{CSDS} *3-50 + 5 t_{CLK_LCP0A}	-	ns	
SCS ↑ → SCK ↑ setup time	t_{CSSE}	SCK0 to SCK3, SCS0x to SCS3x	Slave mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	3t_{CLK_LCP0A} + 30	-	ns	
SCK ↓ → SCS ↓ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}	SCS0x to SCS3x		3t_{CLK_LCP0A} + 30	-	ns	
SCS ↑ → SOT delay time	t_{DSE}	SCS0x to SCS3x, SOT0 to SOT3		-	50	ns	
SCS ↓ → SOT delay time	t_{DEE}			0	-	ns	
SCK ↑ → SCS ↑ clock switching time	t_{SCC}	SCK0 to SCK3, SCS0x to SCS3x	Master mode round operation (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	3t_{CLK_LCP0A} + 0	3t_{CLK_LCP0A} + 50	ns	

*1: t_{CSSU} = SCSTR:CSSU[7:0] x serial chip select timing operating clock

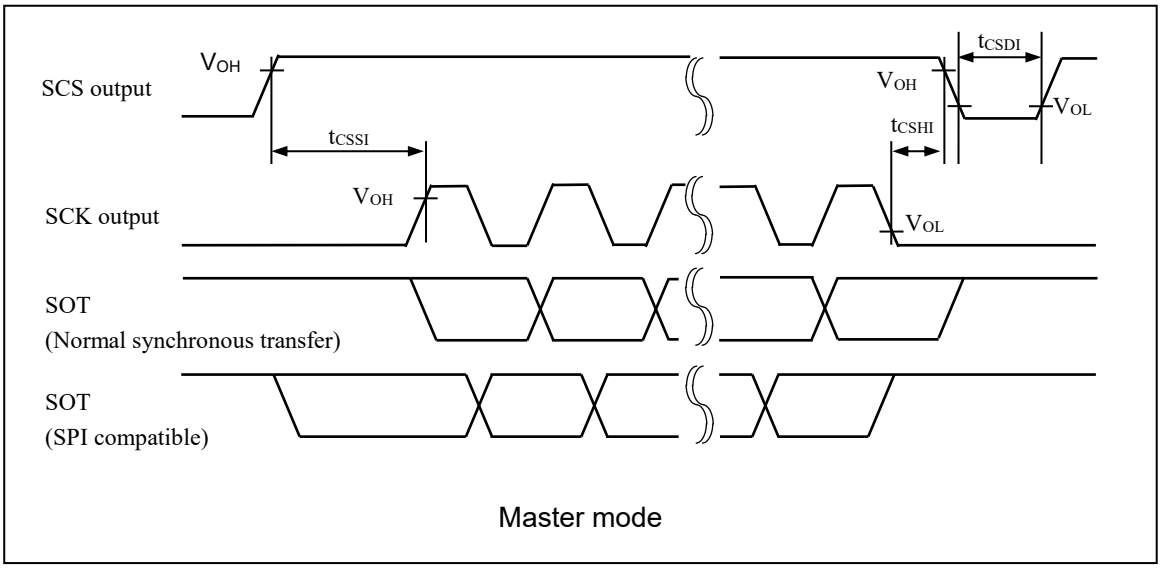
*2: t_{CSHD} = SCSTR:CSHD[7:0] x serial chip select timing operating clock

*3: t_{CSDS} = SCSTR:CSDS[15:0] x serial chip select timing operating clock

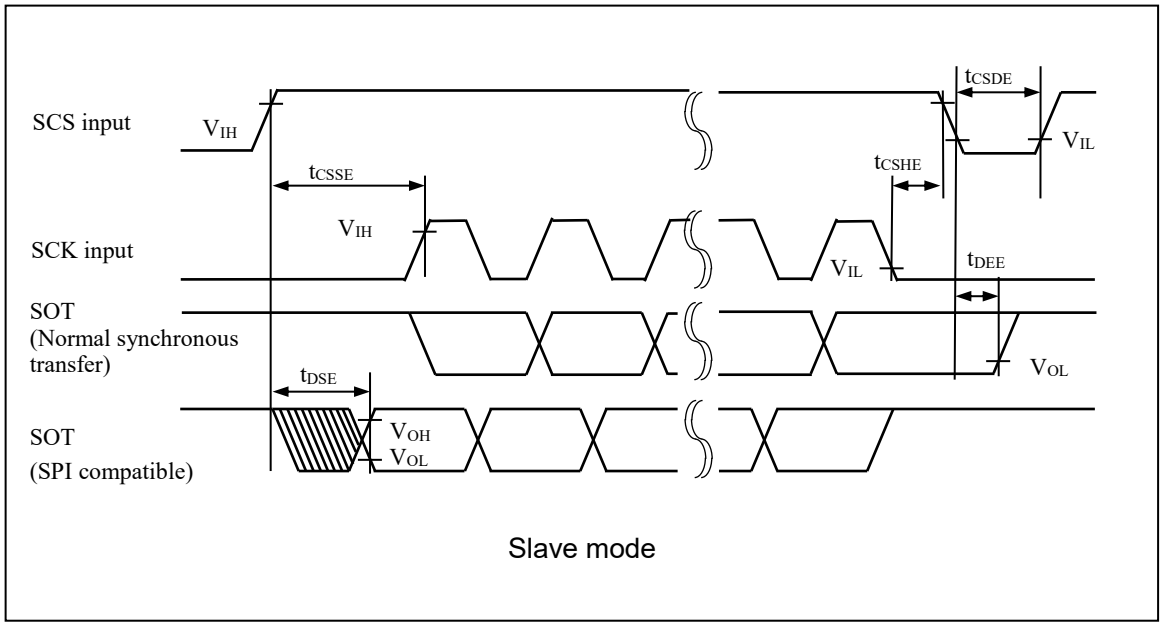
For details on *1, *2, and *3 above, see the hardware manual.

Notes:

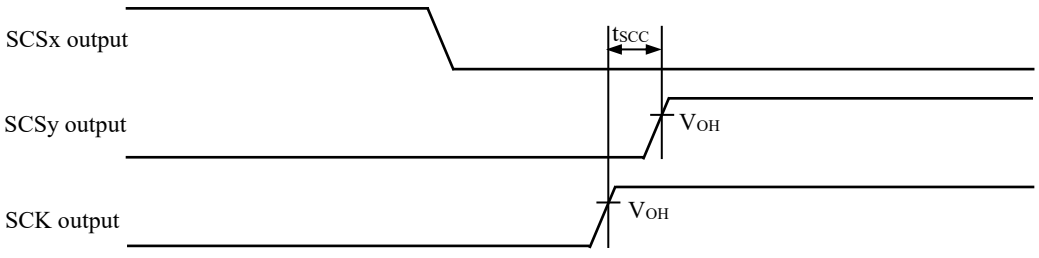
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



Master mode



Slave mode



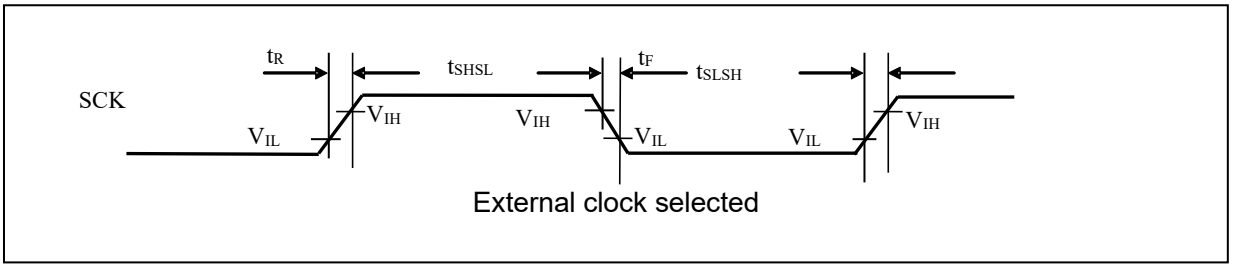
Clock switching example by master mode round operation
(x,y=0,1,2 : x and y are different value)

10.4.5.2 UART (Async Serial Interface) Timing
(SMR:MD[2:0] = 000B, 001B)

(5-2-1) External clock selected (BGR:EXT = 1)

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK3	(C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CLK_LCP0A} +10	-	ns	
Serial clock "H" pulse width	t_{SHSL}			t_{CLK_LCP0A} +10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	



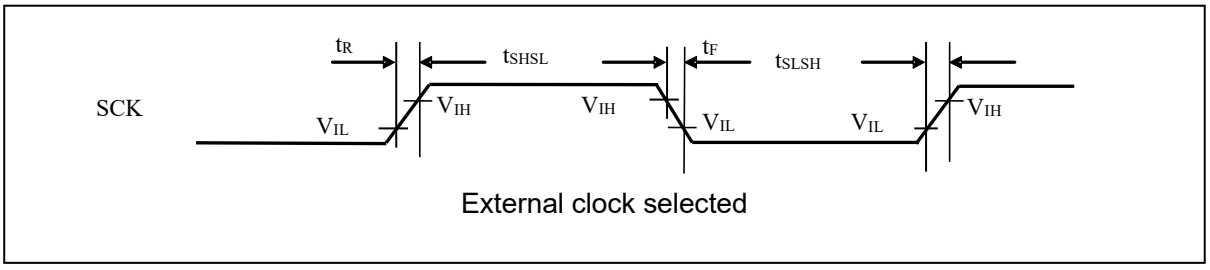
External clock selected

10.4.5.3 LIN Interface (v2.1) (LIN Communication Control Interface (v2.1)) Timing (SMR:MD[2:0] = 011_B)

(5-3-1) External Clock Selected (BGR:EXT = 1)

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK3	(C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CLK_LCP0A}+10	-	ns	
Serial clock "H" pulse width	t_{SHSL}			t_{CLK_LCP0A}+10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	



External clock selected

10.4.5.4 I²C timing (SMR:MD[2:0] = 100B)

(T_A: Recommended operating conditions, Vcc = 5.0 V +5%/-10%, Vss = AVss = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Standard Mode		Unit	Remarks
				Min	Max		
SCL clock frequency	f_{SCL}	SCL0 to SCL3	C_L = 50 pF, R = (Vp/I_{OL})*1	0	100	kHz	
Repeat "start" condition hold time SDA ↓ → SCL ↓	t_{HDSTA}	SDA0 to SDA3 SCL0 to SCL3		4.0	-	µs	
Period of "L" for SCL clock	t_{LOW}	SCL0 to SCL3		4.7	-	µs	
Period of "H" for SCL clock	t_{HIGH}			4.0	-	µs	
Repeat "start" condition setup time SCL ↑ → SDA ↓	t_{SUSTA}	SDA0 to SDA3 SCL0 to SCL3		4.7	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}			0	3.45*2	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}			250	-	ns	
"Stop" condition setup time SCL ↑ → SDA ↑	t_{SUSTO}			4.0	-	µs	
Bus-free time between "stop" condition and "start" condition	t_{BUF}	-		4.7	-	µs	
Noise filter	t_{SP}	-		t_{NFT}*3	-	ns	

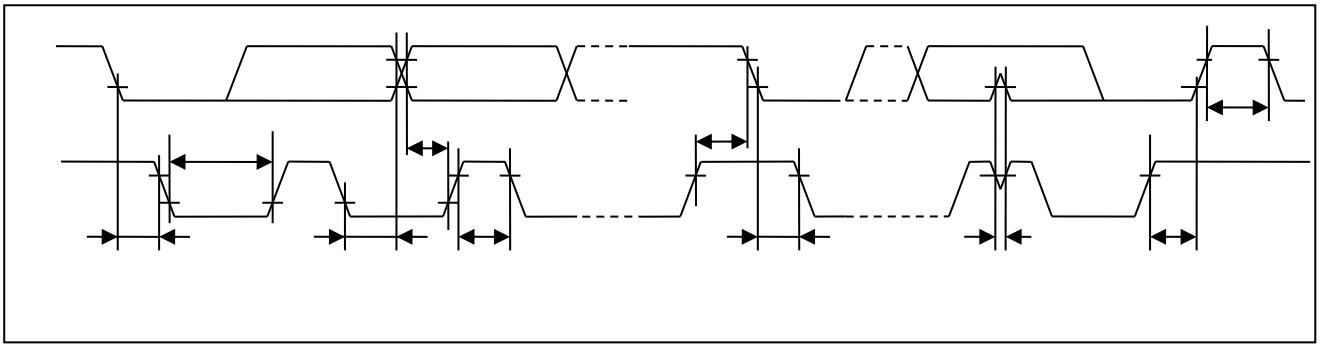
*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively Vp shows that the power-supply voltage of the pull-up resistor and IOL shows the VOL guarantee current.

*2: The maximum tHDDAT only has to be met if the device does not extend the "L" width (tLOW) of the SCL signal.

*3: tNFT = (NFCR:NFT[4:0]+1) x 2 x tCLK_LCP0A

Notes:

- In this device, Standard mode (Max. 100 kbps) is supported only.
- This model does not support high-speed mode. (Max. 400 kbps).
- This model does not support Min. I_{OL} = 3 mA with V_{OL} = 0.4 V.

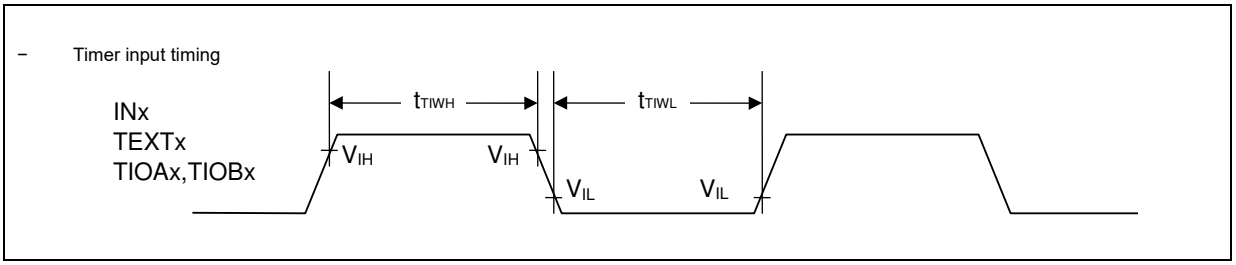


10.5 Timer Input Timing

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TWH}, t_{TWL}	IN0 to IN11	-	$4t_{CLK\_LCP0A}$	-	ns	$4t_{CLK\_LCP0A} \geq 100$ ns
				100			$4t_{CLK\_LCP0A} < 100$ ns
		TEXT0 to 5	-	$4t_{CLK\_LCP0A}$	-	ns	$4t_{CLK\_LCP0A} \geq 100$ ns
				100			$4t_{CLK\_LCP0A} < 100$ ns
		TIOA0 to TIOA29 TIOB0 to TIOB7	-	$4t_{CLK\_LCP0A}$	-	ns	$4t_{CLK\_LCP0A} \geq 100$ ns
				100			$4t_{CLK\_LCP0A} < 100$ ns

- Timer input timing

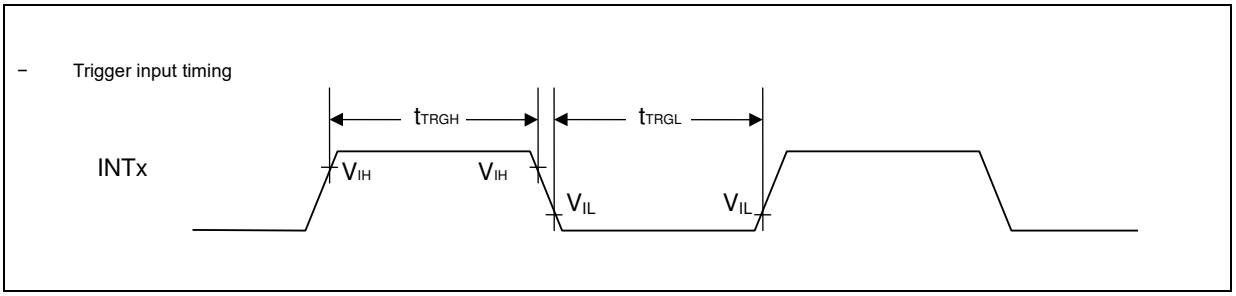


10.6 Trigger Input Timing

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT15	-	100	-	ns	
		INT0 to INT15	-	1	-	µs	Stop mode

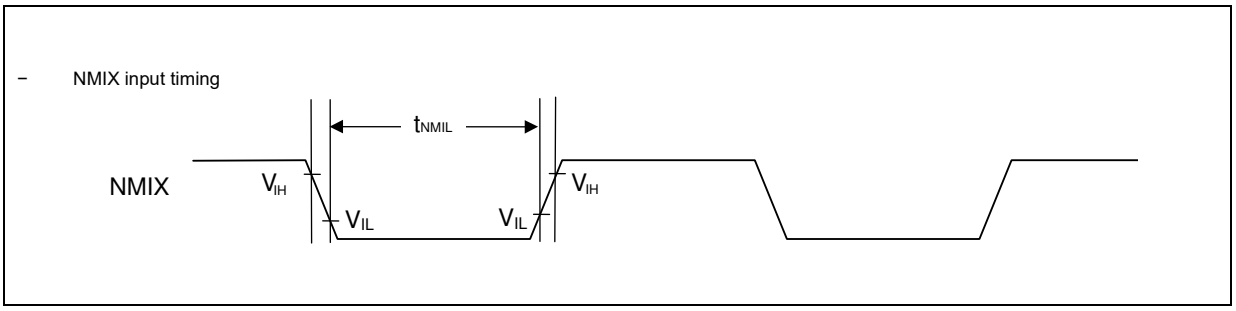
- Trigger input timing



10.7 NMI Input Timing

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{NMIL}	NMIX	-	300	-	ns	



10.8 Low-Voltage Detection (External Low-Voltage Detection)

(T_A: Recommended operating conditions, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{DP5}	VCC	-	3.5	-	5.25	V	
Detection voltage	V_{DL0}	VCC	*1 *3	3.6	3.8	4.0	V	When power-supply voltage falls and detection level is set initially
	V_{DL1}	VCC	*1 *4	3.8	4.0	4.2	V	
	V_{DL2}	VCC	*1 *5	4	4.2	4.4	V	
Hysteresis width	V_{HYS}	VCC	-	-	100	-	mV	When power-supply voltage rises
Low-voltage detection time	T_d	-	-	-	-	30	µs	
Power supply voltage regulation	-	VCC	-	-2	-	2	V/ms	*2

*1: If the fluctuation of the power supply has exceeded the detection voltage range within the time less than the low-voltage detection time (T_d), there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: Please suppress the change of the power supply within the range of the power-supply voltage regulation to do low-voltage detection by detecting voltage (V_{DL})

*3: SYSC0_RUNLVDCFGR.LVDH1V = 0100_B or SYSC0_PSSLVDCFGR.LVDH1V = 0100_B

*4: SYSC0_RUNLVDCFGR.LVDH1V = 0101_B or SYSC0_PSSLVDCFGR.LVDH1V = 0101_B

*5: SYSC0_RUNLVDCFGR.LVDH1V = 0110_B or SYSC0_PSSLVDCFGR.LVDH1V = 0110_B

10.9 Low-Voltage Detection (RAM Retention Low-Voltage Detection)

(T_A: Recommended operating conditions, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{RDP5}	-	-	0.6	-	1.4	V	
Detection voltage*	V_{RDL}	-	*1	0.9	0.95	1.0	V	When power-supply voltage falls
Hysteresis width	V_{RHYS}	-	-	-	75	-	mV	When power-supply voltage rises
Low-voltage detection time	T_{Rd}	-	-	-	-	30	µs	

*: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage.

*1: If the fluctuation of the power supply has exceeded the detection voltage range within the time less than the low-voltage detection time (T_{Rd}), there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

10.10 Low-Voltage Detection (1.2 V Power Supply Low-Voltage Detection)

(T_A: Recommended operating conditions, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks	Guaranteed MCU operation range
				Min	Typ	Max			
Power supply voltage range	V_{RDP5}	-	-	0.6	-	1.4	V		No
Detection voltage*	V_{RDL0}	-	*1 *2 *4	0.92	0.97	1.02	V	When power-supply voltage falls	
	V_{RDL1}	-	*1 *3 *4	1.02	1.07	1.12	V		
Hysteresis width	V_{RHYS}	-	-	-	75	-	mV	When power-supply voltage rises	
Low-voltage detection time	T_{Rd}	-	-	-	-	30	µs		

*: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.

*1: If the fluctuation of the power supply has exceeded the detection voltage range within the time less than the low-voltage detection time (T_{Rd}), there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: SYSC0_RUNLVDCFGR.LVDL1V = 10_B or SYSC0_PSSLVDCFGR.LVDL1V = 10_B

*3: SYSC0_RUNLVDCFGR.LVDL1V = 11_B or SYSC0_PSSLVDCFGR.LVDL1V = 11_B

*4: These detection voltage level settings are below the minimum operation voltage.
Between these detection voltages and the minimum operation voltage, MCU functions are not guaranteed except for the low voltage detector.
Note that although the detection level is below the minimum operation voltage, the LVD reset factor flag is set as the voltage drops below the detection level.

10.11 A/D Converter

10.11.1 Electrical Characteristics

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Total Error	-	-	-	-	±12	LSB	*3
Integral Nonlinearity	-	-	-	-	±4.0	LSB	*4
Differential Nonlinearity	-	-	-	-	±1.9	LSB	*4
Zero transition voltage	V_{ZT}	*6	AVRL -11.5LSB	-	AVRL +12.5LSB	V	*5
Full-scale transition voltage	V_{FST}	*6	AVRH -13.5LSB	-	AVRH +10.5LSB	V	
Sampling time	t_{SMP}	-	0.3	-	12	µs	*1
Compare time	t_{CMP}	-	0.7	-	28	µs	*1
A/D conversion time	t_{CNV}	-	1.0	-	40	µs	*1
Analog port input current	I_{AIN}	*7	-1.0	-	1.0	µA	$V_{AVSS} \le V_{AIN} \le V_{AVCC}$
		*8	-2.0	-	2.0		
		*9	-3.0	-	3.0		
Analog input voltage	V_{AIN}	*6	AVSS	-	AVRH	V	
Reference voltage	AVRH	AVRH0, AVRH1	4.5	-	5.25	V	$AV_{CC} \ge$ AVRH
	AVRL	AVRL0/AVSS0, AVRL1/AVSS1	-	0.0	-	V	
Power supply current	I_A	AVCC	-	500	900	µA	per one unit
	I_{AH}		-	1.0	100	µA	*2
	I_R	AVRH	-	1	2	mA	per one unit
	I_{RH}		-	-	5.0	µA	*2
Variation between channels	-	*10	-	-	4	LSB	
		AN32 to AN62	-	-	4	LSB	

*1: Time for each channel

*2: The power supply current (V_{CC} = AV_{CC} = 5.0 V) is specified if the A/D converter is not operating and CPU is stopped.

*3: Total Error is a comprehensive static error that includes the linearity. 1LSB = (AVRH-AVRL)/4096

*4: 1LSB = (V_{FST}-V_{ZT})/4094

*5: 1LSB = (AVRH-AVRL)/4096

*6: AN0 to AN3, AN5, AN6, AN9, AN10, AN12 to AN15, AN17 to AN24, and AN27 to AN62

*7: AN3, AN5, AN6, AN9, AN10, AN12 to AN15, AN17 to AN24, and AN27 to AN42

*8: AN0 to AN2, and AN43

*9: AN44 to AN62

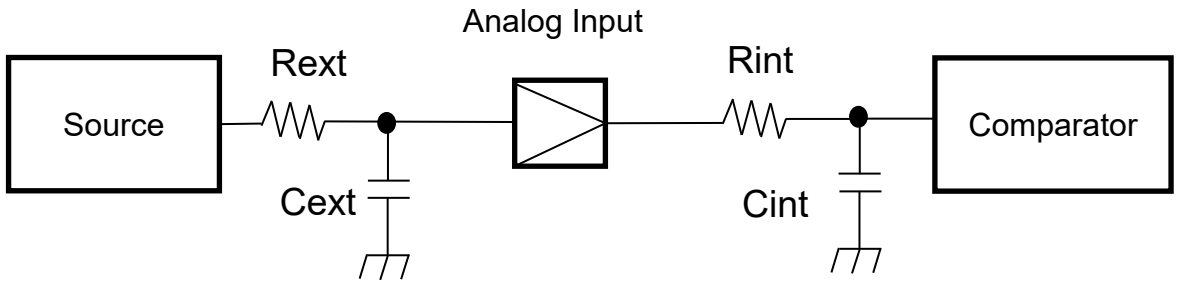
*10: AN0 to AN3, AN5, AN6, AN9, AN10, AN12 to AN15, AN17 to AN24, and AN27 to AN31

10.11.2 Notes on Using A/D Converters

About the output impedance of an external circuit for analog input

When the external impedance is too high, the analog voltage sampling time may become insufficient. In this case, we recommend attaching a capacitor (about 0.1 µF) to an analog input pin.

Analog Input Circuit Model



Rint : Analog input impedance
3.9 kilo ohms (max) (4.5V≤AV_{CC}≤5.25V)
Cint : Capacitance of MCU input pin
11.0pF (max) (4.5V≤AV_{CC}≤5.25V)
Rext : External driving impedance
Cext : Capacitance of PCB at A/D converter input

The following approximation formula for the replacement model above can be used:
sampling time (minimum) = 9 × ((Rint + Rext) × Cint + Rext × Cext)

Note: Listed values must be considered as reference values.

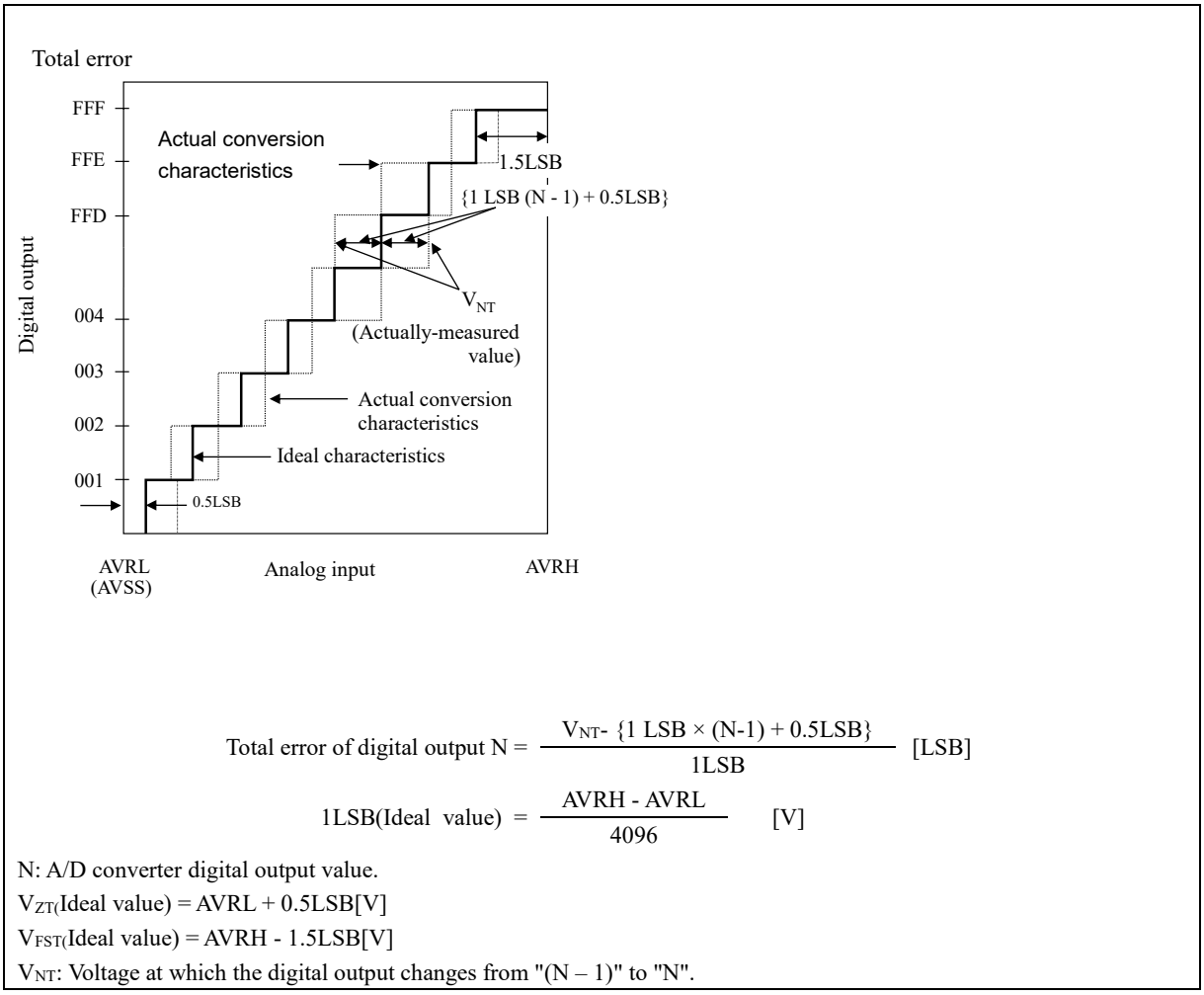
10.11.3 Definition of terms

Resolution: Analog variation that is recognized by an A/D converter

Integral Nonlinearity error *: Deviation of the straight line connecting the zero transition point ("0000 0000 0000" <--> "0000 0000 0001") and full-scale transition point ("1111 1111 1110" <--> "1111 1111 1111") from actual conversion characteristics includes zero transition error, full-scale transition error, and non-linearity error.

Differential Nonlinearity error: Deviation from the ideal value of the input voltage required for changing the output code by 1 LSB
Total error: Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and non linearity error.

*: Represented as "Linearity error" in the former product series.



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + 0.5\text{LSB}\}}{1\text{LSB}} \quad [\text{LSB}]$$

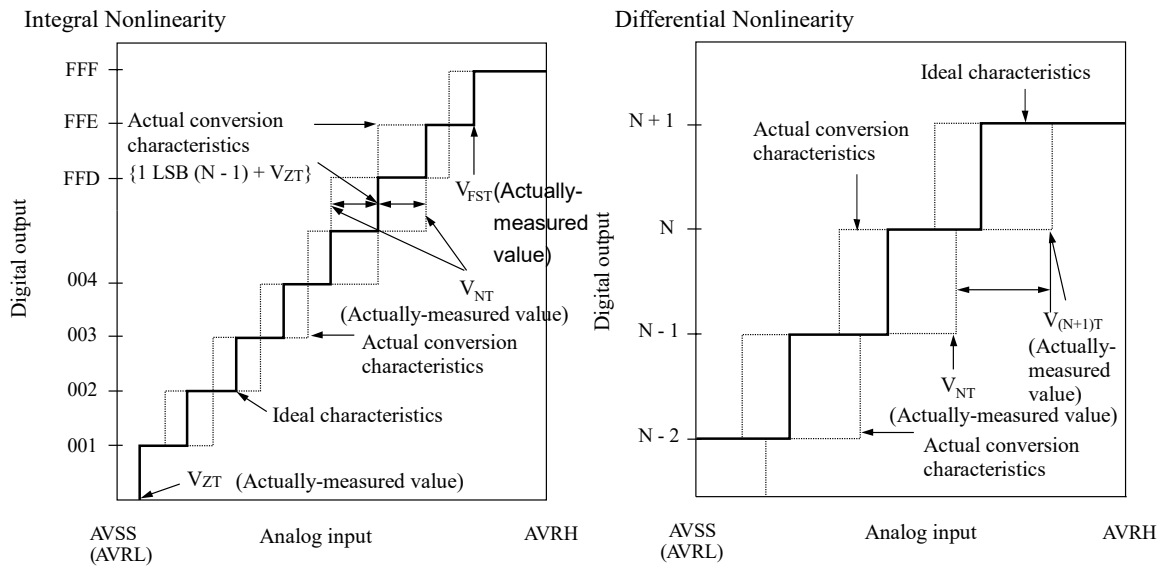
$$1\text{LSB(Ideal value)} = \frac{\text{AVRH} - \text{AVRL}}{4096} \quad [\text{V}]$$

N: A/D converter digital output value.

V_{ZT}(Ideal value) = AVRL + 0.5LSB[V]

V_{FST}(Ideal value) = AVRH - 1.5LSB[V]

V_{NT}: Voltage at which the digital output changes from "(N – 1)" to "N".



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + V_{ZT}\}}{1\text{LSB}}\ [\text{LSB}]$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)}T - V_{NT}}{1\text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\text{LSB} = \frac{V_{FST} - V_{ZT}}{4094}\ [\text{V}]$$

V_{ZT}: Voltage for which digital output changes from "0x000" to "0x001"

V_{FST}: Voltage for which digital output changes from "0xFFE" to "0xFFF".

10.12Flash Memory

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	300	1100	ms	8-KB sector[*1] Internal preprogramming time included
	-	800	3700	ms	64-KB sector[*1] Internal preprogramming time included
8-bit write time	-	15	288	µs	System-level overhead time excluded[*1]
16-bit write time	-	19	384	µs	System-level overhead time excluded[*1]
32-bit write time	-	27	567	µs	System-level overhead time excluded[*1]
64-bit write time	-	45	945	µs	System-level overhead time excluded[*1]
8-bit (with ECC) write time	-	19	384	µs	System-level overhead time excluded[*1]
16-bit (with ECC) write time	-	23	483	µs	System-level overhead time excluded[*1]
32-bit (with ECC) write time	-	31	651	µs	System-level overhead time excluded[*1]
64-bit (with ECC) write time	-	49	1029	µs	System-level overhead time excluded[*1]
Erase count[*2]/ Data retention time	1,000/20 years, 10,000/10 years, 100,000/5 years	-	-	-	Temperature at write/erase time Average temperature T_A = +85 degrees Celsius

[*1] Guaranteed value for up to 100,000 erases

[*2] Number of erases for each sector

Notes:

- While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited.
- In the application system where V_{CC} might be shut down while writing or erasing, be sure to turn the power off by using an external low-voltage detection function.
- To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}), hold V_{CC} at 2.7 V or more within the duration calculated by the following expression:
  T_d[*1] [µs] + (1 / F_{CRF}[*2][MHz]) x 1029 + 25 [µs]

  [*1] : See "10.8 Low-voltage detection (external low-voltage detection)"

  [*2] : See "10.4.1 Source clock timing"

11. Ordering Information

Part Number	Package
S6J311xHzCSEy0000	144-pin Plastic TEQFP (LEU144)

Note:

- "x"/"y" is a part number option. For the part number option, see the following table. For details on each package, see "PACKAGE DIMENSIONS."
  * z: A

12. Part Number Option

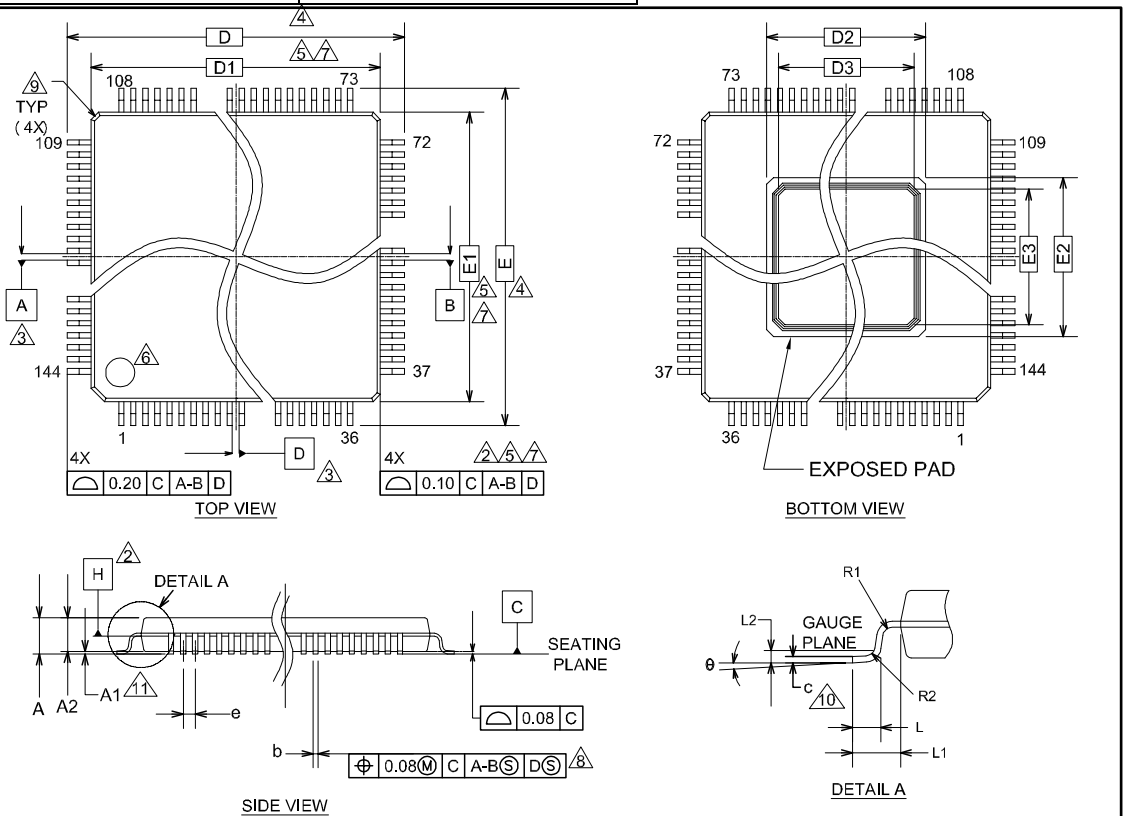
Part Number Option "x"	FLASH Memory
A	1 MByte
9	768 KByte

Part Number Option "y"	
2	PureSn & Halogen Free

Part Number Option "z"	SHE
A	SHE ON

13. Package Dimensions

Package Type	Package Code
Ex-LQFP 144	LEU144



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.05	——	0.15
A2	1.35	1.40	1.45
D	22.00 BSC.		
D1	20.00 BSC.		
D2	7.05 BSC.		
D3	5.85 BSC.		
E	22.00 BSC.		
E1	20.00 BSC.		
E2	7.05 BSC.		
E3	5.85 BSC.		

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
b	0.17	0.22	0.27
e	0.50 BSC.		
R1	0.08	——	——
R2	0.08	——	0.20
θ	0°	4°	8°
c	0.12	——	0.20
L	0.45	0.60	0.75
L1	1.00 REF.		
L2	0.25		

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-10858 *A

PACKAGE OUTLINE, 144 LEAD TEQFP
20.0X20.0X1.7 MM LEU144

14. Errata

This section describes the errata for the S6J3110 Series. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number
S6J311AHACSE20000 S6J3119HACSE20000

S6J3110 Qualification Status

Product Status: Production

Errata Summary

The following table defines the errata applicability to available S6J3110 Series devices.

Items	Part Number	Fix Status
1. MCAN Wrong Message Transmission	S6J311AHACSE20000 S6J3119HACSE20000	No silicon fix planned
2. CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID		
3. CAN FD: Incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID		

1. MCAN Wrong Message Transmission

■ Problem Definition

There is a possibility a message with an ID (arbitration field) and a format and DLC (control field) is transmitted which was not configured by the application. The message itself is syntactically correct and can be received by other nodes.

The occurrence of the limitation requires a certain relationship in time between a transmission request for sending a message and the coincidence of noise in the 3rd bit of intermission field which is treated as the start of new message transmission (SoF).

■ Trigger Condition

Under the following conditions a message with wrong ID, format and DLC is transmitted:

- M_CAN is in state "Receiver" (PSR.ACT = "10"), no pending transmission.
- A new transmission is requested after sample point of 2nd bit of intermission but before the 3rd bit of Intermission is reached.
- The CAN bus is sampled dominant at the third bit of Intermission which is treated as SoF (see ISO11898-1:2015 Section 10.4.2.2).

■ Scope of Impact

Under the conditions listed above it may happen, that:

- The shift register is not loaded with ID, format, and DLC of the requested message.
- The M_CAN will start arbitration with wrong ID, format, and DLC.
- In case the ID won arbitration, a CAN message with valid CRC is transmitted.

- In case this message is acknowledged, the ID stored in the Tx Event FIFO is the ID of the requested Tx message and not the ID of the message transmitted on the CAN bus
- Neither an error is detected by the transmitting node nor at the receiving node.

■ Workaround

Workaround 1:

This workaround avoids submitting a transmission request in the critical time window of about one bit time before the sample point of the 3rd bit of intermission field when on other pending transmission request exists:

- Request a new transmission if another transmission is already pending or when the M_CAN / M_TTCAN is not in state "Receiver" (when PSR.ACT ≠ "10").
- If no pending transmission request exists, the application software needs to evaluate the Rx Interrupt flags IR.DRX, IR.RF0N, IR.RF1N which are set at the last bit of EoF when a received and accepted message gets valid.
- A new transmission may be requested by writing to TXBAR once the Rx interrupt occurred and the application waited another 3 bit times before submitting its Tx request. Note the Rx interrupt is generated at the last bit of EoF which is followed by three bits of Intermission.
- The application has to take care that the transmission request for the CAN Protocol Controller is activated before the critical window of the following reception is reached.

A supplemental action can be applied in order to detect messages which contain wrong ID and control filed information:

- A checksum covering arbitration and control fields can be added to the data field of the message to be transmitted, to detect frames transmitted with wrong arbitration and control fields.

Workaround 2:

This workaround ensures that always at least one pending Tx request exists. If that is the case, the application may launch its Tx requests at any time without suffering from the limitation.

- Define a low priority message with DLC = 0 that can be sent without harm. E.g. loses arbitration against all other application messages, does not pass any acceptance filter of nodes in the same network. DLC = 0 shall reduce latency for other application messages.
- Configure sufficient Tx buffers – at least two - for this message type thus that there is always another one waiting to be sent. E.g. an application that cannot react quickly enough with the time a single message of this type is sent, more than 2 Tx buffer may become necessary.
- The application uses the standard interfaces of the CAN / CAN FD stack to feed these messages.
- Whenever Tx confirmation is indicated for the second but last message of this type with pending Tx request, the application needs to submit at least one new Tx request. Note Tx confirmation is a standard feature in the AUTOSAR SW architecture.
- Before initially leaving INIT state of the M_CAN IP by clearing CCCR.INIT bit, make sure to activate a Tx request after having cleared CCCR.CCE. This will ensure that the conditions for the occurrence of the limitation when synchronizing to the CAN bus the first time after RESET are prevented.

■ Fix Status

No silicon fix planned

2. CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID

■ Problem Definition

CAN FD controller message order inversion when multiple Tx Buffers that are configured with the same Message ID have pending Tx requests.

■ Configuration

Several Tx Buffers are configured with the same Message ID. Transmission of these Tx Buffers is requested sequentially with a delay between the individual Tx requests.

■ Expected behavior

When multiple Tx Buffers that are configured with the same Message ID have pending Tx requests, they shall be transmitted in ascending order of their Tx Buffer numbers. The Tx Buffer with lowest buffer number and pending Tx request is transmitted first.

■ Observed behavior

It may happen, depending on the delay between the individual Tx requests, that where multiple Tx Buffers are configured with the same Message ID the Tx Buffers are not transmitted in order of the Tx Buffer number (lowest number first).

■ Workaround

First, write the group of Tx messages with the same Message ID to the Message RAM and then request transmission of all these messages concurrently by a single write access to TXBAR. Before requesting a group of Tx messages with this Message ID, ensure that no message with this Message ID has a pending Tx request.
Applications not able to use the above workaround can implement a counter within the data section of their messages sent with same ID in order to allow the recipients to determine the correct sending sequence.

■ Fix Status

No silicon fix planned

3. CAN FD: Incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID

■ Problem Definition

There was an incomplete description related to transmission from multiple buffers configured with the same Message ID in Section 3.5.2 Dedicated Tx Buffers and Section 3.5.4 Tx Queue of the Hardware Manual..

■ Detailed explanation

The following is the updated description in Section 3.5.2 Dedicated Tx Buffers and Section 3.5.4 Tx Queue of the Hardware Manual.

Section 3.5.2 Dedicated Tx Buffers:

- Original content in the hardware manual:

In case that multiple Tx Buffers are configured with the same Message ID, the Tx Buffer with the lowest buffer number is transmitted first.

- Enhancement:

These Tx buffers shall be requested in ascending order with the lowest buffer number first. Alternatively, all Tx buffers configured with the same Message ID can be requested simultaneously by a single write access to TXBAR.

Section 3.5.4 Tx Queue:

- Original content in the Hardware Manual:

In case that multiple Queue Buffers are configured with the same Message ID, the Queue Buffer with the lowest buffer number is transmitted first.

- Replacement:

In case that multiple Tx Queue buffers are configured with the same Message ID, the transmission order depends on numbers of the buffers where the messages were stored for transmission. As these buffer numbers depend on the then current states of the PUT index, a prediction of the transmission order is not possible.

- Original content in the Hardware Manual:

An Add Request cyclically increments the Put Index to the next free Tx Buffer.

- Replacement:

The Put Index always points to that free buffer of the Tx Queue with the lowest buffer number.

■ **Workaround**

In case a defined order of transmission is required the Tx FIFO shall be used for transmission of messages with the same Message ID. Alternatively dedicated Tx buffers with same Message ID shall be requested in ascending order with lowest buffer number first or by a single write access to TXBAR. Alternatively, a single Tx Buffer can be used to transmit those messages one after the other.

■ **Fix Status**

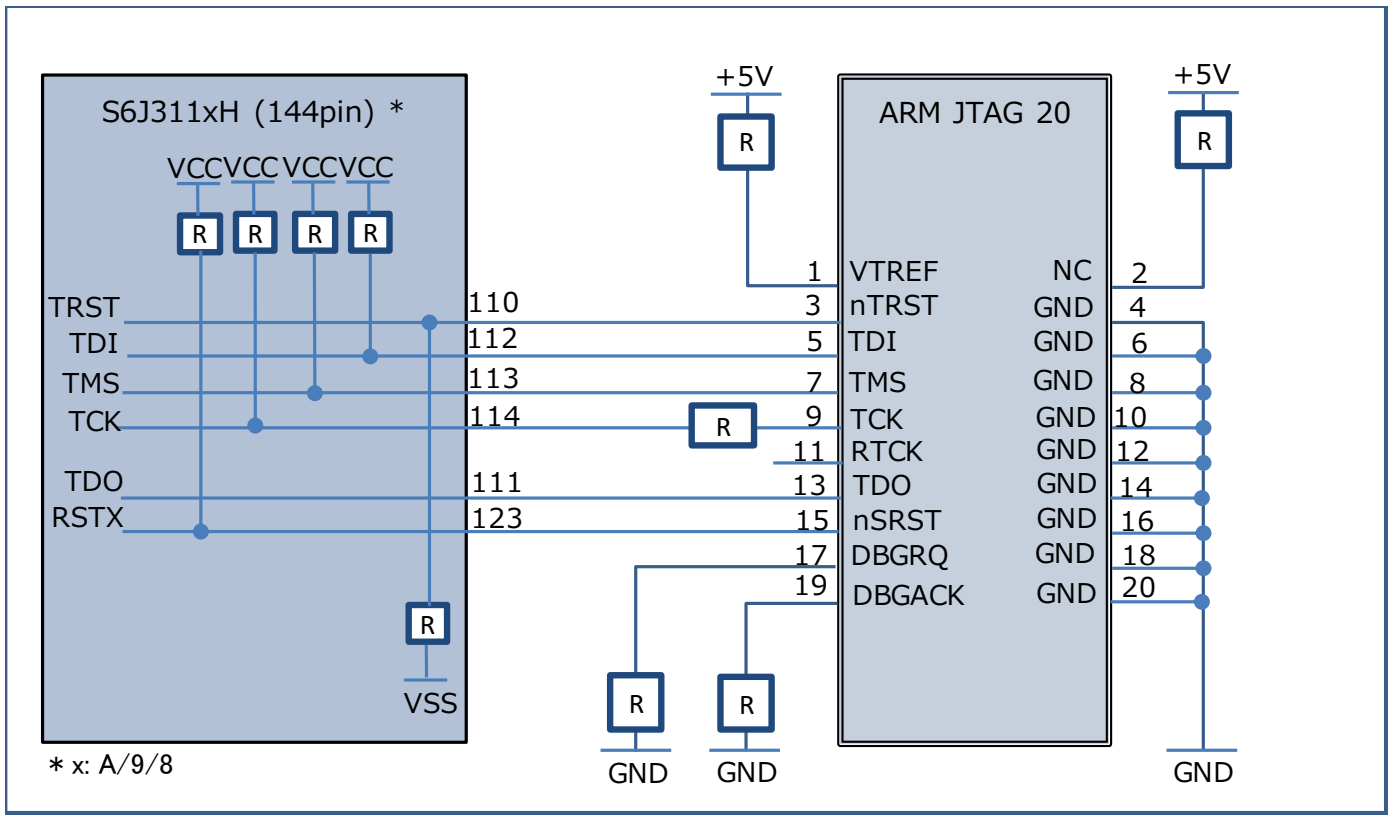
No silicon fix planned. Use workaround.

Hardware Manual will be updated accordingly.

15. Appendix

15.1 Application 1: JTAG tool connection

This is an application example of JTAG tool connection. See the relevant application note AN203911 in detail.



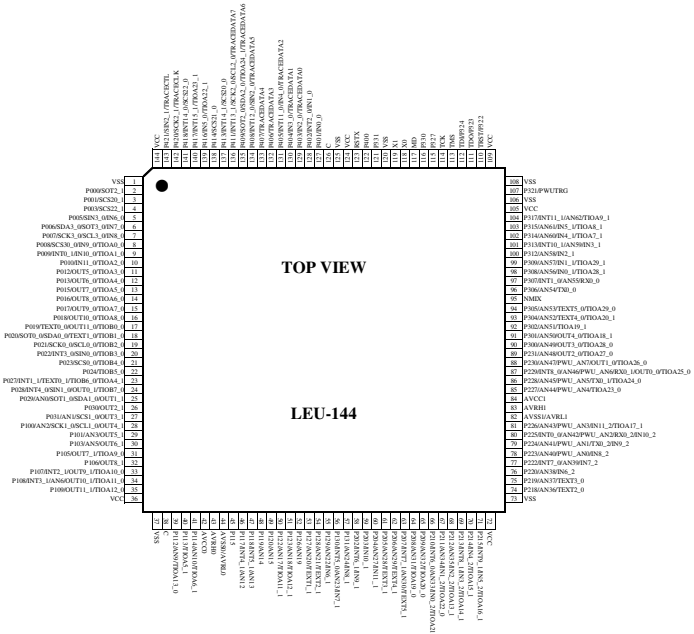
16. Major Changes

Spansion Publication Number: S6J311A_DS708-00004

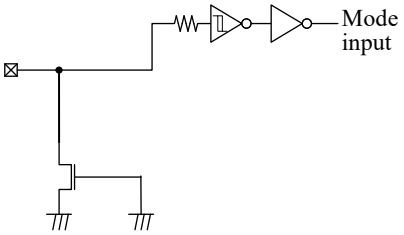
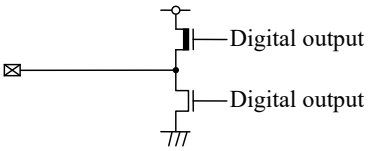
Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 1.0		
1,3	Cover	Added the family product names(S6J3119HAA / S6J3118HAA)
1,3	Cover	Revised the level of this data sheet as full production
6	2. Features 2.2 Peripheral Functions	Added the information about the memory capacity expansion
7	2. Features 2.2 Peripheral Functions	Revised the CAN transfer speed to 5Mbps
9	3. Product Lineup	Added the specifications as full production
11	4. Pin Assignment	Revised the product names of title S6J311AHAA-> S6J311xHAA
12	5. Pin Description	Revised the product names of title S6J311AHAA-> S6J311xHAA
12~21	5. Pin Description	Revised the product names of Pin No. S6J311AHAA-> S6J311xHAA
30	8. Handling Devices	Revised the note of “About power supply pins”
32	8. Handling Devices	Revised the note of “About C pin processing”(Delete “and pin 38”)
33	9. Block Diagram	Revised the block diagram of S6J311xHAA as full production
34	10. Memory Map	Revised the memory map of S6J311xHAA (added information of S6J3119HAA / S6J3118HAA)
36	10.Memory Map	Revised the product names of title S6J311AHAA-> S6J311xHAA
42,44,52,55	12. Electrical Characteristics	Added the product names S6J311AHAA-> S6J311xHAA
42	12. Electrical Characteristics 12.1 Absolute Maximum Ratings	Revised “Remarks” of Analog supply voltage to “AV_{CC}=V_{CC}”
42	12. Electrical Characteristics 12.1 Absolute Maximum Ratings	Revised the note of *2
42	12. Electrical Characteristics 12.1 Absolute Maximum Ratings	Revised the symbol of Maximum clamp current
43	12. Electrical Characteristics 12.1 Absolute Maximum Ratings	Moved the note of *8 to the bottom of note
44	12. Electrical Characteristics 12.2 Recommended Operating Conditions	Delete the information about CS2
44	12. Electrical Characteristics 12.2 Recommended Operating Conditions	Revised C pin connection diagram
44	12. Electrical Characteristics 12.2 Recommended Operating Conditions	Added “Remarks” of Smoothing capacitor
45	12. Electrical Characteristics 12.3 DC Characteristics	Revised the minimum value of VIH6 2.0 -> 2.3
52	12. Electrical Characteristics 12.3 DC Characteristics	Revised the following DC characteristics I_{CC5}, I_{CCS5}, I_{CCT52}, I_{CCH52}
55	12. Electrical Characteristics 12.4.2 Internal Clock Timing	Revised the product names in the table S6J311AHAA-> S6J311xHAA
55	12. Electrical Characteristics 12.4.2 Internal Clock Timing	Delete the line of FCD0_CLK and tCD0_CLK
57	12. Electrical Characteristics 12.4.2 Internal Clock Timing	Revised the note as follow FCDO_CLK->FCPU_CLK
58	12. Electrical Characteristics 12.4.2 Internal Clock Timing	Revised the voltage value of Hysteresis input pin (TTL). 2.0V -> 2.3V
60	12. Electrical Characteristics 12.4.4 Power-on Conditions	Revised the value of Level detection voltage
60	12. Electrical Characteristics 12.4.4 Power-on Conditions	Added the line of Level release voltage

Page	Section	Change Results
75	12. Electrical Characteristics 12.4.5.1 CSIO Timing (SMR:MD[2:0]=010B)	Added the Figure of 5-1-7(1st, 2nd, 3rd)
82	12. Electrical Characteristics 12.6 Trigger Input Timing	Deleted the following pin names in the table of “Input pulse width” and figure of “Trigger input timing” “RX0”, “RXx”
86	12. Electrical Characteristics 12.11.1 Electrical Characteristics	Revised the value of “Analog port input current” in the table, and revised the pin name note *7 to *9
86	12. Electrical Characteristics 12.11.1 Electrical Characteristics	Revised the pin name note of “Variation between channels” *7 -> *10
89	12. Electrical Characteristics 12.11.3 Definition of Terms	Revised the note of “Total error”
91	12. Electrical Characteristics 12.12 Definition of Terms	Deleted the note *3
92	13. Ordering Information	Revised the note of “Package”
92	14. Part Number Option	Added the part number options as full production
Revision *A		
1	Features Cortex-R5 Core	Revised the following note (Error) ECC support for the TCM ports (Correct) ECC support for the TCM ports for RAM
1	Features Peripheral Functions	Revised the full production and SHE-OFF series as follows: (Correct) Built-in flash memory size −Program: 1024 K + 64 KB (S6J311AHzB*) / 768 K + 64 KB (S6J3119HzB*) / 512 K + 64 KB (S6J3118HzB*) −Work: 48 KB (S6J311AHzB*) / 48 KB (S6J3119HzB*) / 48 KB (S6J3118HzB*) *z: A/B
1	Features Peripheral Functions	Revised the full production and SHE-OFF series as follows: (Correct) Built-in RAM size −TCRAM 64 KB (S6J311AHzB*) / 48 KB (S6J3119HzB*) / 32 KB (S6J3118HzB*) −System SRAM 16 KB (S6J311AHzB*) / 16 KB (S6J3119HzB*) / 16 KB (S6J3118HzB*) −Backup RAM 8 KB (S6J311AHzB*) / Backup RAM 8 KB (S6J3119HzB*) / Backup RAM 8 KB (S6J3118HzB*) *z: A/B
1	Features Peripheral Functions	Revised the full production and SHE-OFF series as follows: (Correct) General-purpose ports: 116 channels (S6J311AHzB*) / 116 channels (S6J3119HzB*) / 116 channels (S6J3118HzB*) *z: A/B
1	Features Peripheral Functions	Revised the full production and SHE-OFF series as follows: (Correct) A/D converter (successive approximation type) 12-bit resolution, 2 units mounted: Max 56 channels (25 channels + 31 channels) (S6J311AHzB*) / Max 56 channels (25 channels + 31 channels) (S6J3119HzB*) / Max 56 channels (25 channels + 31 channels) (S6J3118HzB*) *z: A/B
1	Features Peripheral Functions	Revised the full production and SHE-OFF series as follows: (Correct) Multi-function serial (transmission and reception FIFOs mounted) :Max 4 channels (S6J311AHzB*) / Max 4 channels (S6J3119HzB*) / Max 4 channels (S6J3118HzB*) *z: A/B

Page	Section	Change Results
1	FEATURES Peripheral Functions	Added the following function lists: <I²C> - Full-duplex double buffering system, 64-byte transmission FIFO, 64-byte reception FIFO. −Standard mode (Max. 100kbps) is supported only. −DMA transfer is supported
2	FEATURES Peripheral Functions CAN controller: CAN-FD Max 1 channel	Added the following function list: −32 message buffer/channel (transmission message buffer size)
2	Features Peripheral Functions	Revised the full production and SHE-OFF series as follows: (Correct) −Package: LEU144 (S6J311xHzB*) *z: A/B
2	Features Peripheral Functions	Added ”−Partial wakeup function”
4	1. Product Lineup	Revised the full production and SHE-OFF series of “Table 3-1 Memory Size” (Error) S6J311AHAA S6J3119HAA S6J3118HAA (Correct) S6J311AHzB* S6J3119HzB* S6J3118HzB* *z: A/B
4	1. Product Lineup	Added Table 3-2. SHE option as follows: Table 1-2. SHE option | | S6J311xHAB* | S6J311xHBB* | | Security (SHE) | ON | OFF | * x: A/9/8
4	1. Product Lineup	Revised the full production and SHE-OFF series of “Table 1-3: Product Lineup” (Error) S6J311xHAA (Correct) S6J311xHzB* * x: A/9/8, z: A/B
5	1.Product Lineup	Added ”Partial wakeup function”

Page	Section	Change Results
6	2. Pin Assignment	Revised “Figure 2-1 Pin Assignment for S6J311xHzB*” as follows. (Correct) * x: A/9/8, z: A/B 
7	3. Pin Description	Revised the tables as follows for full production. (Correct) Table 3-1 S6J311xHzB* Pin Functions * x: A/9/8, z: A/B
7 to 13	3. Pin Description	Added the I2C function to Pin 6,7,18,19,25,28,135,136. Pin 6 SDA3_0 I²C bus ch.3 serial data I/O pin Pin 7 SCL3_0 I²C bus ch.3 serial clock I/O pin Pin 18 SDA0_0 I²C bus ch.0 serial data I/O pin Pin 19 SCL0_0 I²C bus ch.0 serial clock I/O pin Pin 25 SDA1_0 I²C bus ch.1 serial data I/O pin Pin 28 SCL1_0 I²C bus ch.1 serial clock I/O pin Pin 135 SDA2_0 I²C bus ch.2 serial data I/O pin Pin 136 SCL2_0 I²C bus ch.2 serial clock I/O pin

Page	Section	Change Results
11	3. Pin Description	Added the Partial wakeup function from Pin 78to Pin 81, and from Pin 85 to Pin88. 78 AN40 ADC analog 40 input pin PWU_AN0 Partial wakeup ADC analog 0 input pin 79 AN41 ADC analog 41 input pin PWU_AN1 Partial wakeup ADC analog 1 input pin 80 AN42 ADC analog 42 input pin PWU_AN2 Partial wakeup ADC analog 2 input pin 81 AN43 ADC analog 43 input pin PWU_AN3 Partial wakeup ADC analog 3 input pin 85 AN44 ADC analog 44 input pin PWU_AN4 Partial wakeup ADC analog 4 input pin 86 AN45 ADC analog 45 input pin PWU_AN5 Partial wakeup ADC analog 5 input pin 87 AN46 ADC analog 46 input pin PWU_AN6 Partial wakeup ADC analog 6 input pin 88 AN47 ADC analog 47 input pin PWU_AN7 Partial wakeup ADC analog 7 input pin
12	3.Pin Description	Revised the “I/O Circuit Type “and add PWUTRG to Pin 107 (Correct) 107 P321 - R General-purpose output port PWUTRG - Partial wakeup trigger output pin

Page	Section	Change Results
15	4. I/O Circuit Types	Revised Type C of “I/O Circuit Type” as follows: (Correct) 
17	4. I/O Circuit Types	Added Type R to “11. I/O Circuit Type” R  Output of 2 mA
22	5.Handling Devices	Revised the following notice. (Error) About the Power-on Time To prevent the internal built-in voltage step-down circuit from malfunctioning, secure a voltage rising time of 50 µs (between 0.2 V and 2.7 V) or longer at the power-on time. (Correct) About the Power-on Time To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic during power-on.
22	5.Handling Devices	Revised the item as follows: (Error) This device has a built-in voltage step-down circuit. Be sure to connect a capacitor to the C pin (pin 126 in S6J311xHAA specifications) (Correct) This device has a built-in voltage step-down circuit. Be sure to connect a capacitor to the C pin (pin 126 in S6J311xHzB* specifications) *x:A/9/8, z: A/B
23	7.Block Diagram	Revised the title as follows: (Error) Figure 7-1 S6J311xHAA Block Diagram (Correct) Figure 7-1 S6J311xHzB* Block Diagram * x: A/9/8, z: A/B
23	7.Block Diagram	Added “Partial Wake up” to “Block Diagram”
24	8.Memory Map	Revised Figure 8-1 as follows (Correct) Figure 8-1 Memory Map (S6J311AHzB/9HzB/8HzB*) * z: A/B
25	8.Memory Map	Added item as follows: “The ECC movement in TCM port is based on ECC setting inside the CPU.”

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>26</td><td>8.Memory Map</td><td>Revised " S6J311xHAA Peripheral Map" as follows
(Correct)
S6J311xHzB* Peripheral Map
* x:A/9/8, z:A/B</td></tr>
<tr><td>28</td><td>8.Memory Map</td><td>Added “Partial Wake Up” to address of “B484_8400 to B484_87FF”.
<table><tr><td>B484_8400</td><td>B484_87FF</td><td>APPS #5</td><td>A/D unit1 , Partial Wake Up</td><td>297</td></tr></table></td></tr>
<tr><td>28</td><td>8.Memory Map</td><td>Revised the memory map of APPS#5 as follows.
(Correct)<table><tr><td>B484_8C00</td><td>B484_8FFF</td><td></td><td>Reserved</td><td>-</td></tr><tr><td>B484_9000</td><td>B484_93FF</td><td>APPS #5</td><td>Global Timer</td><td>300</td></tr><tr><td>B484_9400</td><td>B484_FFFF</td><td></td><td>Reserved</td><td>-</td></tr></table></td></tr>
<tr><td>28</td><td>8. Memory Map</td><td>Added the following comments and restriction under the table of “APPS#5 area”

When MPU attribute of Cortex-R5 is configured as "Normal", store buffer inside Cortex-R5 can operate and write data can be merged. To avoid influence of this data merger, MPU attribute "Device" or "Strongly Ordered" should be used.
MPU attribute "Device" or "Strongly Ordered" must be used for areas below, to avoid this influence.
− Backup RAM area (BACKUP_RAM) [0E80_0000 ~ 0E87_FFFF]
− Peripheral area (Peri area) [B000_0000 ~ B7FF_FFFF]
− Error Config area (ERRCFG) [FFFE_E000 ~ FFFE_FFFF]
MPU attribute "Device" or "Strongly Ordered" is required for accesses to areas below, in particular situation.
− FLASH Memory (when writing commands)
SHE OFF product is prohibited to access SHE area (B200_0000 to B20F_FFFF)</td></tr>
<tr><td>29,30</td><td>9. Pin Status in CPU Status</td><td>Added Pin name about I²C and PWU to Table 9-1 Pin State Table (1/2) and Table 9-2 Pin State Table (2/2).</td></tr>
<tr><td>31</td><td>9. Pin Status in CPU Status</td><td>Added the item as follows
*5: When the PWU function is enabled, a change to output occurs.
*7: When PPC_PCFGRijj:POF[2:0] is set to initial value.</td></tr>
<tr><td>32,33</td><td>10. Electrical Characteristics
10.1 Absolute Maximum Ratings</td><td>Revised “S6J311xHAA” to “S6J311xHzB”
Added ”* x:A/9/8, z:A/B” to “*8”.</td></tr>
<tr><td>34</td><td>10. Electrical Characteristics
10.2 Recommended Operating Conditions</td><td>Revised “S6J311xHAA” to “S6J311xHzB”
Added ”* x: A/9/8, z: A/B”.</td></tr>
</table>

Page	Section	Change Results
35	10. Electrical Characteristics 10.2 Recommended operating conditions	Added the following notes -The following condition should be satisfied in order to facilitate heat dissipation. 1.4 or more layers PCB should be used. 2.The area of PCB should be 114.3 mm x 76.2 mm or more, and the thickness should be 1.6 mm or more. (JEDEC standard) 3.1 layer of middle layers at least should be used for dedicated layer to radiate heat with residual copper rate 90% or more. The layer can be used for system ground. 4.35~50% of the die stage area which is exposed at back surface of package should be soldered to a part of 1st layer. 5.The part of 1st layer should be connected to the dedicated heat radiation layer with more than 10 thermal via holes.
35	10. Electrical Characteristics 10.2 Recommended operating conditions	Added the following notes −Figure10.2-1 is a schematic diagram showing PCB in section. −Figure10.2-2 in the following pages are recommended land patterns for each package series. Thermal via holes should closely be placed and aligned with lands. −If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.
35,36	10. Electrical Characteristics 10.2 Recommended operating conditions	Added the following figures Figure 10.2-1: Example thermal via holes on PCB. Figure 10.2-2: Land Pattern and Thermal Via LEU144
41	10. Electrical Characteristics 10.3 DC Characteristics	Deleted the pin name “P321” in Rup3 of Pull-up register.
43	10. Electrical Characteristics 10.3 DC Characteristics	Revised “S6J311xHAA” to “S6J311xHzB” Added”* x: A/9/8, z: A/B”.
43	10. Electrical Characteristics 10.3 DC Characteristics	Added the following symbol and value I_{CCP}
45	10. Electrical Characteristics 10.4.2 Internal Clock Timing	Revised “S6J311xHAA” to “S6J311xHzB” Added”* x: A/9/8, z: A/B”.
49	10. Electrical Characteristics 10.4.4 Power-on Conditions	Deleted the Slope detection undetected specification. Added the Power ramp rate and Maximum ramp rate guaranteed to not generate power-on reset. *1, *2: Changed the sentence. Added *3, *4, Note, Figure at the Power off time, Power ramp rate, Maximum ramp rate guaranteed to not generate power-on reset.
69,70	10. Electrical Characteristics 10.4.5.4 I2C timing (SMR:MD[2:0]=100B)	Added”10.4.5.4 I^2C timing (SMR:MD[2:0]=100B)” as a new item.
75	10. Electrical Characteristics 10.9 Low-Voltage Detection (RAM Retention Low-Voltage Detection)	Revised the title in 10.9 “Internal Low-Voltage Detection” to “RAM Retention Low-Voltage Detection”.
75	10. Electrical Characteristics 10.10 Low-Voltage Detection (1.2 V Power Supply Low-Voltage Detection)	Added the notice *4
81	11. Ordering Information	Added SHE option to the part number
81	11. Ordering Information	Revised Package Code “LES144” to “LEU144”
81	12. Part Number Option	Added Part Number Option “z” as SHE option
Revision *I		
77, 79, 80	14. Errata	Added about CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID

Revision *J		
77, 79, 80	14. Errata	Added CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID

NOTE: Please see “Document History” for later revised information.

Document History

Document Title: S6J311A, S6J3119 32-Bit TRAVEO™ T1G Family S6J3110 Series Microcontroller Datasheet
Document Number: 002-04632

Revision	ECN	Submission Date	Description of Change
**	-	01/16/2015	Migrated to Cypress and assigned document number 002-04632. No change to document contents or format.
*A	5272677	05/16/2016	Updated to Cypress format. Adapted to full-production. Added some characteristics. For detail, see “Major Changes”.
*B	5311072	06/20/2016	Page 1, Revised the title as follows (error) S6J3110 Series 32-Bit TraveoTM Family Microcontroller Datasheet (correct) S6J311A, S6J3119, S6J3118 32-Bit Traveo™ Family S6J3110 Series Microcontroller Datasheet Page 2, Features Added “CAN-FD (V3.2.0)” under “CAN controller: CAN-FD Max 1 channel”. In page of 1,2,4 to 14,22 to 24,26,32,34,43,45,46,49,81 Revised part number from S6J311xxxB to S6J311xxxC.
*C	5375461	07/27/2016	Page49, 10.4.4 Power-on Conditions Revised Level detection time from 30 to 540, Revised *1 to *4 and Note. Page75, 10.9 Low-Voltage Detection (RAM Retention Low-Voltage Detection)

Revision	ECN	Submission Date	Description of Change
			Added * and Note to Detection voltage. Page75, 10.10 Low-Voltage Detection (1.2 V Power Supply Low-Voltage Detection) Added * and Note to Detection voltage.
*D	5554882	12/15/2016	Page 82, Replaced 13. Package Dimensions Page 83, Added 14. Appendix
*E	5782586	06/22/2017	Updated Cypress logo. Updated Copyright.
*F	5998871	12/19/2017	Sunset update. Updated Figure (spec 002-10858 ** to *A) in Package Diagram.
*G	6231567	07/06/2018	Part Number Option is updated.
*H	6294152	08/29/2018	Page 77 Added 14. Errata
*I	7100292	03/08/2021	Updated 14. Errata. For details, see 16. Major Changes.
*J	7388124	10/25/2021	Updated 14. Errata. For details, see 16. Major Changes.

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