Optical Modulator Driver with Internal Attenuator and Power Detector

Data Sheet

HMC7810A

FEATURES

- 32.0 Gbps maximum data rate
- 13 ps typical output rise time and fall time
- 28 GHz bandwidth
- Self biased, no power sequencing required
- Adjustable gain
- Integrated output peak detector
- Low power consumption
- 0.5 W with 3.3 V positive/negative external supply voltage
- 0.44 W with 2.5 V positive/negative external supply voltage
- Use with compact bias tee: 1 inch × 0402 + 1 inch × 0603, SMT only
- 16-terminal, 2.9 mm × 2.9 mm, leadless chip carrier (LCC) package
- Differential balanced outputs

APPLICATIONS

- Communication infrastructure: 400 G 16 QAM, 100 G DP-QPSK pluggable optical modules in CFP/CFP2
- Broadband gain stage and pre-amplifiers
- Broadband test and measurement equipment

FUNCTIONAL BLOCK DIAGRAM

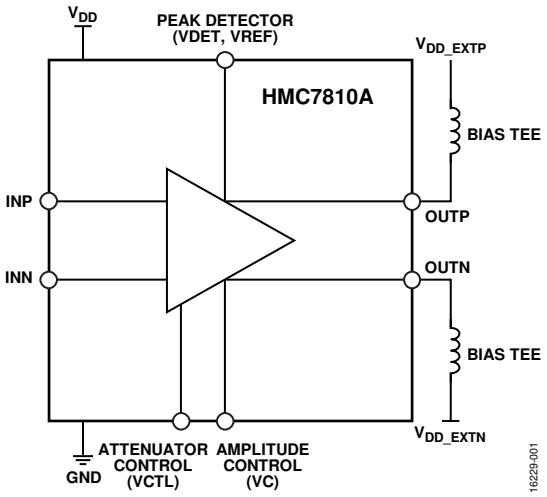


Figure 1.

GENERAL DESCRIPTION

The HMC7810A is a differential input and differential output, broadband linear amplifier, capable of driving a differential indium phosphate (InP) Mach-Zehnder (MZ) modulator for data center interconnect fiber optics or silicon photonics, or driving a single-ended, electroabsorption modulated laser (EML) modulator for short reach or metro applications. The HMC7810A supports data rates up to 32.0 Gbps with a gain flatness of up to 20 GHz. The integrated peak detector at the output enables system designers to maintain constant output by adjusting the gain of the amplifier via the VCTL pin through an external automatic gain control (AGC) circuit. The IC provides module designers with scalable supplies for optimizing power dissipation vs. required linearity. The IC is in a 2.9 mm × 2.9 mm leadless chip carrier (LCC) package and requires an external bias tee. The differential input and differential are externally ac-coupled. No power supply sequencing is required.

Rev. A
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support
www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

6/2018—Rev. 0 to Rev. A

Changes to Charged Device Mode (CDM) Rating, Table 3 5
Changes to Ordering Guide 14

2/2018—Revision 0: Initial Version

SPECIFICATIONS

All specifications with positive supply voltage (V_{DD}) = 3.3 V, positive and negative external supply voltage (V_{DD_EXTP}/V_{DD_EXTN}) = 2.5 V or 3.3 V, T_{MIN} to T_{MAX}, typical values are specified at T_A = 25°C at maximum data rate, unless otherwise stated.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM DATA RATE			28.3	32.0	Gbps	Nonreturn to zero (NRZ), pseudorandom binary sequence (PRBS31) = $2^{31} - 1$
BANDWIDTH						
High			28		GHz	
Low Cutoff			1		MHz	
VOLTAGE RANGE						
Differential						
Input		0.2		1.0	V	With adjusted control voltage (V_{CTL}); for differential input voltage levels higher than 550 mV p-p, adjust V_{CTL} to keep the driver in linear operation
Output			4.4		V	Measured with PRBS31 and differential input of 600 mV p-p and V_{CTL} = −1.5 V
Single-Ended			2.2		V	Measured with PRBS31 and differential input of 600 mV p-p and V_{CTL} = −1.5 V
SMALL SIGNAL GAIN						
Differential to Differential		4	17	18	dB	Adjustable through V_{CTL} control voltage, 1 MHz to 28 GHz, maximum gain: V_{CTL} = −1.5 V, minimum gain: V_{CTL} = 0 V
Differential to Single-Ended		2	11	12	dB	1 MHz to 28 GHz
GAIN FLATNESS			±1		dB	1 MHz to 20 GHz, −1.5 V < V_{CTL} < 0 V
RETURN LOSS						
Input						
Differential			15		dB	100 MHz to 20 GHz, V_{CTL} = −1.15 V
			10		dB	V_{CTL} = −1.5 V
Single-Ended			15		dB	100 MHz to 10 GHz, V_{CTL} = −1.15 V
			10		dB	V_{CTL} = −1.5 V
Single-Ended Output			15		dB	100 MHz to 10 GHz
			10		dB	10 GHz to 30 GHz
SIGNAL-TO-NOISE RATIO (SNR)			22		dB	Input voltage (V_{IN}) = 560 mV p-p, V_{CTL} = −1.5 V
TOTAL POWER CONSUMPTION						V_{DD} = 3.3 V
			0.44		W	V_{DD_EXTP}, V_{DD_EXTN} = 2.5 V
			0.5		W	V_{DD_EXTP}, V_{DD_EXTN} = 3.3 V
TOTAL HARMONIC DISTORTION (THD)						At 1 GHz
			2		%	At 3 V p-p
			3		%	At 4 V p-p
VC PIN VOLTAGE	V_{VC}	0	0.5	1.5	V	
VCTL PIN VOLTAGE	V_{VCTL}	−1.5		0	V	
CONTROL SOURCE CURRENT						
I_{VC}				2	mA	
I_{VCTL}				1	mA	
COMMON-MODE REJECTION RATIO		25			dB	
SUPPLY VOLTAGE TOLERANCE						
		−8		+5	%	V_{DD} = 3.3 V
		−8		+5	%	V_{DD_EXTP}/V_{DD_EXTN} = 3.3 V
		−5		+5	%	V_{DD_EXTP}/V_{DD_EXTN} = 2.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RESISTANCE						
Input						
Differential			100		Ω	
Single-Ended			50		Ω	
Output						
Differential			100		Ω	
Single-Ended			50		Ω	

TIMING SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
GROUP DELAY VARIATION		±7.5		ps	1 GHz to 30 GHz
OUTPUT					
Rise Time		13		ps	20% to ~ 80%
Fall Time		13		ps	20% to ~ 80%
Jitter					V_{CTL} = −1.5 V
Additive RMS		350		fs	V_{DD_EXTP}, V_{DD_EXTN} = 2.5 V
		400		fs	V_{DD_EXTP}, V_{DD_EXTN} = 3.3 V
Deterministic		3		ps	V_{DD_EXTP}, V_{DD_EXTN} = 3.3 V and 2.5 V

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Positive VDD Supply to GND	12 V
INN and INP to GND	2 V
OUTP to GND	12 V
VC to GND	2.5 V
VCTL to GND	−2.5 V to +0.5 V
Electrostatic Discharge (ESD) Protection	
Human Body Model (HBM)	Class 1A, 250 V_{RF}, 500 V_{DC}
Charged Device Mode (CDM)	Class III, 250 V_{RF}, 500 V_{DC}
Maximum Reflow Temperature	
Moisture Sensitivity Level 3 (MSL3)	260°C
Operating Temperature Range	−40°C to +130°C
Maximum Junction Temperature (T_J)	175°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 4. Thermal Resistance

Package Type[1]	θ_{JA}[2]	θ_{JC}[3]	Unit
E-16-1	53	51	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with nine thermal vias.
[2] θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.
[3] θ_{JC} is the junction to case thermal resistance.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

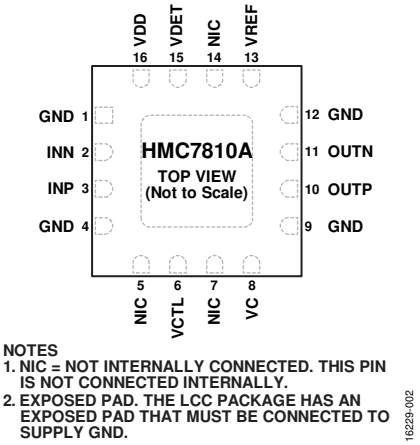


Figure 2. Pin Configuration

Table 5. Pin Function and Descriptions

Pin No.	Mnemonic	Description
1, 4, 9, 12	GND	Supply GND.
2	INN	Data Negative Differential Input.
3	INP	Data Positive Differential Input.
5, 7, 14	NIC	Not Internally Connected. This pin is not connected internally.
6	VCTL	Analog Attenuator Control Voltage.
8	VC	Amplitude Control Voltage.
10	OUTP	Positive Differential Output.
11	OUTN	Negative Differential Output.
13	VREF	Reference Voltage for Detector.
15	VDET	Detector Voltage Output.
16	VDD	Supply Voltage.
	EPAD	Exposed Pad. The LCC package has an exposed pad that must be connected to supply GND.

TYPICAL PERFORMANCE CHARACTERISTICS

Time domain properties, typical 32 Gbps NRZ output eye diagram, measured with PRBS31 pattern and 600 mV p-p differential input.

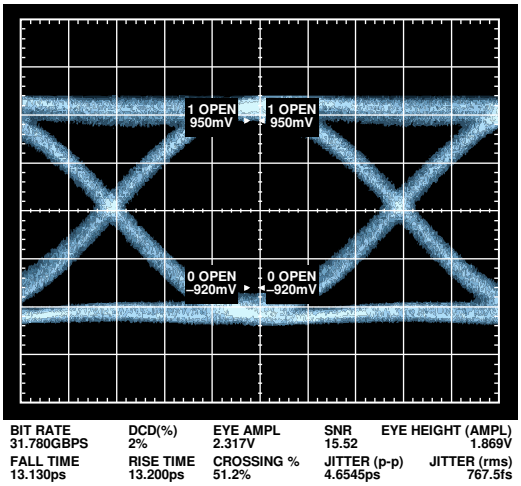


Figure 3. Single-Ended Output, 2.3 V p-p Swing

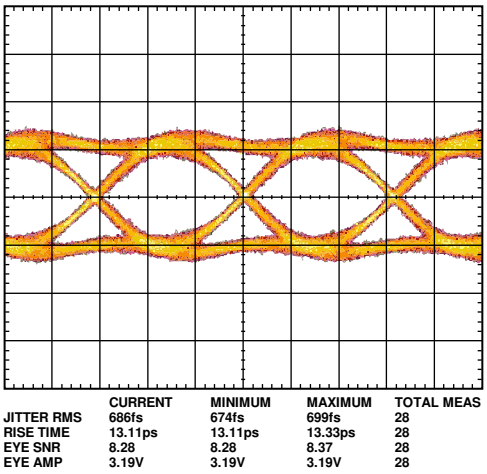


Figure 6. Differential Output, V_{CTL} = –1 V

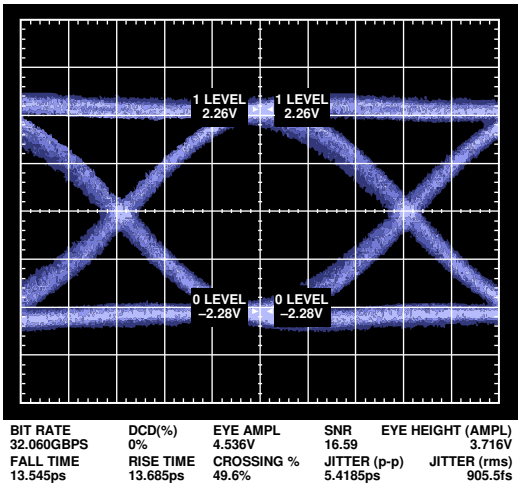


Figure 4. Differential Output, 4.5 V p-p Swing

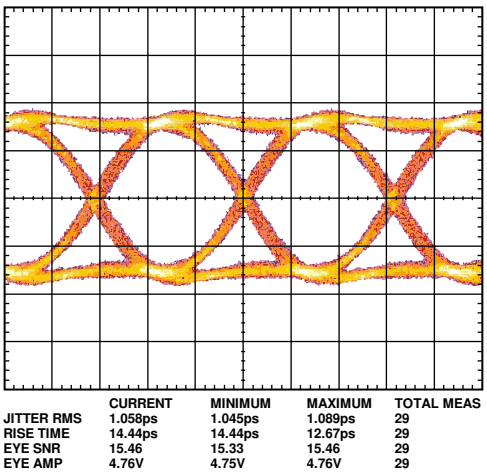


Figure 7. Differential Output, V_{CTL} = –1.5 V

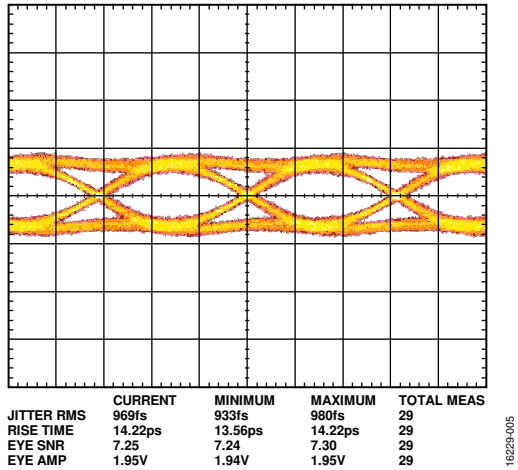


Figure 5. Differential Output, V_{CTL} = 0 V

FREQUENCY DOMAIN PROPERTIES

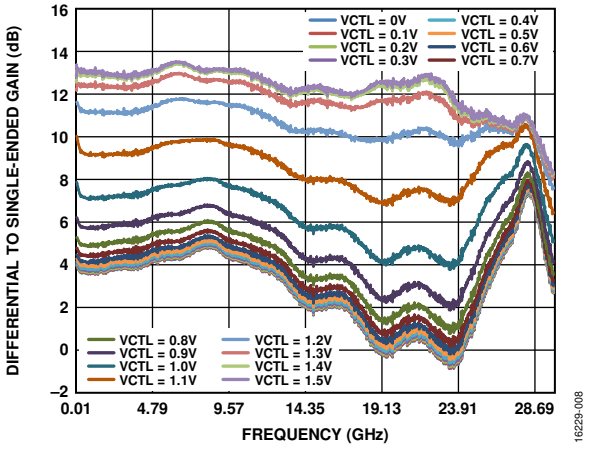


Figure 8. Differential to Single-Ended Gain (S21) vs. Frequency with Respect to the VCTL Pin, Measurement Taken with EV1HMC7810ALC3 Evaluation Board (Fixture Not De-Embedded)

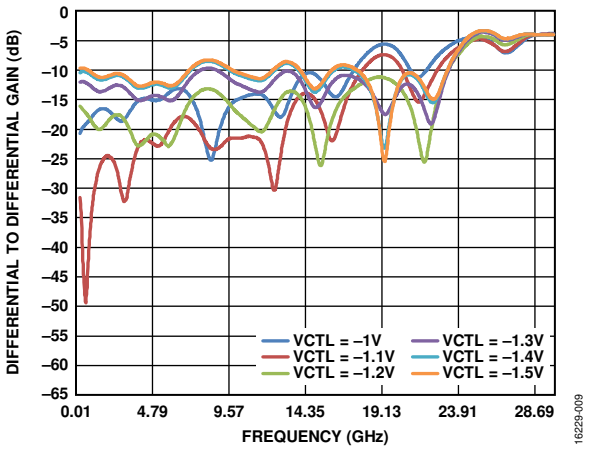


Figure 9. Differential to Differential Gain (S11) vs. Frequency with Respect to the VCTL Pin, Measurement Taken with EV1HMC7810ALC3 Evaluation Board (Fixture De-Embedded)

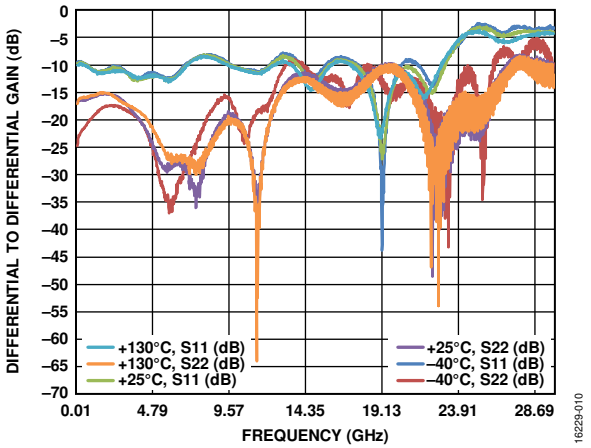


Figure 10. Differential to Differential Gain (S11, S22) vs. Frequency, VCTL Pin = –1.5 V, Zoomed for Gain Flatness (Fixture De-Embedded)

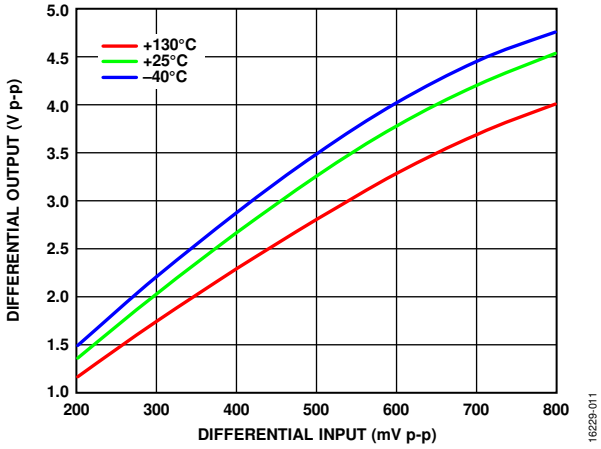


Figure 11. Differential Output vs. Differential Input, Measured at 1 GHz Sine Wave

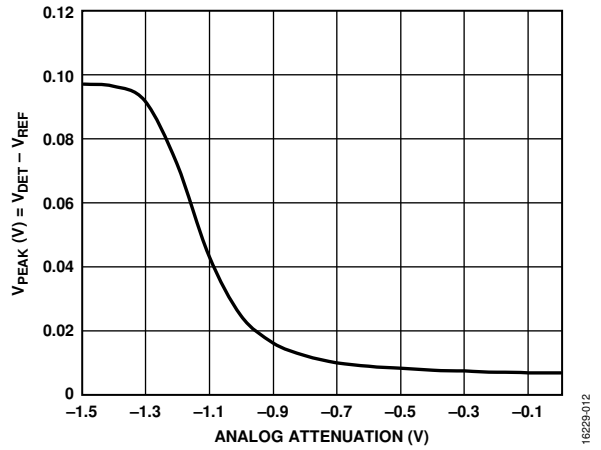


Figure 12. Peak Voltage (V_{PEAK}) = Detector Output Voltage (V_{DET}) – Reference Voltage (V_{REF}) vs. Analog Attenuation

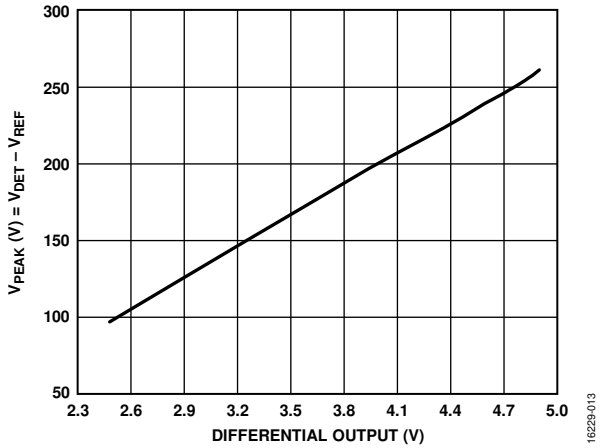


Figure 13. $V_{PEAK} = V_{DET} – V_{REF}$ vs. Differential Output

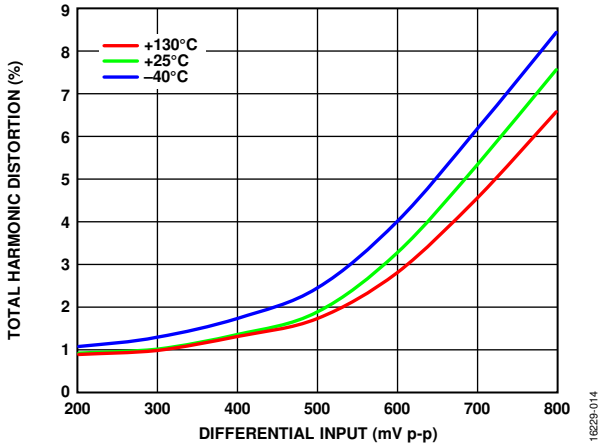


Figure 14. Total Harmonic Distortion (THD) vs. Differential Input

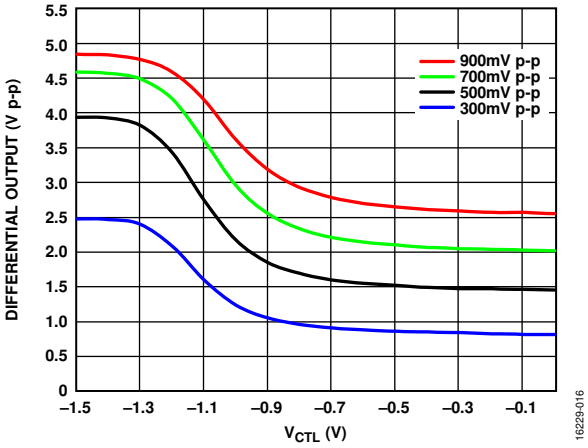


Figure 16. Differential Output vs. V_{CTL}, Voltage Measured at Various Differential Input Voltages, 32 Gbps PRBS31 Data at the Input

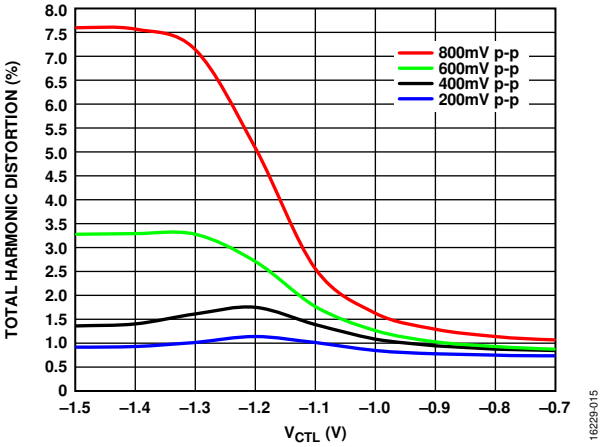


Figure 15. Total Harmonic Distortion vs. V_{CTL}, Voltage Measured at Various Differential Input Voltages

THEORY OF OPERATION

The HMC7810A is a broadband linear amplifier with a differential input and output. The device supports a maximum data rate of 32.0 Gbps with a typical bandwidth of 28 GHz. The HMC7810A is self biased and does not requires any bias sequencing or current adjustment circuitry. The device has two external supply voltages: V_{DD} = 3.3 V supply at the supply pin and V_{DD_EXTP}/V_{DD_EXTN}. The V_{DD_EXTP}/V_{DD_EXTN} supply has two options: 2.5 V, which achieves better jitter performance, and 3.3 V, which achieves higher output voltage swings.

The HMC7810A includes an integrated analog that allows a gain adjustment of at least 6 dB. When V_{CTL} is −1.5 V, the gain is maximum, and when V_{CTL} is 0 V, the gain is minimum. The HMC7810A contains a peak detector that behaves linearly with respect to the output swing. The peak detector has two outputs, VDET and VREF. Use the difference of these voltages to read the output voltage swing. To implement an external automatic gain control, use an analog attenuator and the features of the peak detector.

APPLICATIONS INFORMATION

The HMC7810A can drive Mach-Zehnder modulators in differential or single-ended operation. To keep the output swing constant at a desired value, build an analog or digital gain control loop. To build a gain control loop, use the voltage difference of the VREF and VDET pins (V_{PEAK}) as an input to an analog or digital gain control mechanism to drive the VCTL pin (see Figure 17). The HMC7810A requires an external bias from the output side; however, the modulator bias can be provided after a dc blocking capacitance.

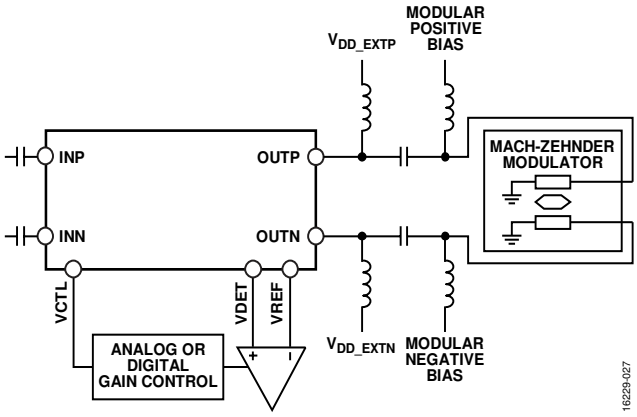


Figure 17. Analog or Digital Gain Control Loop

REFLOW SOLDER PROFILE

Figure 18 shows the typical, Pb-free reflow solder profile.

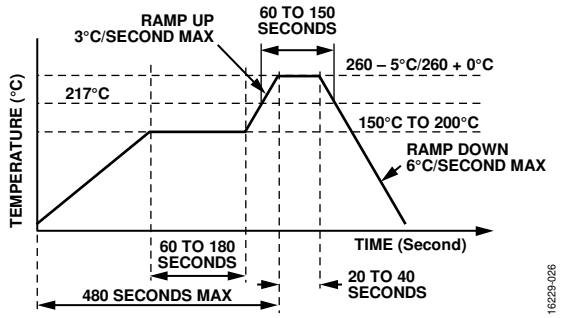


Figure 18. Typical Pb-Free Reflow Solder Profile

EVALUATION BOARD

EVALUATION BOARD SCHEMATIC

Figure 19 shows the schematic for the EV1HMC7810ALC3 evaluation board. Table 6 lists the bill of materials.

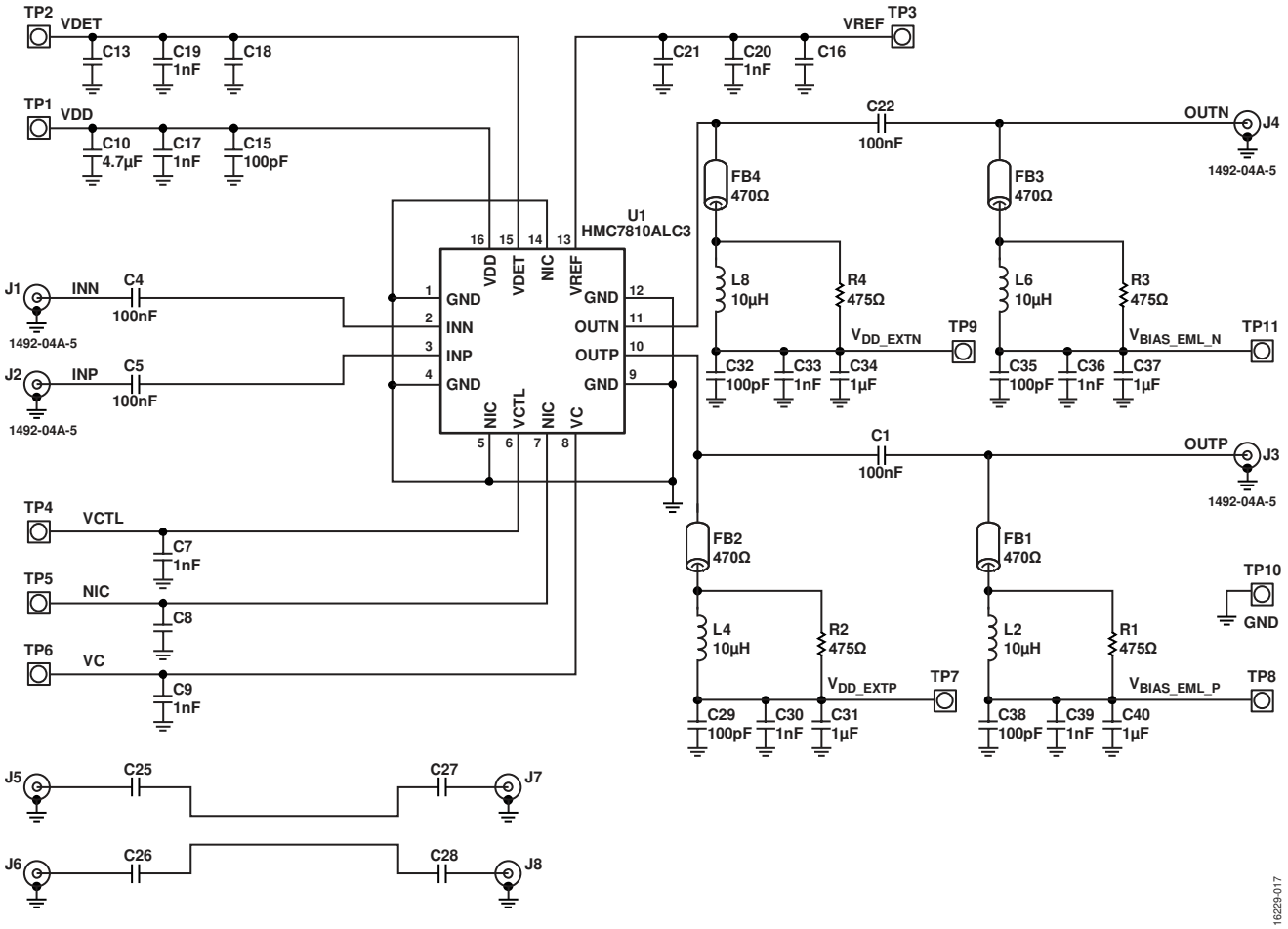


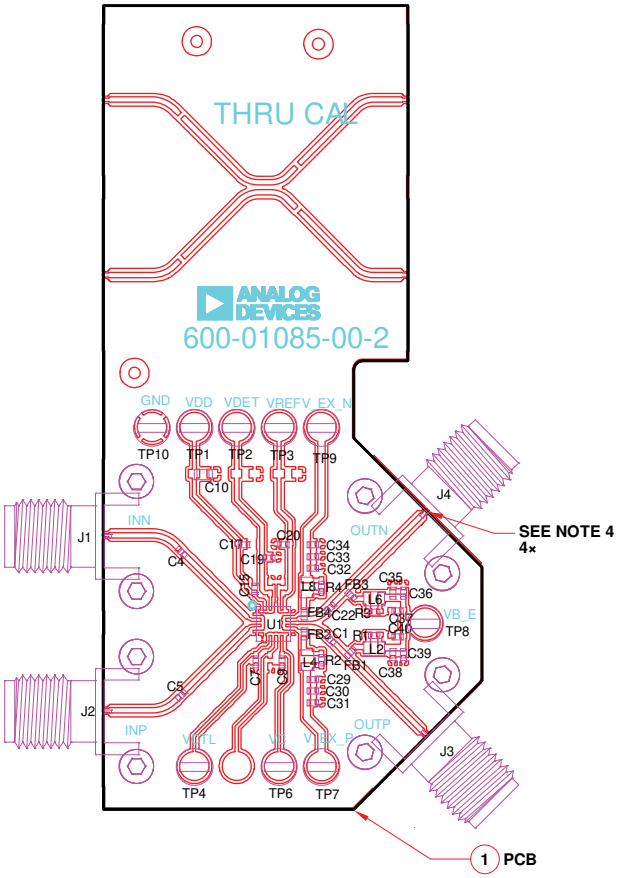
Figure 19. Evaluation Board Schematic

Table 6. Bill of Materials

Qty.	Reference Designator	Description	Manufacturer/Part Number
1	EV1HMC7810ALC3	Evaluation board	Analog Devices, Inc./EV1HMC7810ALC3
4	C1, C4, C5, C22	100 nF, 16 V, tin, ultra broadband capacitor	American Technical Ceramics/ATC550L101KT16T
5	C7, C9, C17, C19, C20, C30, C33, C36, C39	1 nF, 50 V, X7R, 0402, ceramic capacitor	Murata/GRM15555C1H101J
9	C8, C13, C16, C18, C21, C25 to C28	Do not populate	Not applicable
1	C10	4.7 µF, 25 V, 10%, X7R, 0603, gold terminal ceramic capacitors	Capax Technologies, Inc./0603X475K250GW
5	C15, C29, C32, C35, C38	100 pF, 50 V, 5%, C0G, 0402, ceramic capacitors	Murata/GRM155R71H102KA01D
4	C31, C34, C37, C40	1 µF, 16 V, 10%, X5R, 0402, ceramic capacitors	Taiyo Yuden/EMK105BJ105KV-F
4	FB1 to FB4	Ferrite chips, 470 Ω, 200 mA, 0402	Murata/BLM15GG471SN1D
4	J1 to J4	Connectors, K connector	SRI Connector Gage Co./25-146-1000-92
3	J5 to J8	Do not populate	
4	L2, L4, L6, L8	Inductors, 10 µH, 0603, 5%, 0.18 A	Coilcraft/0603LS-103XJLB
4	R1 to R4	475 Ω, 1/10 W, 1%, 0402, resistors, SMD	Panasonic/ERJ-2RKF470X

Qty.	Reference Designator	Description	Manufacturer/Part Number
8	TP1 to TP4, TP6 to TP9	Test point, PC compact, 0.063 inch, red	Keystone Electronics/5005
1	TP5	Do not populate	
1	TP10	Test point, PC, compact, 0.063 inch, black	Keystone Electronics/5006
1	U1	Optical modulator driver with internal attenuator and power detector	Analog Devices/HMC7810ALC3

EVALUATION PCB OUTLINE



NOTES
1. SOLDER QUALITY TO IPC-A-610 CLASS 2.
2. MANUALLY DISPENSE SOLDER (ITEM 5) FOR ALL COMPONENTS.
3. J1 TO J4, ATTACH TO PCB WITH CENTER PIN ON TOP SIDE TRACE. MANUALLY DISPENSE SOLDER (ITEM 5) TO CENTER PIN AND GROUND LEADS, TOP AND BOTTOM. AFTER REFLOW, SOLDER MUST JOIN CONNECTOR AND PCB EDGE.
4. TRIM EDGE PLATING WITH ITEM 6 (106356).

Figure 20. Evaluation Board PCB

OUTLINE DIMENSIONS

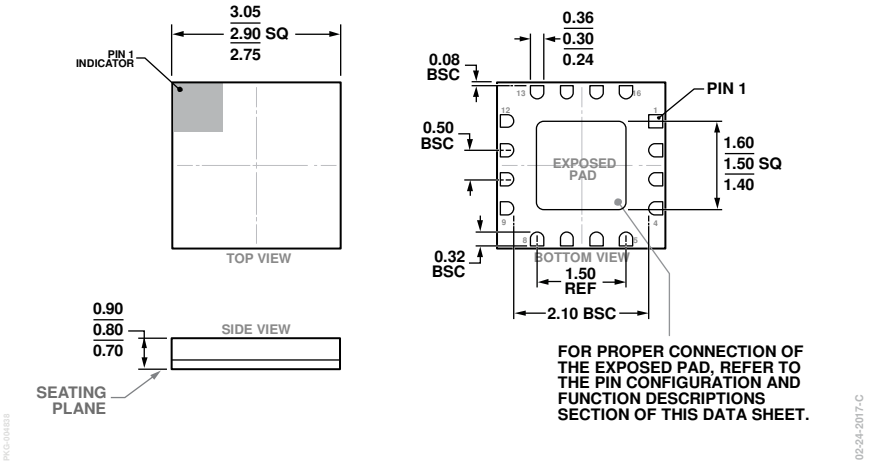


Figure 21. 16-Terminal Leadless Ceramic Chip Package [LCC]
(E-16-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Lead Finish	Package Option
HMC7810ALC3	–40°C to +130°C	16-Terminal Leadless Ceramic Chip Carrier [LCC]	Nickel/gold (NiAu)	E-16-1
HMC7810ALC3TR	–40°C to +130°C	16-Terminal Leadless Ceramic Chip Carrier [LCC]	NiAu	E-16-1
EV1HMC7810ALC3		Evaluation Board with Bias Tee and AC-Coupled Input/Output Capacitors		

[1] All models are RoHS compliant parts.