National Semiconductor

PRELIMINARY
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DS3875 Futurebus+ Arbitration Controller MIL-STD-883

General Description

(For a complete description of operation, please refer to the commercial datasheet.)

The DS3875 Futurebus+ Arbitration Controller is a member of National Semiconductor's Futurebus+ chip set designed specifically for the IEEE 896.1 Futurebus+ standard. The DS3875 implements Distributed Arbitration and Distributed Arbitration messages in a single chip.

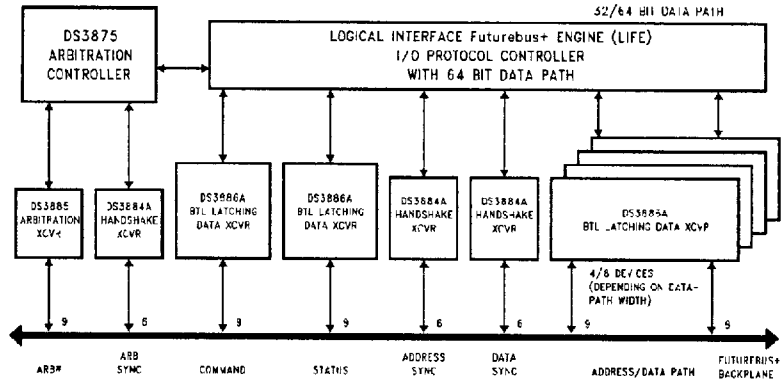
The DS3875 interfaces with Futurebus+ through the DS3885 BTL Arbitration Transceiver and the DS3884A BTL Handshake Transceiver. The DS3885 BTL Arbitration Transceiver incorporates the competition logic needed for the Arbitration Number signal lines. The DS3884A BTL Handshake Transceiver has selectable Wired-OR receiver glitch filtering. The DS3884A is used for the Arbitration Sequencing and Arbitration Condition signal lines.

Additional transceiver included in the military Futurebus+ chip set is the DS3886A BTL 9-bit Latching Data Transceiver. The DS3886A transceiver features edge-triggered latches in the driver which may be bypassed during a fall-through mode and a transparent latch in the receiver.

The Logical Interface Futurebus+ Engine (LIFE) I/O Protocol Controller with 64-bit Data Path incorporates the Compelled Mode Futurebus+ Parallel Protocol. The Protocol Controller handles all the handshaking signals between the Futurebus+ and the local bus interfaces, and incorporates a DMA Controller with built-in FIFOs for fast queueing.

Features

- The controller implements the complete requirements of the IEEE 896.1 specification as a subset of its features
- Supports Arbitration message sending and receiving
- Supports the two modes of operation (RESTRICTED/UNRESTRICTED)
- Software configurable double/single pass operation, slow/fast, IBA/Parking and restricted/unrestricted modes of arbitration
- Built-in 1 μs timer for use in the arbitration cycle
- User programmable 16 arbitration delays (8 slow and 8 fast)
- Built-in PLL for accurate delays. The PLL accepts clocks from 2 MHz to 40 MHz in steps of 1 MHz
- Signal to unlock slave modules on transfer of tenure. Auto unlock through a dummy cycle if the current master locked resources
- Programmable delay for releasing ar* after issuing COMPETE/IBA_CMPT. This is to ensure the assertion of the arbitration number during competition, before the release of ar*. Also this delay ensures there is sufficient time to assert the AD/DATA lines during Idle Bus Arbitration before the release of ar*
- Read/Write facility with data acknowledge for the host to load arbitration numbers, an arbitration message, and control registers
- On chip parity generator unloads the host of the additional parity generation function
- Separate interrupts to indicate error occurrence and arbitration message received. Interrupts cleared on a register write. Error status is available in a separate status register
- A special output pin to indicate that a POWERFAIL message was received
- Hardwired register to hold the first word of the arbitration message
- FIFO strobe provided to store more than one arbitration message externally to prevent overrun
- Idle Bus Arbitration (IBA) supported
- Parking implemented
- Bus initialization, system reset and Live-insertion supported. (The logic to detect these conditions must be implemented externally.)
- Testability in the form of reading from key registers which include the STATE, MCW, 1 μs timer and programmable input clock divider
- 68-pin CQD Package



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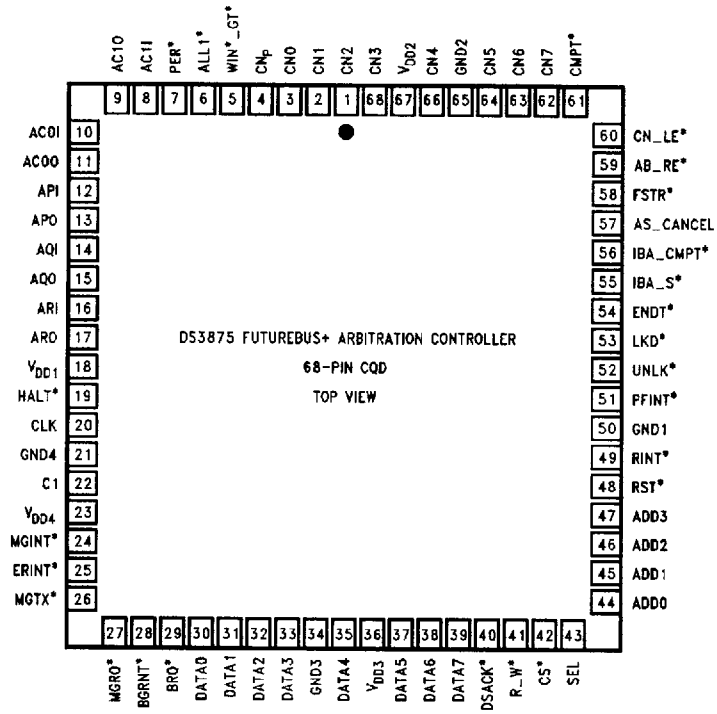
National's Futurebus+ Chip Set Diagram

RRD B30M105/Printed in U. S. A.



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Pin Definition

Pin	# of Pins	Type	Description
SIGNAL TO/FROM THE HANDSHAKE TRANSCEIVER			
APO	1	O	Arbitration handshake signal from the controller.
AQO	1	O	Arbitration handshake signal from the controller.
ARO	1	O	Arbitration handshake signal from the controller.
AC0O	1	O	Arbitration condition signal from the controller.
AC1O	1	O	Arbitration condition signal from the controller.
API	1	I	Arbitration handshake signal from Futurebus+. This signal is the filtered and inverted version of the Futurebus+ backplane signal AP*.
AQI	1	I	Arbitration handshake signal from Futurebus+. This signal is the filtered and inverted version of the Futurebus+ backplane signal AQ*.
ARI	1	I	Arbitration handshake signal from Futurebus+. This signal is the filtered and inverted version of the Futurebus+ backplane signal AR*.
AC0I	1	I	Arbitration condition signal from Futurebus+.
AC1I	1	I	Arbitration condition signal from Futurebus+.
SIGNAL TO/FROM THE ARBITRATION TRANSCEIVER (Note: These pins are mapped to/from the DS3885 Futurebus+ Arbitration Transceiver.)			
CN(7:0)	8	I/O	The bus to carry competition number to/from the arbitration transceiver.
CNp	1	O	Parity bit of the competition number.
CMPT*	1	O	Enables the Arbitration number onto Futurebus+.
AB_RE*	1	O	Direction control for the competition number bus to/from the transceiver.
CN_LE*	1	O	Latch enable for latching the Arbitration number from the controller into the transceiver.
PER*	1	I	**PARITY ERROR:** Indicates that a parity error was detected on the winner's arbitration number.
WIN*_GT*	1	I	Win signal when competing/greater than signal when not competing (used to preempt).
ALL1*	1	I	Indicates that all the arbitration number lines on the bus are asserted (used for messages).
SIGNALS TO/FROM THE PARALLEL PROTOCOL CONTROLLER			
BRQ*	1	I	**BUS REQUEST:** Indicates to the controller to acquire the bus for the module's use.
BGRNT*	1	O	**BUS GRANT:** Signal asserted by the controller after the detection of a bus request. The module can start using the bus.
RINT*	1	I	Will put the arbitration controller in phase 0 and release all the bus lines except AR*. A selective reset is performed. The rising edge will release controller from phase 0. This reset is to be used for bus initialization.
RST*	1	I	Reset signal from the host. An internal reset is performed. All bus signals are released. The rising edge will put the controller in phase 0 (same as power-up reset).
HALT*	1	I	Will halt the arbitration controller in phase 0. This signal is for use during live insertion.
ENDT*	1	I	**END OF TENURE:** Indicates the true end of bus tenure of the current master. This line may be asserted only after all the parallel protocol lines are released. (Generated via external logic from BRQ* released.)

Pin Definition (Continued)

Pin	# of Pins	Type	Description
SIGNALS TO/FROM THE HOST (CPU Plus External Interface Logic)			
DATA(7:0)	8	I/O	Data bus for the host to access the register bank of the controller.
ADD(3:0)	4	I	Address bits for the register bank of the controller.
CS*	1	I	**CHIP SELECT:** The host can read or write to/from the controller.
R_W*	1	I	Read/write signal from the host.
DSACK*	1	O	Data acknowledge pin for host read/write.
SEL	1	I	**SELECT:** Determines how the controller latches in data. A "1" on the pin uses the rising edge of CS*. A "0" on the pin uses the falling edge of DSACK*.
MGRQ*	1	I	**MESSAGE REQUEST:** Indicates to the controller to send an arbitration message.
MGTX*	1	O	**MESSAGE TRANSMIT:** Indicates the successful transmission of an arbitration message.
ERINT*	1	O	**ERROR INTERRUPT:** Indicates that an error occurred during the arbitration cycle.
MGINT*	1	O	**MESSAGE INTERRUPT:** Indicates the reception of an arbitration message.
PFINT*	1	O	**POWER FAIL INTERRUPT:** Indicates that a powerfail message was received.
EXTERNAL LOGIC			
IBA_CMPT*	1	O	Signal to indicate that the Parallel Protocol controller may assert its bit on the ADDRESS/DATA bus if it is participating in an Idle Bus Arbitration.
IBA_S*	1	I	This signal indicates that IBA was successful. If this module was a competitor in the IBA competition (!BRQ*), then this module is the winner and now the bus master. If this module was the master, but did not compete in the IBA competition and IBA was successful, then the M bit (Status register) is negated.
AS_CANCEL	1	I	Indicates the start of the disconnection phase of the current master or cancel the current arbitration cycle.
LKD*	1	I	**LOCKED:** Signal to indicate that resources have been locked in the current tenure and hence generate either a dummy cycle if current master or UNLK* otherwise. (Decoded from Futurebus + Command port output from Data Path Unit.)
UNLK*	1	O	**UNLOCK:** Transfer of tenure indication to the parallel protocol controller for unlocking its resources. Generated only if the LKD* signal is asserted. (To external logic.)
FSTR*	1	O	**FIFO STROBE:** Signal generated to load an external FIFO for received arbitration messages.
CLK	1	I	Clock input to the internal PLL.
C1	1	I	External capacitor input for PLL—0.1 μF.

Electrical Characteristics

Absolute Maximum Ratings

The 883 specifications are written to reflect the Reliability Electrical Test Specifications (RETS) established by National Semiconductor for this product. For a copy of the RETS, please contact your local National Semiconductor sales office or distributor.

Supply Voltage	6.5V
Control Input Voltage	5.5V
Power Dissipation at 125°C	1.3W
Storage Temperature Range	−65°C to +150°C
Lead Temperature	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{DD}	4.5	5.5	V
Operating Free Air Temperature	−55	+125	°C

Electrical Characteristics (Notes 2 and 3) $T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	Minimum Input High Voltage		2.8		V
V_{IL}	Minimum Input Low Voltage			0.75	V
V_{OH}	Voltage Output High	I_{OH}, I_{OL} for Several Drivers i.e., I_{OL} 4 mA	2.4		V
V_{OL}	Voltage Output Low	I_{OH}, I_{OL} for Several Drivers i.e., I_{OL} 8 mA		0.7	V
I_I	Input Leakage Current	Input at V_{DD} or V_{SS}	−3	3	μA
I_{DD}	Supply Current	Dynamic Supply Current		100	mA
I_{CC}	Static Supply Current	Input at Standby		30	mA

Note 1: "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pin are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for $V_{DD} = 5V$, and $T_A = 25°C$.

AC Parameters

Legend to AC Parameter Number Assignments

Parameter Number	Description
t000–t099	Phase 0
t100–t199	Phase 1
t200–t299	Phase 2
t300–t399	Phase 3
t400–t499	Phase 4
t500–t599	Phase 5
tAXX	Reset, Initialization
tBXX	Register Access Data Port
tCXX	Register Access CN Port - Input
tDXX	Clearing Interrupts
tEXX	FIFO Strobe
tFXX	WIN*_GT* Valid
tGXX	Message Signals
tHXX	Busrequest, Busgrant, End of Tenure
tJXX	Locked, Unlock Handshake Signals

AC Parameters (Continued)

AC Timing Parameters Unless otherwise stated: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$

All transitions are specified after the input signals are stable and valid for evaluation. This table will describe the parameters as given in the following pages. All values are given in nanoseconds (ns), unless otherwise stated.

Number	Symbol	Parameter Description	Min	Max
t_1	t_{BQBG}	BRQ* Asserted to BGRNT* Asserted		36
t_2	t_{AQAC}	AQI Negated to AC0O, AC1O Negated		30
t_3	t_{APIO}	API Asserted to APO Asserted		31
t_4	t_{RQAP}	MGRQ* or BRQ* Asserted to APO Asserted		38
t_5	t_{EDAP}	(Dummy Cycle) ENDT* Asserted to APO Asserted		46
t_6	t_{BQAP}	(Consecutive Bus Requests) BRQ* Asserted to APO Asserted		34
t_7	t_{HTAP}	HALT* Negated to APO Asserted		28
t_{100}	$t_{CNLEAR}+(0-25)$	CN__LE* Negated to ARO Negated. Determined by Programmable Value		$4+(0-25)$
t_{101}	t_{CNLE}	CN__LE* Width	18	28
t_{102}	t_{CNS}	CN Port Setup Time	23	
t_{103}	t_{CNZ}	ARI Negated to TRI-STATE CN Port	16	
t_{104}	t_{IBCAR}	(IBA Mode) IBA-CMPT* Asserted to ARO Negated. Determined by Programmable Value	$20+(0-25)$	
t_{105}	t_{CPTAR}	CMPT* Asserted to ARO Negated. Determined by Programmable Value	$20+(0-25)$	
t_{106}	t_{AC0AR}	(Slow Mode) AC0O Asserted to ARO Negated. Determined by Programmable Value	$18+(0-25)$	
t_{107}	t_{APCNLE}	APO Asserted to CN-LE* Asserted. CTRL3[0], "G0" Bit is Set		32
t_{108}	t_{APCPTA}	APO Asserted to CMPT* Asserted		24
t_{109}	t_{APIBC}	APO Asserted to IBA__CMPT* Asserted		22
t_{110}	t_{APAC}	APO Asserted to AC0O Asserted (Slow Mode)		32
t_{200}	t_{ARABRD}	ARI Negated to AB__RE* Asserted		62
t_{202}	t_{IBSBG}	(IBA Mode) IBA__S* Asserted to BGRNT* Asserted		40
t_{203}	t_{WINAQ}	WIN*__GT* Asserted to AQO Asserted. After T_A Expired.		35
t_{204}	t_{AQIO}	AQI Asserted to AQO Asserted		24
t_{205}	t_{ARAQ}	ARI Negated to AQO Asserted		$30+T_A$
t_{207}	t_{IBSAQ}	(IBA Mode) IBA-S* Asserted to AQO Asserted		35
t_{300}	t_{AC10AP}	AC10 Asserted to APO Negated		29
t_{301}	t_{ASNAP}	AS__Cancel* Negated to APO Negated		27
t_{310}	t_{APABRD}	APO Negated to AB__RE* Negated		10
t_{320}	t_{AQAC1}	AQO Asserted to AC1O Asserted		13
t_{321}	$t_{AC1IAPN}$	AC1I Asserted to APO Negated	5	21
t_{322}	t_{ASAAP}	AS__Cancel* Asserted to APO Negated	5	21
t_{330}	t_{AC1IAP}	AC1I Asserted to APO Negated		24
t_{340}	t_{RQAC}	MGRQ* or BRQ* Negated to AC0O, AC1O Asserted		40
t_{341}	t_{AQAC0}	AQO Asserted to AC0O Negated		4
t_{342}	t_{AQER}	AQO Asserted to ERIT* Asserted		23
t_{400}	t_{APCPTN}	API Negated to CMPT* Negated		34

AC Parameters (Continued)

AC Timing Parameters Unless otherwise stated: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$ (Continued)

All transitions are specified after the input signals are stable and valid for evaluation. This table will describe the parameters as given in the following pages. All values are given in nanoseconds (ns), unless otherwise stated.

Number	Symbol	Parameter Description	Min	Max
t_{401}	t_{AC1IAR}	AC1I Asserted to ARO Asserted		26
t_{403}	t_{CANAC1}	AS__Cancel* Asserted to AC1O Asserted	7	24
t_{406}	t_{ARIO}	ARI Asserted to ARO Asserted		25
t_{407}	t_{EDAR}	ENDT* Asserted to ARO Asserted		32
t_{500}	t_{ARBG}	ARO Asserted to BGRNT* Asserted		12
t_{501}	t_{OAQ}	BGRNT*, MGTX*, UNLK* or any Interrupt Asserted to AQO Negated	3	
t_{502}	t_{ARFTR}	ARO Asserted to FSTR* Negated		10
t_{503}	t_{ARIBC}	ARO Asserted to IBA__CMPT* Negated		10
t_{504}	t_{ARABSA}	ARO Asserted to MGTX*, UNLK* or any Interrupt Asserted		10
t_{A1}	t_{RSTPW}	RST* Pulse Width	50	
t_{A2}	t_{RSTRE}	Output Reset Time		54
t_{A3}	t_{RSTAR}	RST* Negated to ARO Asserted		25
t_{A4}	t_{RINTPW}	RINT* Pulse Width	50	
t_{A5}	t_{RINTRE}	Output Initialization Reset Time		45
t_{B1}	t_{CSPW}	CS* Pulse Width	35	
t_{B2}	t_{CSPWN}	CS* Recovery Time	15	
t_{B3}	t_{CSDKA}	CS* Asserted to DSACK* Asserted		23
t_{B4}	t_{ADDS}	ADD (3:0) Setup Time	5	
t_{B5}	t_{ADDH}	ADD (3:0) Hold Time	9	
t_{B6}	t_{CSDKN}	CS* Negated to DSACK* Negated	5	
t_{B7}	t_{RWS}	R__W* Setup Time	0	
t_{B8}	t_{SELS}	SEL Setup Time	0	
t_{B10}	$t_{DATASDK}$	Data (7:0) Setup Time with Respect to DSACK*	28	
t_{B11}	$t_{DATAHDK}$	Data (7:0) Hold Time with Respect to DSACK*	0	
t_{B12}	t_{SELH}	SEL Hold Time	5	
t_{B24}	$t_{DATASCS}$	Data (7:0) Setup Time with Respect to CS* Negated	15	
t_{B25}	$t_{DATAHCS}$	Data (7:0) Hold Time with Respect to CS* Negated	5	
t_{B28}	t_{DATAV}	Data (7:0) Valid Time before DSACK*		
t_{B29}	t_{DATAA}	Data (7:0) Access Time with Respect to CS* Asserted		33
t_{C2}	$t_{ABRDCNZ}$	AB__RE* Negated to CN (7:0) TRI-STATE	0	
t_{D1}	$t_{CSXINTN}$	CS* Asserted to any Interrupt Negated		43

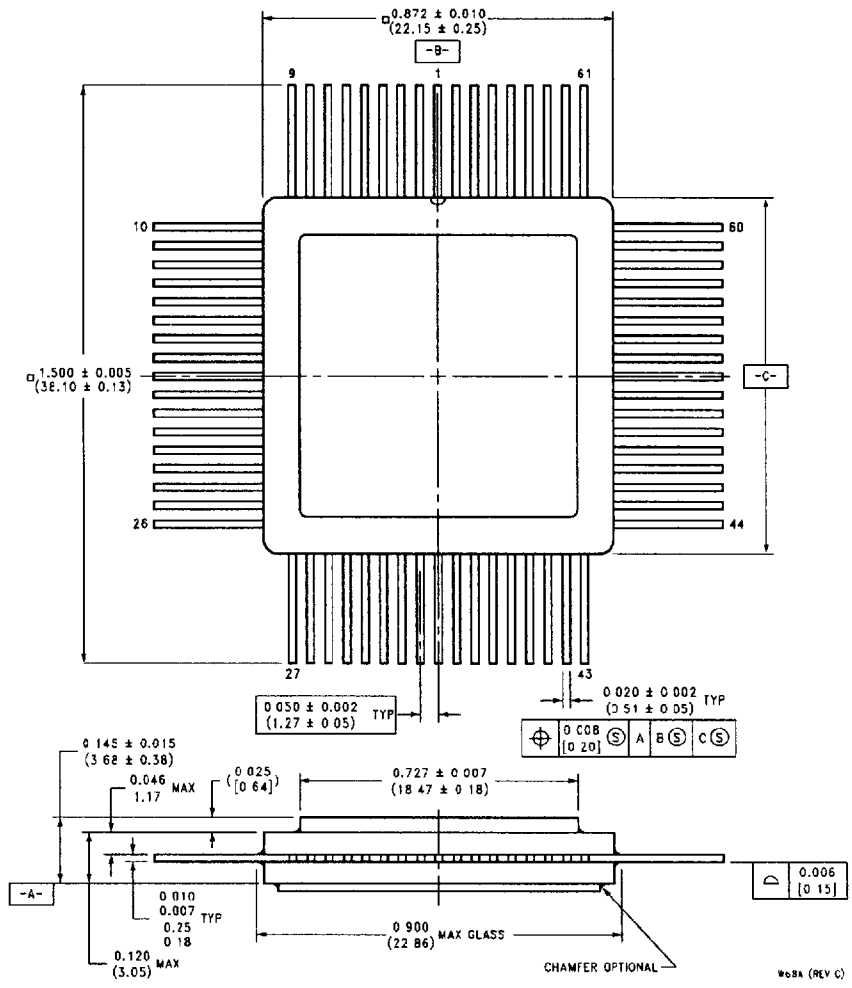
AC Parameters (Continued)

AC Timing Parameters Unless otherwise stated: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$ (Continued)

All transitions are specified after the input signals are stable and valid for evaluation. This table will describe the parameters as given in the following pages. All values are given in nanoseconds (ns), unless otherwise stated.

Number	Symbol	Parameter Description	Min	Max
t_{F1}	$t_{WINALL1}$	ALL1* Asserted with Respect to WIN*_GT*		5
t_{F2}	t_{WINPER}	PER* Asserted with Respect to WIN*_GT*		5
t_{G1}	t_{MGXN}	MGRQ* Negated to MGTX* Negated		23
t_{H2}	t_{EDBGN}	ENDT* Asserted to BGRNT* Negated		25
t_{U1}	t_{LKULKN}	LKD* Negated to UNLK* Negated		25

Physical Dimensions inches (millimeters)



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