LPV321-N Single/LPV358 Dual/LPV324 Quad General Purpose, Low Voltage, Low Power, Rail-to-Rail Output Operational Amplifiers

Check for Samples: LPV321, LPV324-N, LPV358-N

FEATURES

(For V^+ = 5V and V^- = 0V, Typical Unless Otherwise Noted)

- **Ensured 2.7V and 5V Performance**
- **No Crossover Distortion**
- **Space Saving Package**
  - **5-Pin SC70 2.0x2.1x1.0 mm**
- **Industrial Temperature Range, −40°C to +85°C**
- **Gain-Bandwidth Product, 152 kHz**
- **Low Supply Current**
  - **LPV321-N, 9 µA**
  - **LPV358, 15 µA**
  - **LPV324, 28 µA**
- **Rail-to-Rail Output Swing @ 100 kΩ Load**
  - **V^+−3.5 mV**
  - **V^-+90 mV**
- **V_{CM}, −0.2V to V^+−0.8V**

APPLICATIONS

- **Active Filters**
- **General Purpose Low Voltage Applications**
- **General Purpose Portable Devices**

DESCRIPTION

The LPV321-N/358/324 are low power (9 µA per channel at 5.0V) versions of the LMV321/358/324 op amps. This is another addition to the LMV321-N/358/324 family of commodity op amps.

The LPV321-N/358/324 are the most cost effective solutions for the applications where low voltage, low power operation, space saving and low price are needed. The LPV321-N/358/324 have rail-to-rail output swing capability and the input common-mode voltage range includes ground. They all exhibit excellent speed-power ratio, achieving 5 kHz of bandwidth with a supply current of only 9 µA.

The LPV321-N is available in space saving 5-Pin SC70, which is approximately half the size of 5-Pin SOT-23. The small package saves space on PC boards, and enables the design of small portable electronic devices. It also allows the designer to place the device closer to the signal source to reduce noise pickup and increase signal integrity.

The chips are built with Texas Instruments's advanced submicron silicon-gate BiCMOS process. The LPV321-N/358/324 have bipolar input and output stages for improved noise performance and higher output current drive.

Connection Diagram

Top View

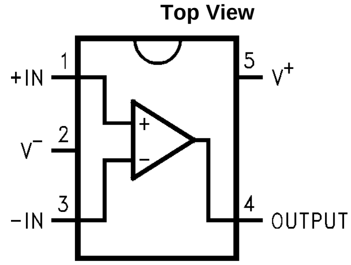


Figure 1. 5-Pin SC70 and SOT-23 Packages
See Package Numbers DCK0005A and DBV0005A

Top View

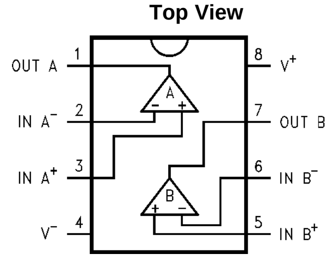


Figure 2. 8-Pin SOIC and VSSOP Packages
See Package Numbers D0008A and DGK0008A

Top View

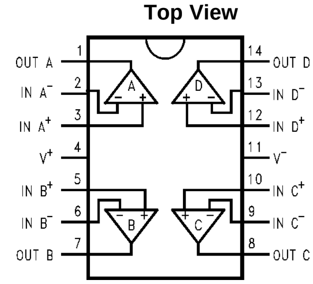


Figure 3. 14-Pin SOIC and TSSOP Packages
See Package Numbers D0014A and PW0014A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	
Human Body Model	
LPV324	2000V
LPV358	1500V
LPV321-N	1500V
Machine Model	100V
Differential Input Voltage	±Supply Voltage
Supply Voltage (V^+–V^-)	5.5V
Output Short Circuit to V^+	(4)
Output Short Circuit to V^-	(5)
Soldering Information	
Infrared or Convection (20 sec)	235°C
Storage Temperature Range	−65°C to 150°C
Junction Temp. (T_J, max) (6)	150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) Shorting output to V^+ will adversely affect reliability.
(5) Shorting output to V^- will adversely affect reliability.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings (1)

Supply Voltage	2.7V to 5V
Temperature Range	−40°C to +85°C
Thermal Resistance (θ_{JA}) (2)	
5-Pin SC70	478°C/W
5-Pin SOT-23	265°C/W
8-Pin SOIC	190°C/W
8-Pin VSSOP	235°C/W
14-Pin SOIC	145°C/W
14-Pin TSSOP	155°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) All numbers are typical, and apply for packages soldered directly onto a PC board in still air.

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = V^+/2 and R_L > 1 MΩ.

Parameter		Test Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage			1.2	7	mV
TCV_{OS}	Input Offset Voltage Average Drift			2		µV/°C
I_B	Input Bias Current			1.7	50	nA
I_{OS}	Input Offset Current			0.6	40	nA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.7V	50	70		dB
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V V_O = 1V, V_{CM} = 1V	50	65		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	0	−0.2		V
				1.9	1.7	
V_O	Output Swing	R_L = 100 kΩ to 1.35V	V^+ −100	V^+ −3		mV
				80	180	
I_S	Supply Current	LPV321-N		4	8	µA
		LPV358 Both Amplifiers		8	16	
		LPV324 All Four Amplifiers		16	24	

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = V^+/2 and R_L > 1 MΩ.

Parameter		Test Conditions	Min (1)	Typ (2)	Max (1)	Units
GBWP	Gain-Bandwidth Product	C_L = 22 pF		112		kHz
Φ_m	Phase Margin			97		Deg
G_m	Gain Margin			35		dB
e_n	Input-Referred Voltage Noise	f = 1 kHz		178		nV/√Hz
i_n	Input-Referred Current Noise	f = 1 kHz		0.50		pA/√Hz

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

5V DC Electrical Characteristics

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 2.0V, V_O = V^+/2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage			1.5	7 **10**	mV
TCV_{OS}	Input Offset Voltage Average Drift			2		µV/°C
I_B	Input Bias Current			2	50 **60**	nA
I_{OS}	Input Offset Current			0.6	40 **50**	nA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 4V	50	71		dB

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

5V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 2.0V, V_O = V^+/2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min [1]	Typ [2]	Max [1]	Units
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V V_O = 1V, V_{CM} = 1V	50	65		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	0	−0.2		V
				4.2	4	
A_V	Large Signal Voltage Gain [3]	R_L = 100 kΩ	15 **10**	100		V/mV
V_O	Output Swing	R_L = 100 kΩ to 2.5V	V^+ −100 **V^+ −200**	V^+ −3.5		mV
				90	180 **220**	
I_O	Output Short Circuit Current Sourcing	LPV324, LPV358, and LPV321-N V_O = 0V	2	16		mA
	Output Short Circuit Current Sinking	LPV321-N V_O = 5V	20	60		
		LPV324 and LPV358 V_O = 5V	11	16		
I_S	Supply Current	LPV321-N		9	12 **15**	µA
		LPV358 Both amplifiers		15	20 **24**	
		LPV324 All four amplifiers		28	42 **46**	

(3) R_L is connected to V^-. The output voltage is 0.5V ≤ V_O ≤ 4.5V.

5V AC Electrical Characteristics

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 2.0V, V_O = V^+/2 and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min [1]	Typ [2]	Min [1]	Units
SR	Slew Rate	[3]		0.1		V/µs
GBWP	Gain-Bandwidth Product	C_L = 22 pF		152		kHz
$Φ_m$	Phase Margin			87		Deg
G_m	Gain Margin			19		dB
e_n	Input-Referred Voltage Noise	f = 1 kHz,		146		nV/√Hz
i_n	Input-Referred Current Noise	f = 1 kHz		0.30		pA/√Hz

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) Connected as voltage follower with 3V step input. Number specified is the slower of the positive and negative slew rates.

Typical Performance Characteristics

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Supply Current vs. Supply Voltage (LPV321-N)

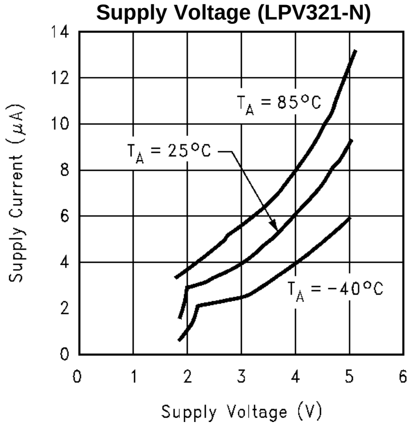


Figure 4.

Input Current vs. Temperature

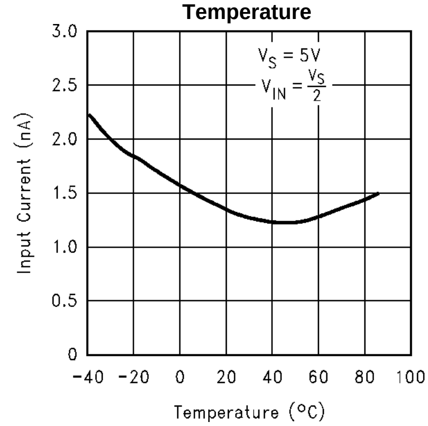


Figure 5.

Sourcing Current vs. Output Voltage

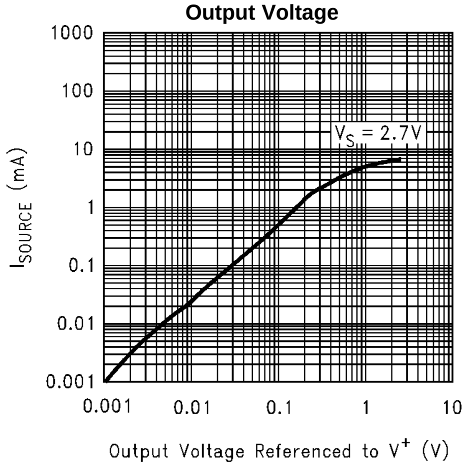


Figure 6.

Sourcing Current vs. Output Voltage

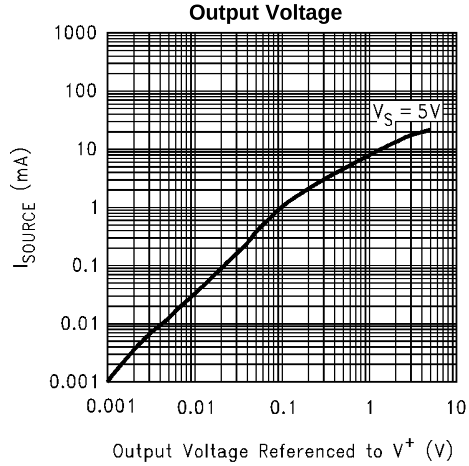


Figure 7.

Sinking Current vs. Output Voltage

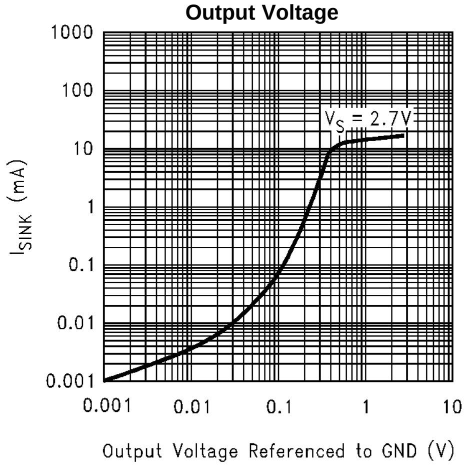


Figure 8.

Sinking Current vs. Output Voltage

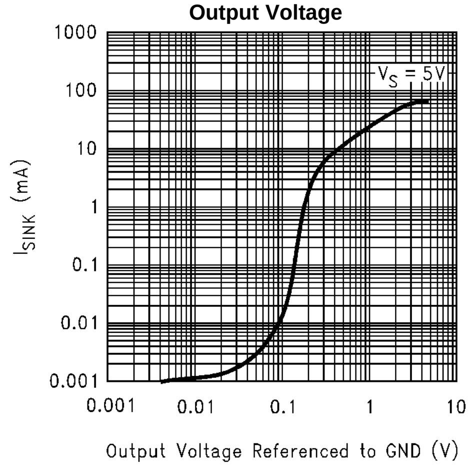


Figure 9.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Output Voltage Swing vs. Supply Voltage

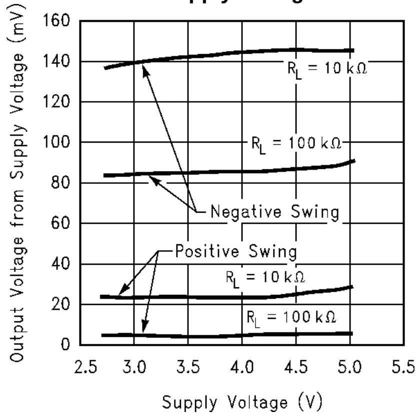


Figure 10.

Input Voltage Noise vs. Frequency

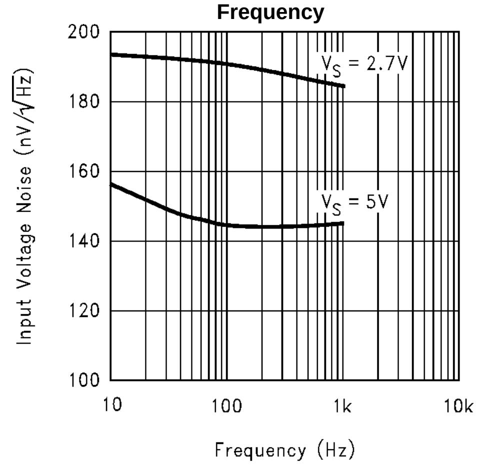


Figure 11.

Input Current Noise vs Frequency

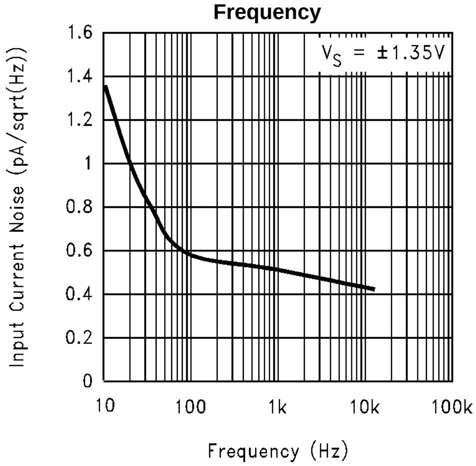


Figure 12.

Input Current Noise vs Frequency

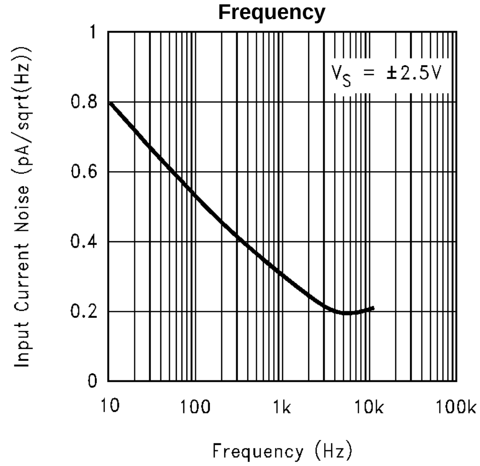


Figure 13.

Crosstalk Rejection vs. Frequency

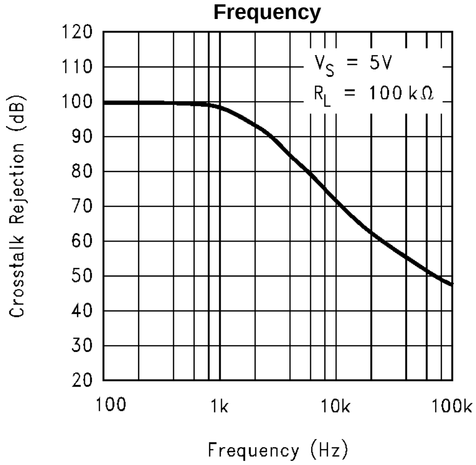


Figure 14.

PSRR vs. Frequency

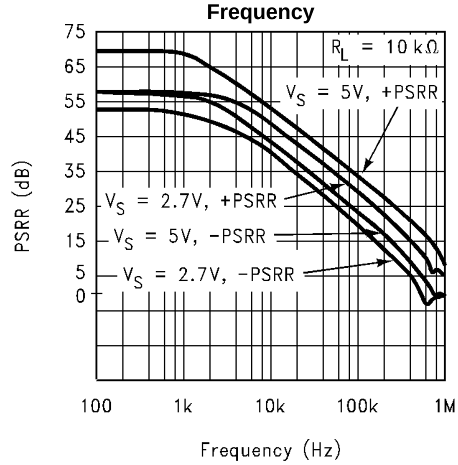


Figure 15.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

CMRR vs. Frequency

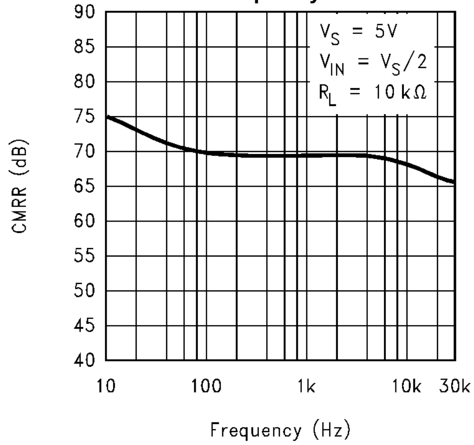


Figure 16.

CMRR vs. Input Common Mode Voltage

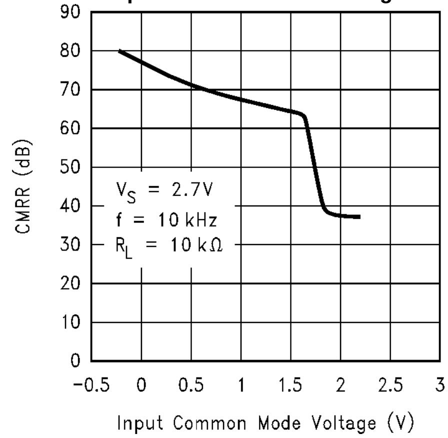


Figure 17.

CMRR vs. Input Common Mode Voltage

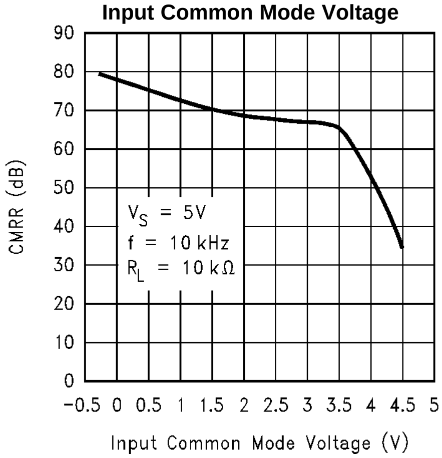


Figure 18.

ΔV_{OS} vs. V_{CM}

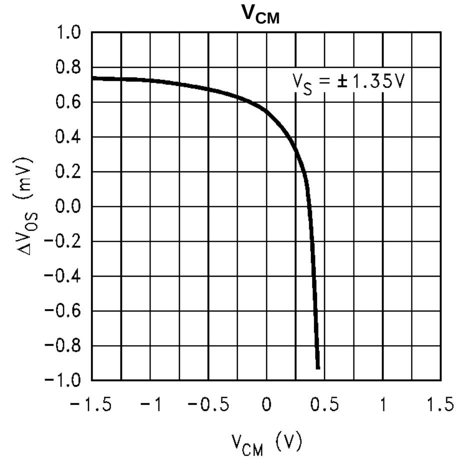


Figure 19.

ΔV_{OS} vs. V_{CM}

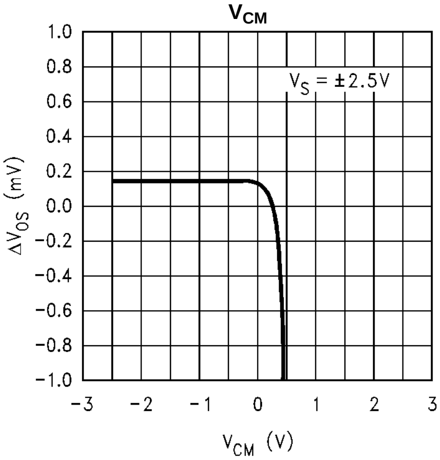


Figure 20.

Input Voltage vs. Output Voltage

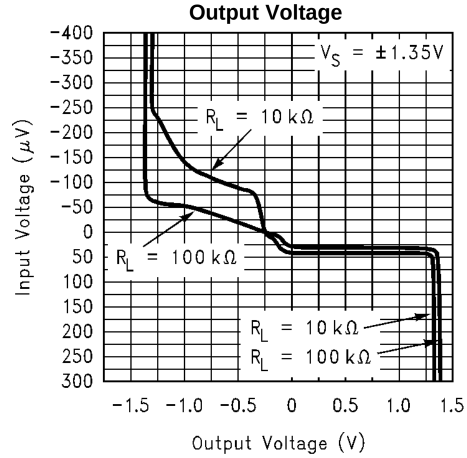


Figure 21.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Input Voltage vs. Output Voltage

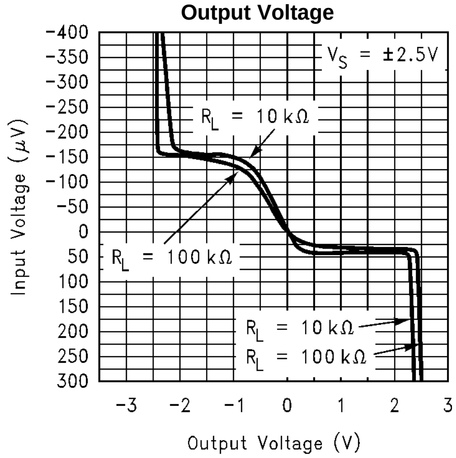


Figure 22.

Open Loop Frequency Response

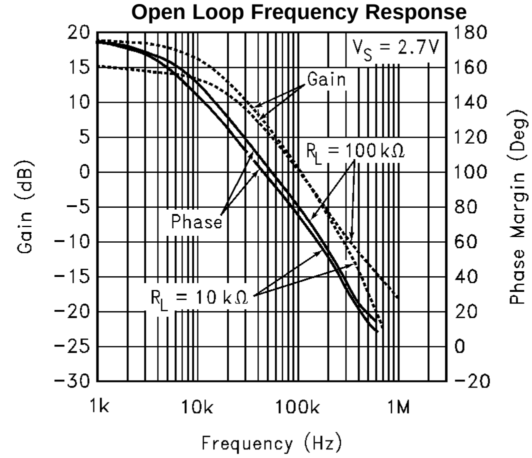


Figure 23.

Open Loop Frequency Response

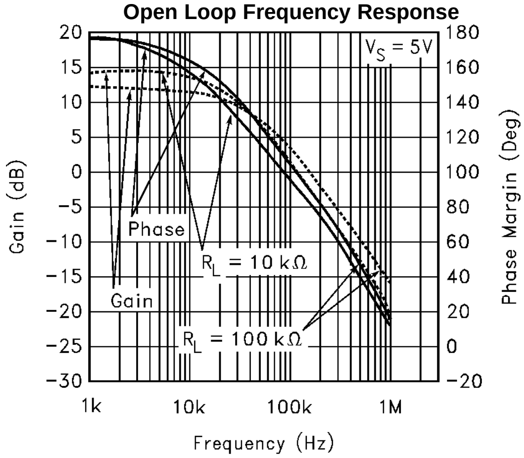


Figure 24.

Gain and Phase vs. Capacitive Load

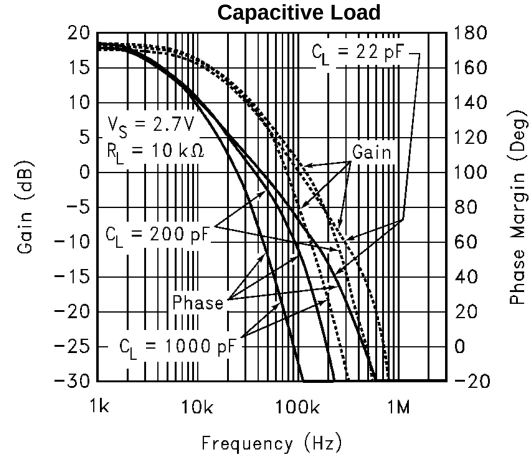


Figure 25.

Gain and Phase vs. Capacitive Load

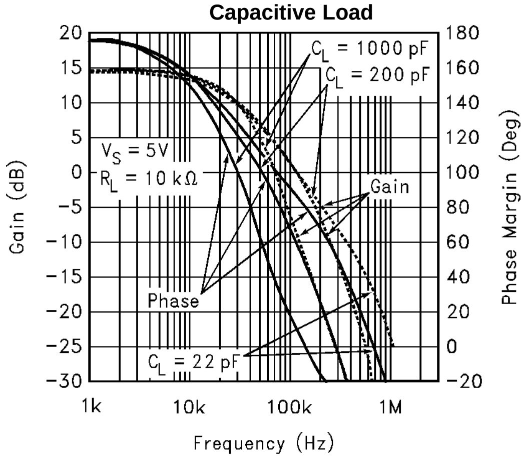


Figure 26.

Slew Rate vs. Supply Voltage

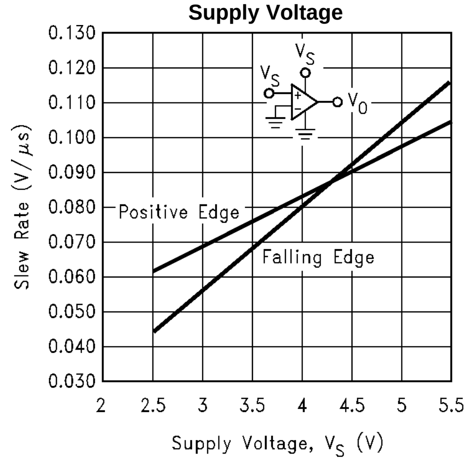


Figure 27.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Non-Inverting Large Signal Pulse Response

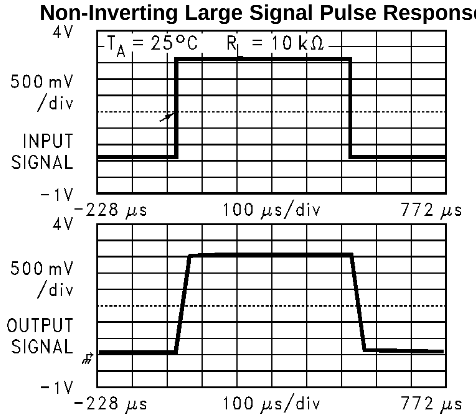


Figure 28.

Non-Inverting Small Signal Pulse Response

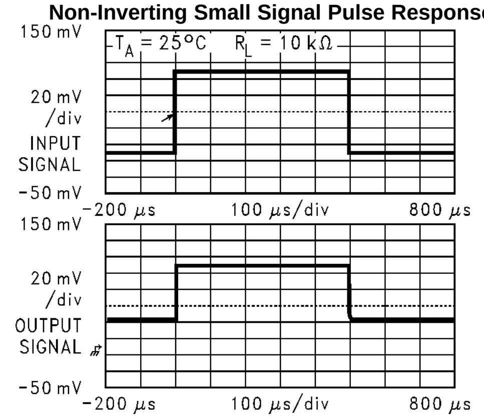


Figure 29.

Inverting Large Signal Pulse Response

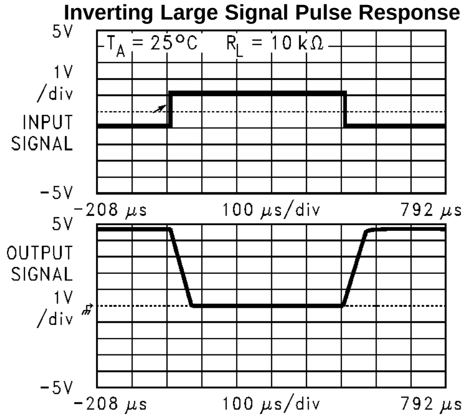


Figure 30.

Inverting Small Signal Pulse Response

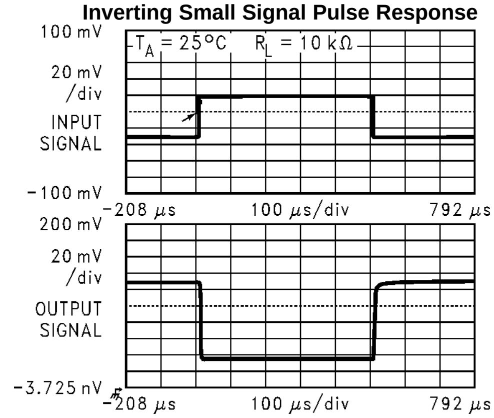


Figure 31.

Stability vs. Capacitive Load

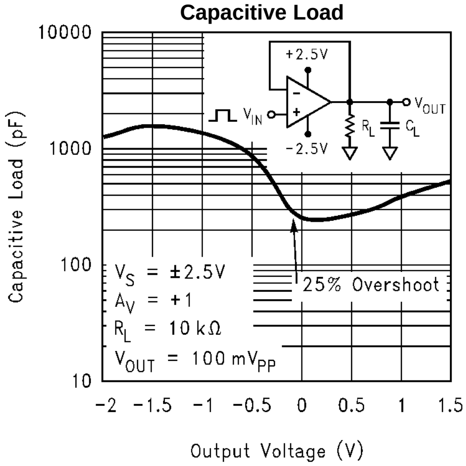


Figure 32.

Stability vs. Capacitive Load

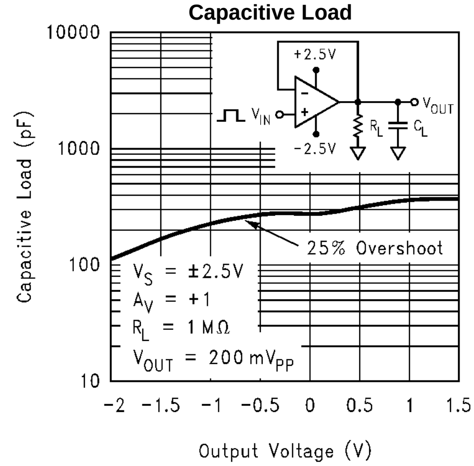


Figure 33.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Stability vs. Capacitive Load

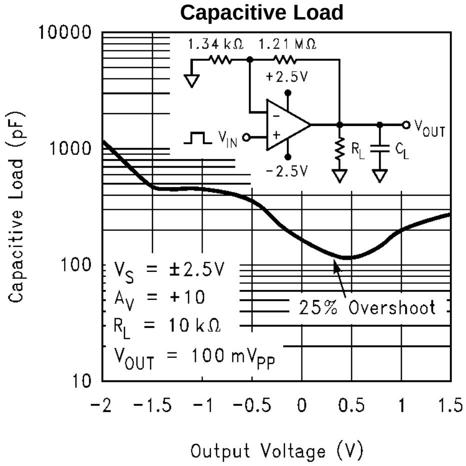


Figure 34.

Stability vs. Capacitive Load

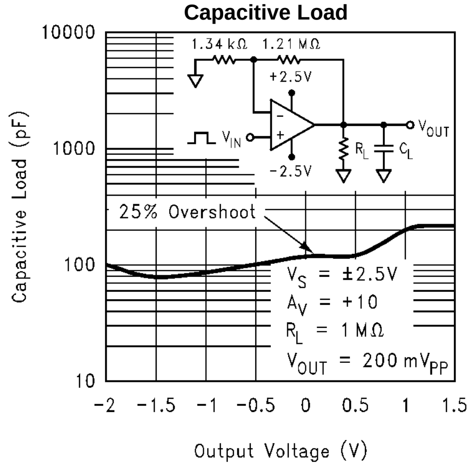


Figure 35.

THD vs. Frequency

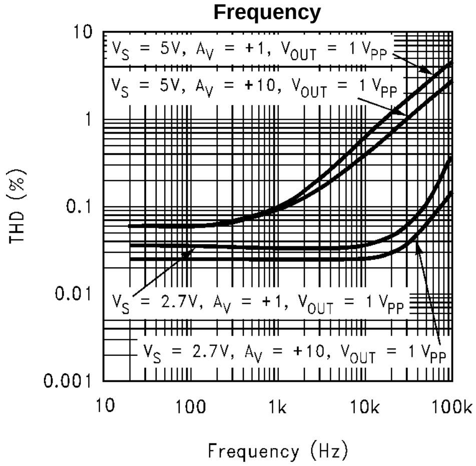


Figure 36.

Open Loop Output Impedance vs Frequency

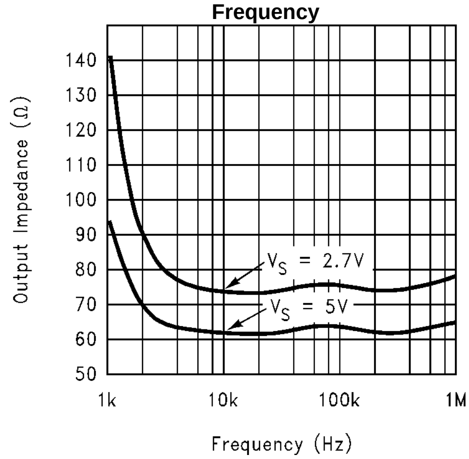


Figure 37.

Short Circuit Current vs. Temperature (Sinking)

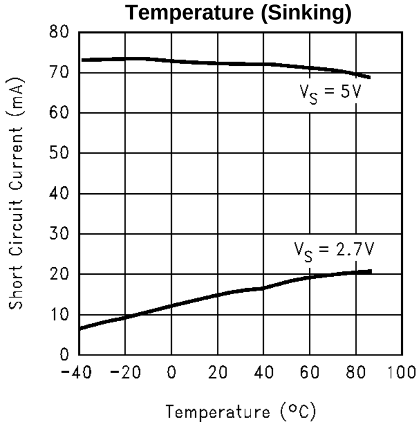


Figure 38.

Short Circuit Current vs. Temperature (Sourcing)

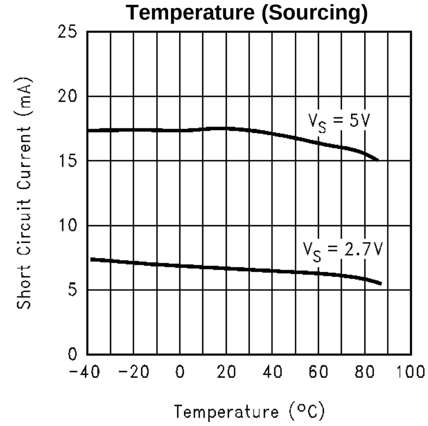


Figure 39.

APPLICATION INFORMATION

Benefits of the LPV321-N/358/324

Size

The small footprints of the LPV321-N/358/324 packages save space on printed circuit boards, and enable the design of smaller electronic products, such as cellular phones, pagers, or other portable systems. The low profile of the LPV321-N/358/324 make them possible to use in PCMCIA type III cards.

Signal Integrity

Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the LPV321-N/358/324 can be placed closer to the signal source, reducing noise pickup and increasing signal integrity.

Simplified Board Layout

These products help you to avoid using long pc traces in your pc board layout. This means that no additional components, such as capacitors and resistors, are needed to filter out the unwanted signals due to the interference between the long pc traces.

Low Supply Current

These devices will help you to maximize battery life. They are ideal for battery powered systems.

Low Supply Voltage

TI provides ensured performance at 2.7V and 5V. These specifications ensure operation throughout the battery lifetime.

Rail-to-Rail Output

Rail-to-rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

Input Includes Ground

Allows direct sensing near GND in single supply operation.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3V (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

Capacitive Load Tolerance

The LPV321-N/358/324 can directly drive 200 pF in unity-gain without oscillation. The unity-gain follower is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation. To drive a heavier capacitive load, circuit in Figure 40 can be used.

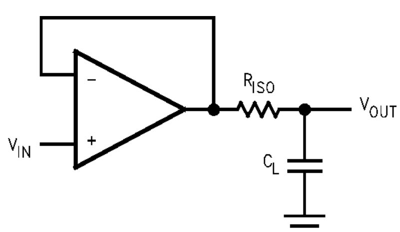


Figure 40. Indirectly Driving A Capacitive Load Using Resistive Isolation

In Figure 40, the isolation resistor R_{ISO} and the load capacitor C_L form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of R_{ISO}. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Figure 41 is an output waveform of Figure 40 using 100 kΩ for R_{ISO} and 1000 pF for C_L.

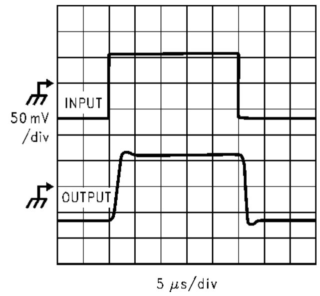


Figure 41. Pulse Response of the LPV324 Circuit in Figure 40

The circuit in Figure 42 is an improvement to the one in Figure 40 because it provides DC accuracy as well as AC stability. If there were a load resistor in Figure 40, the output would be voltage divided by R_{ISO} and the load resistor. Instead, in Figure 42, R_F provides the DC accuracy by using feed-forward techniques to connect V_{IN} to R_L. Caution is needed in choosing the value of R_F due to the input bias current of the LPV321-N/358/324. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop. Increased capacitive drive is possible by increasing the value of C_F. This in turn will slow down the pulse response.

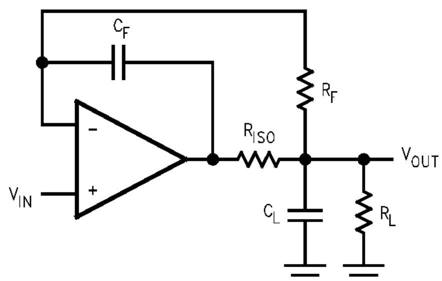


Figure 42. Indirectly Driving A Capacitive Load with DC Accuracy

Input Bias Current Cancellation

The LPV321-N/358/324 family has a bipolar input stage. The typical input bias current of LPV321-N/358/324 is 1.5 nA with 5V supply. Thus a 100 kΩ input resistor will cause 0.15 mV of error voltage. By balancing the resistor values at both inverting and non-inverting inputs, the error caused by the amplifier's input bias current will be reduced. The circuit in Figure 43 shows how to cancel the error caused by input bias current.

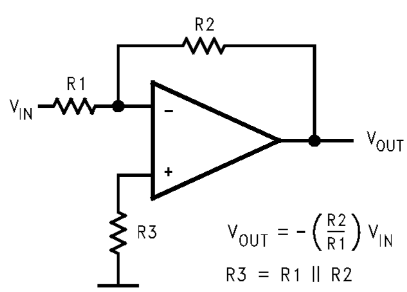


Figure 43. Cancelling the Error Caused by Input Bias Current

Typical Single-Supply Application Circuits

Difference Amplifier

The difference amplifier allows the subtraction of two voltages or, as a special case, the cancellation of a signal common to two inputs. It is useful as a computational amplifier, in making a differential to single-ended conversion or in rejecting a common mode signal.

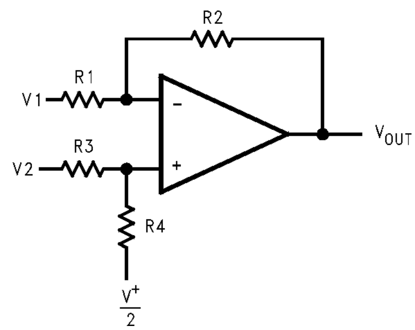


Figure 44. Difference Amplifier

$$V_{OUT} = \left(\frac{R1 + R2}{R3 + R4}\right)\frac{R4}{R1}V_2 - \frac{R2}{R1}V_1 + \left(\frac{R1 + R2}{R3 + R4}\right)\frac{R3}{R1} \bullet \frac{V^+}{2}$$

for R1 = R3 and R2 = R4

$$V_{OUT} = \frac{R2}{R1}\left(V_2 - V_1\right) + \frac{V^+}{2} \quad (1)$$

Instrumentation Circuits

The input impedance of the previous difference amplifier is set by the resistor R_1, R_2, R_3, and R_4. To eliminate the problems of low input impedance, one way is to use a voltage follower ahead of each input as shown in the following two instrumentation amplifiers.

Three-op-amp Instrumentation Amplifier

The quad LPV324 can be used to build a three-op-amp instrumentation amplifier as shown in Figure 45

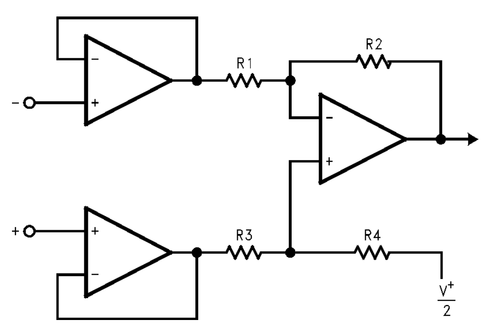


Figure 45. Three-op-amp Instrumentation Amplifier

The first stage of this instrumentation amplifier is a differential-input, differential-output amplifier, with two voltage followers. These two voltage followers assure that the input impedance is over 100 MΩ. The gain of this instrumentation amplifier is set by the ratio of R_2/R_1. R_3 should equal R_1 and R_4 equal R_2. Matching of R_3 to R_1 and R_4 to R_2 affects the CMRR. For good CMRR over temperature, low drift resistors should be used. Making R_4 Slightly smaller than R_2 and adding a trim pot equal to twice the difference between R_2 and R_4 will allow the CMRR to be adjusted for optimum.

Two-op-amp Instrumentation Amplifier

A two-op-amp instrumentation amplifier can also be used to make a high-input-impedance DC differential amplifier (Figure 46). As in the three-op-amp circuit, this instrumentation amplifier requires precise resistor matching for good CMRR. R_4 should equal to R_1 and R_3 should equal R_2.

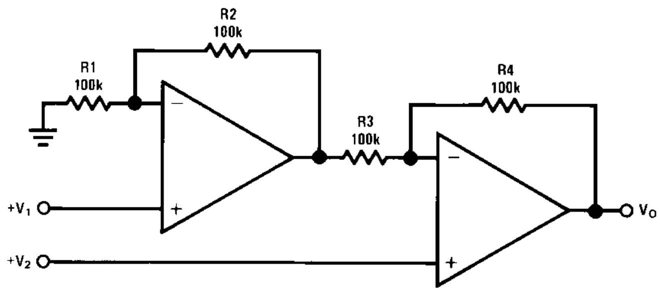


Figure 46. Two-op-amp Instrumentation Amplifier

$$V_O = \left(1 + \frac{R4}{R3}\right)(V_2 - V_1), \text{ where } R1 = R4 \text{ and } R2 = R3$$
$$\text{As shown: } V_O = 2(V_2 - V_1) \quad (2)$$

Single-Supply Inverting Amplifier

There may be cases where the input signal going into the amplifier is negative. Because the amplifier is operating in single supply voltage, a voltage divider using R_3 and R_4 is implemented to bias the amplifier so the input signal is within the input common-common voltage range of the amplifier. The capacitor C_1 is placed between the inverting input and resistor R_1 to block the DC signal going into the AC signal source, V_{IN}. The values of R_1 and C_1 affect the cutoff frequency,

$fc = 1/2\pi R_1C_1$ (3)

As a result, the output signal is centered around mid-supply (if the voltage divider provides $V^+/2$ at the non-inverting input). The output can swing to both rails, maximizing the signal-to-noise ratio in a low voltage system.

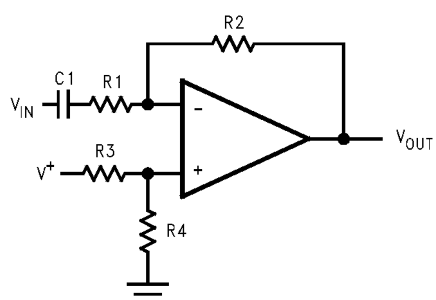


Figure 47. Single-Supply Inverting Amplifier

$$V_{OUT} = -\frac{R2}{R1}V_{IN} \quad (4)$$

Active Filter

Simple Low-Pass Active Filter

The simple low-pass filter is shown in Figure 48. Its low-frequency gain(ω → o) is defined by $-R_3/R_1$. This allows low-frequency gains other than unity to be obtained. The filter has a −20 dB/decade roll-off after its corner frequency fc. R_2 should be chosen equal to the parallel combination of R_1 and R_3 to minimize errors due to bais current. The frequency response of the filter is shown in Figure 49

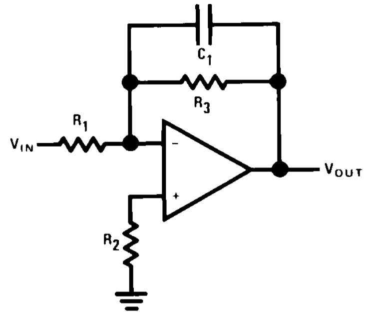


Figure 48. Simple Low-Pass Active Filter

$$A_L = -\frac{R_3}{R_1}$$
$$f_c = \frac{1}{2\pi R_3 C_1}$$
$$R_2 = R_1 \parallel R_3 \quad (5)$$

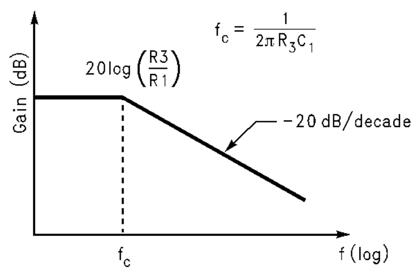


Figure 49. Frequency Response of Simple Low-pass Active Filter in Figure 9

Note that the single-op-amp active filters are used in to the applications that require low quality factor, Q (≤ 10), low frequency (≤ 5 kHz), and low gain (≤ 10), or a small value for the product of gain times Q (≤ 100). The op amp should have an open loop voltage gain at the highest frequency of interest at least 50 times larger than the gain of the filter at this frequency. In addition, the selected op amp should have a slew rate that meets the following requirement:

Slew Rate ≥ 0.5 x ($\omega_H V_{OPP}$) X 10^{-6}V/µsec

where

- ω_H is the highest frequency of interest
- V_{OPP} is the output peak-to-peak voltage (6)

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LPV321M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A27A	Samples
LPV321M5X	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	A27A	
LPV321M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A27A	Samples
LPV321M7	NRND	SC70	DCK	5	1000	TBD	Call TI	Call TI	-40 to 85	A19	
LPV321M7/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A19	Samples
LPV321M7X	NRND	SC70	DCK	5		TBD	Call TI	Call TI	-40 to 85	A19	
LPV321M7X/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A19	Samples
LPV324M/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LPV324M	Samples
LPV324MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LPV324 MT	Samples
LPV324MTX	NRND	TSSOP	PW	14	2500	TBD	Call TI	Call TI	-40 to 85	LPV324 MT	
LPV324MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LPV324 MT	Samples
LPV324MX	NRND	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 85	LPV324M	
LPV324MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LPV324M	Samples
LPV358M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LPV 358M	Samples
LPV358MM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	P358	
LPV358MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	P358	Samples
LPV358MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	P358	Samples
LPV358MX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LPV 358M	
LPV358MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LPV 358M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

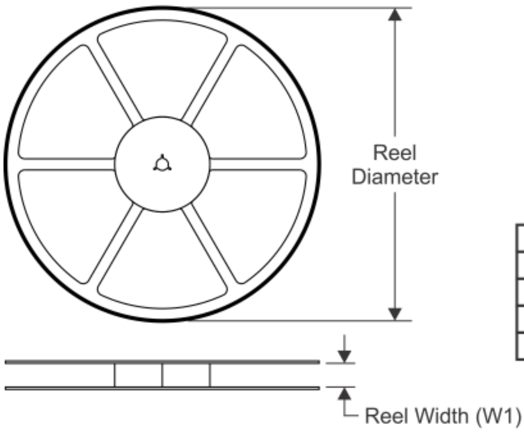
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

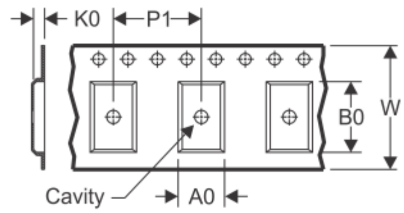
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

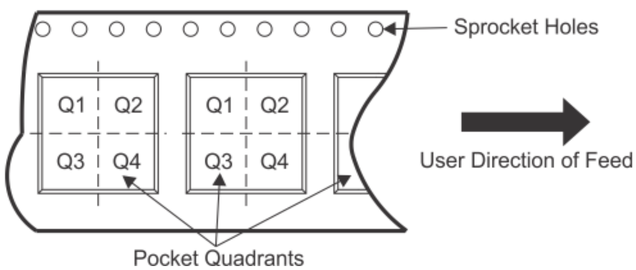


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

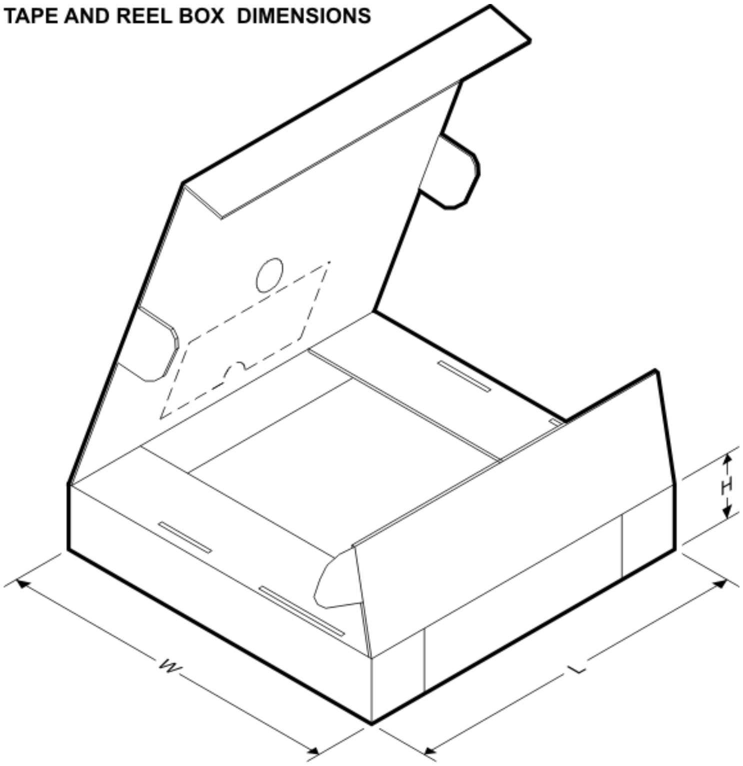
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV321M7	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV321M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV321M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV324MTX	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LPV324MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LPV324MX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LPV324MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LPV358MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV358MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV358MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV358MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LPV358MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

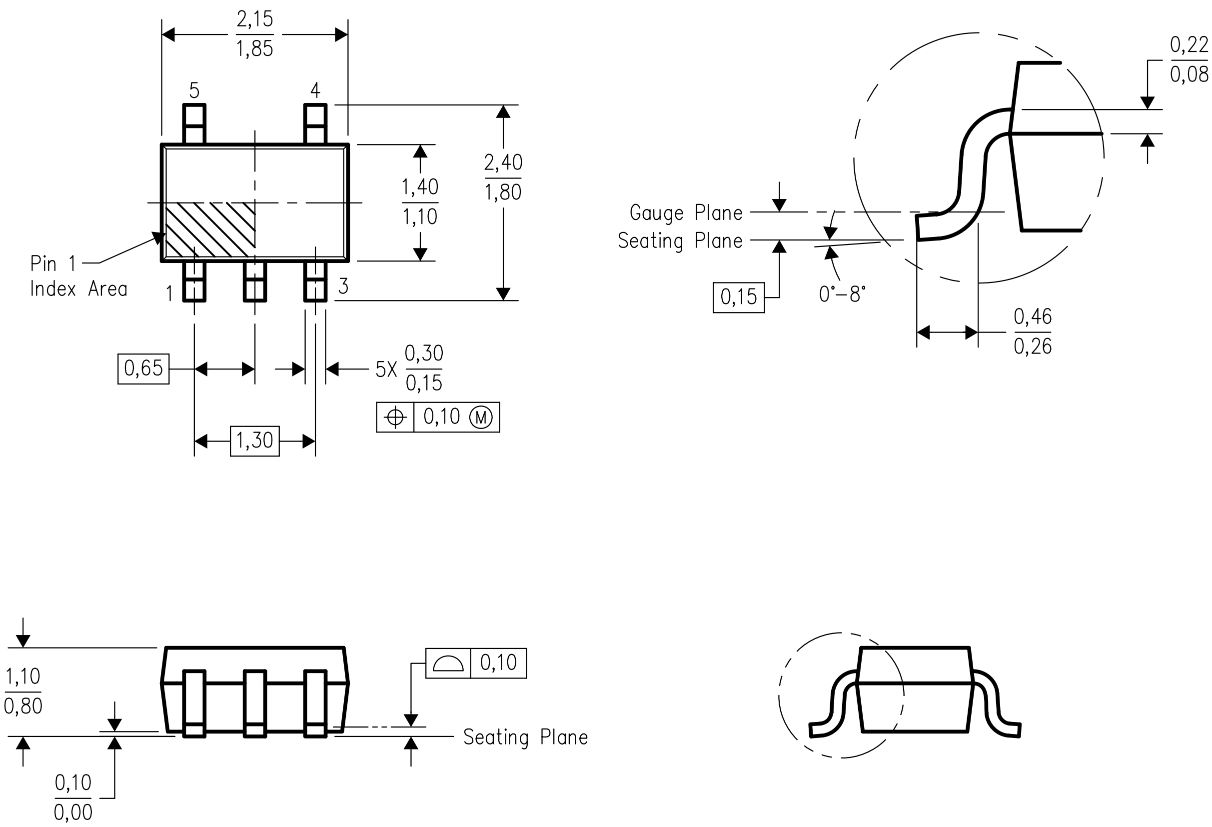
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV321M7	SC70	DCK	5	1000	210.0	185.0	35.0
LPV321M7/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LPV321M7X/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LPV324MTX	TSSOP	PW	14	2500	367.0	367.0	35.0
LPV324MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LPV324MX	SOIC	D	14	2500	367.0	367.0	35.0
LPV324MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LPV358MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LPV358MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LPV358MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LPV358MX	SOIC	D	8	2500	367.0	367.0	35.0
LPV358MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

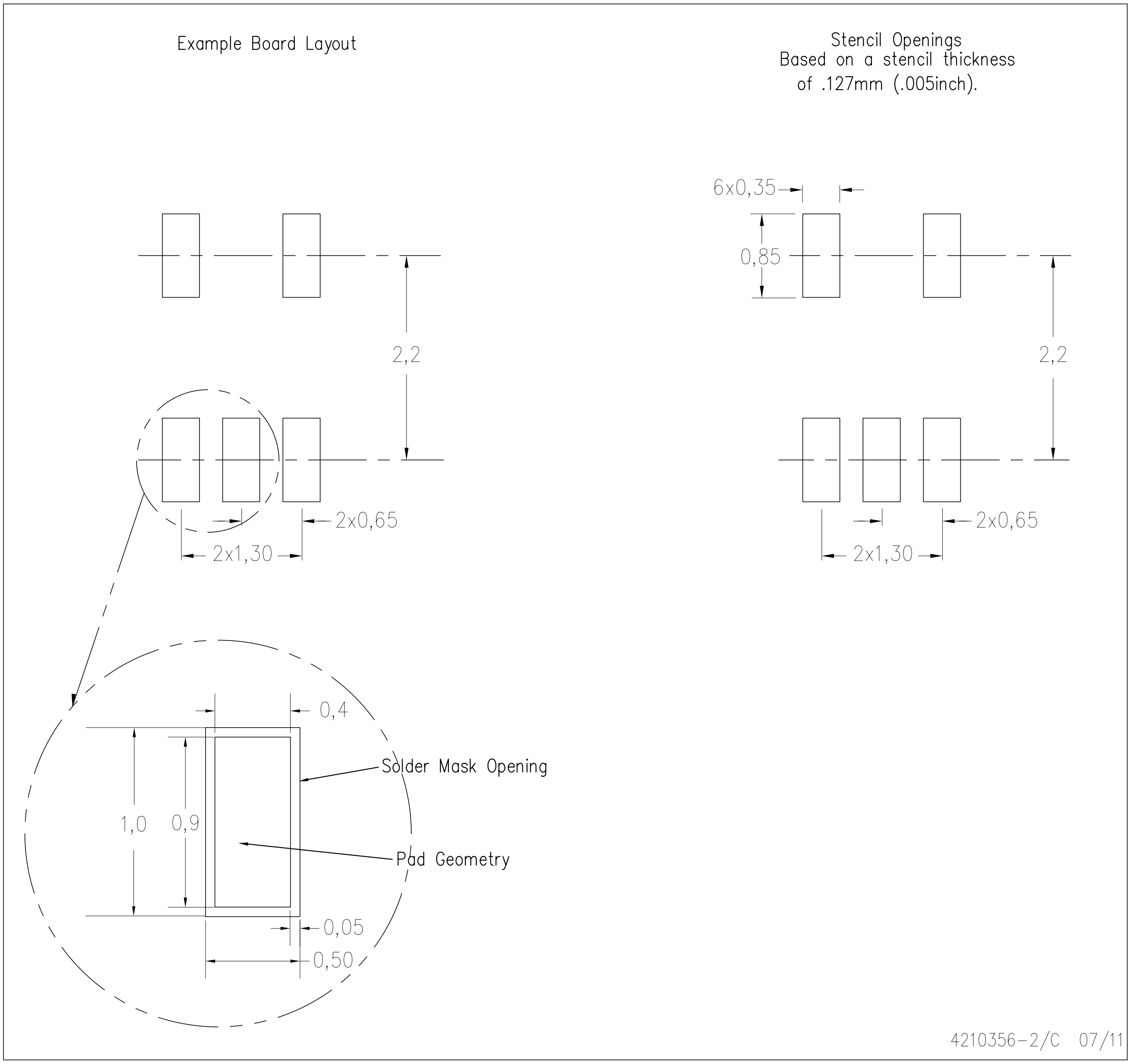
DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

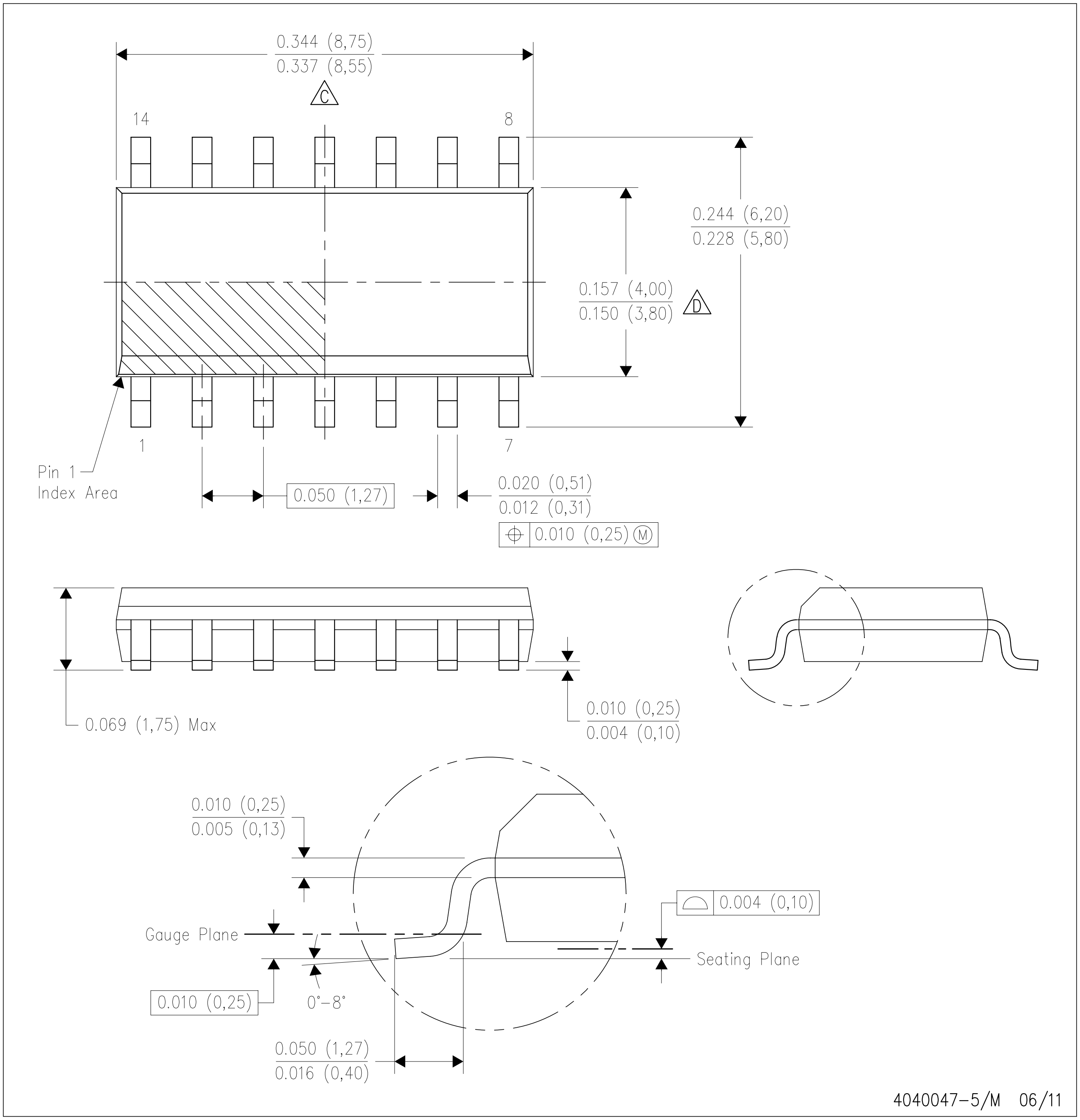
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



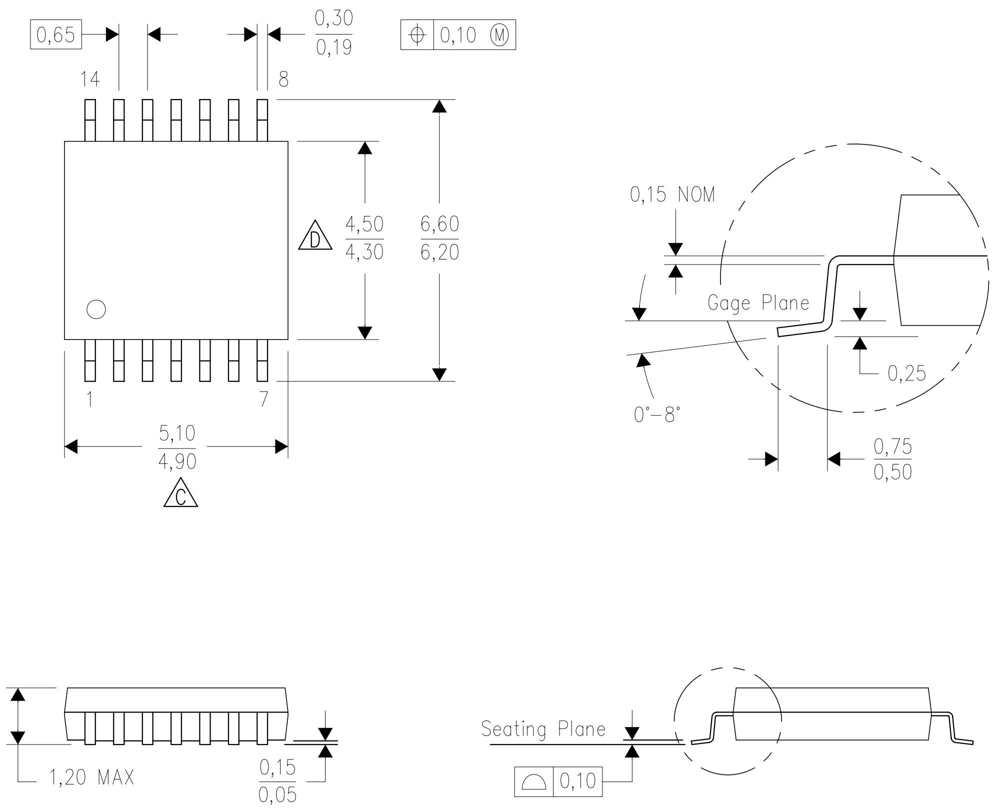
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

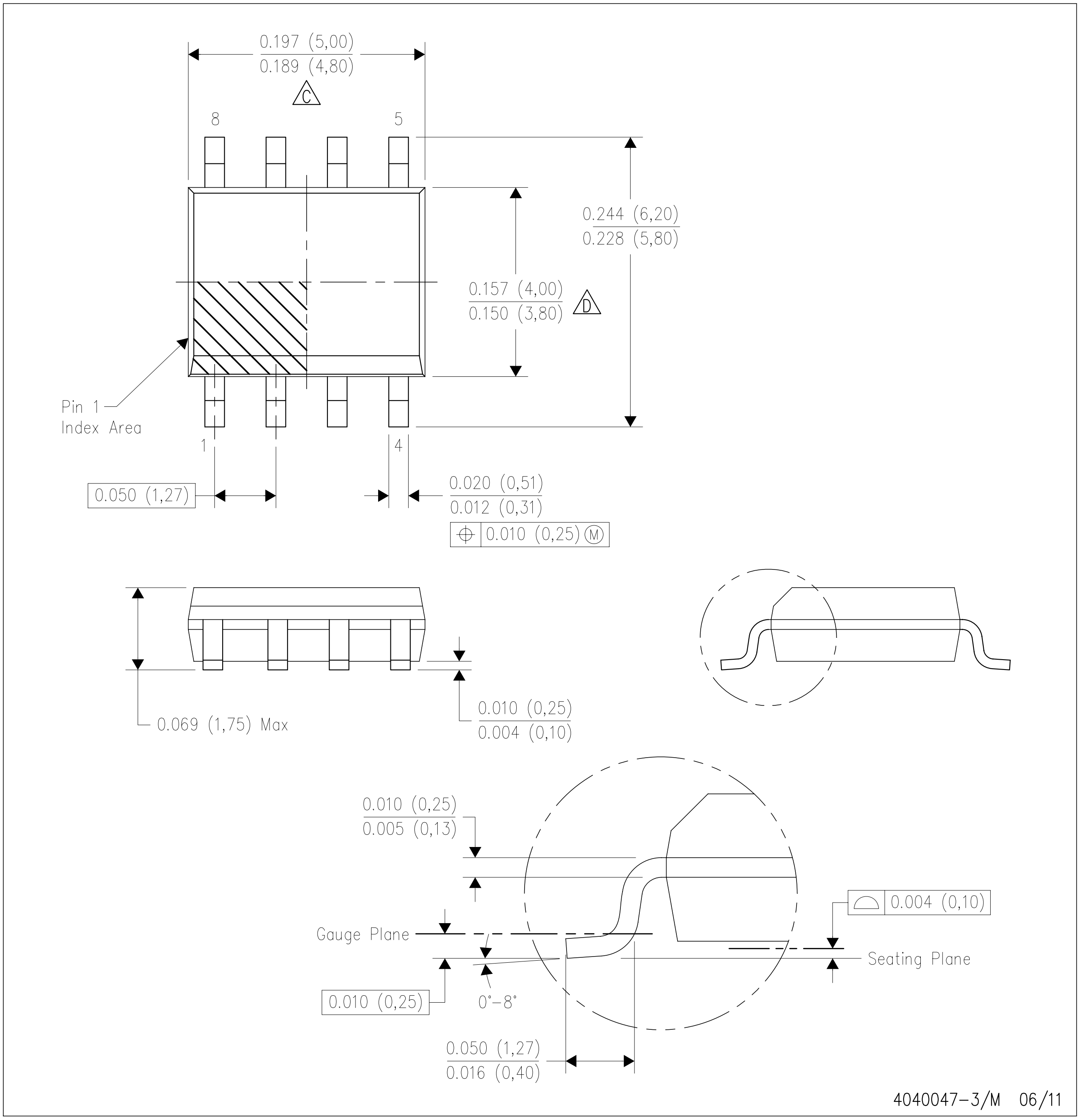
PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



4040064-3/G 02/11

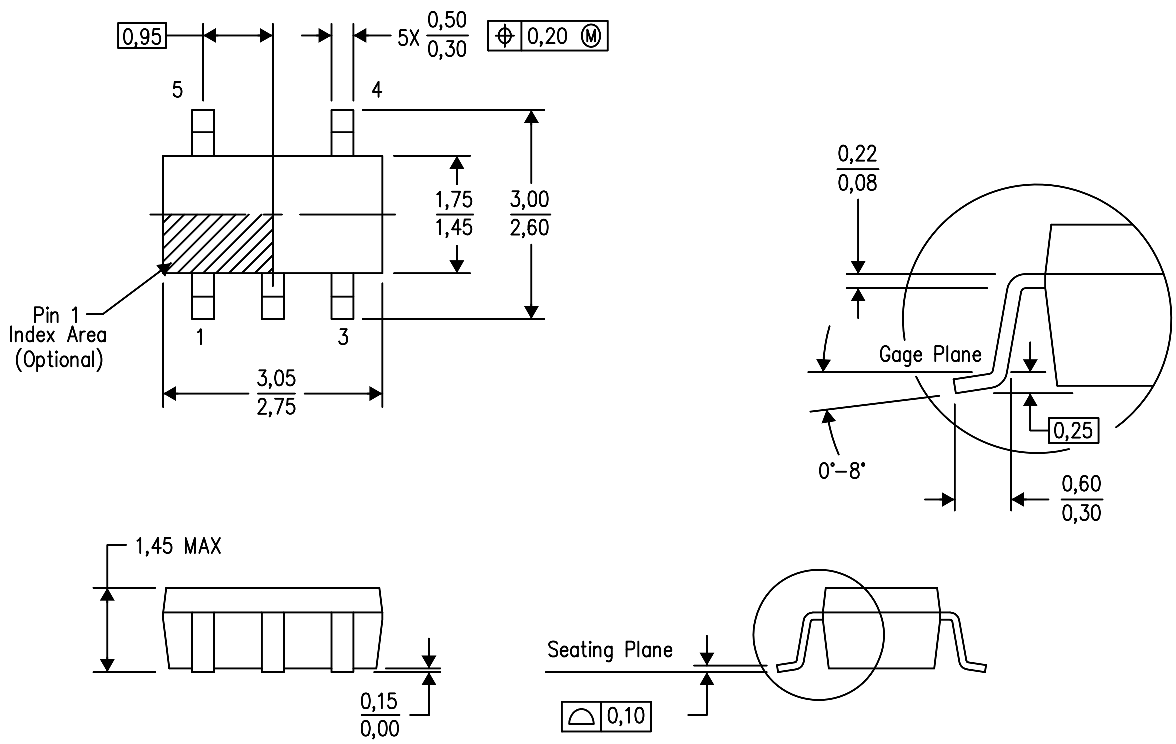
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

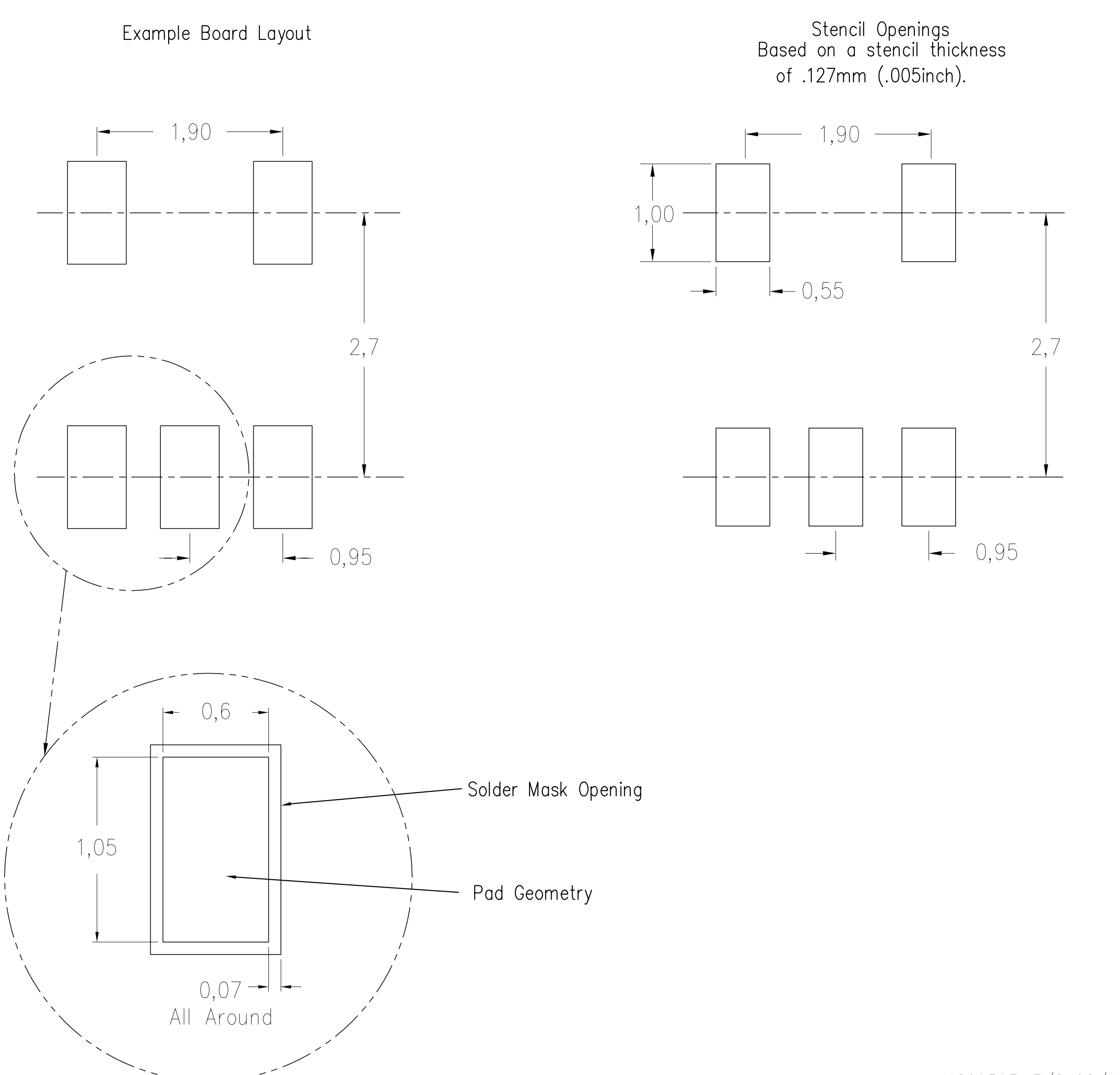
DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/N 12/14

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

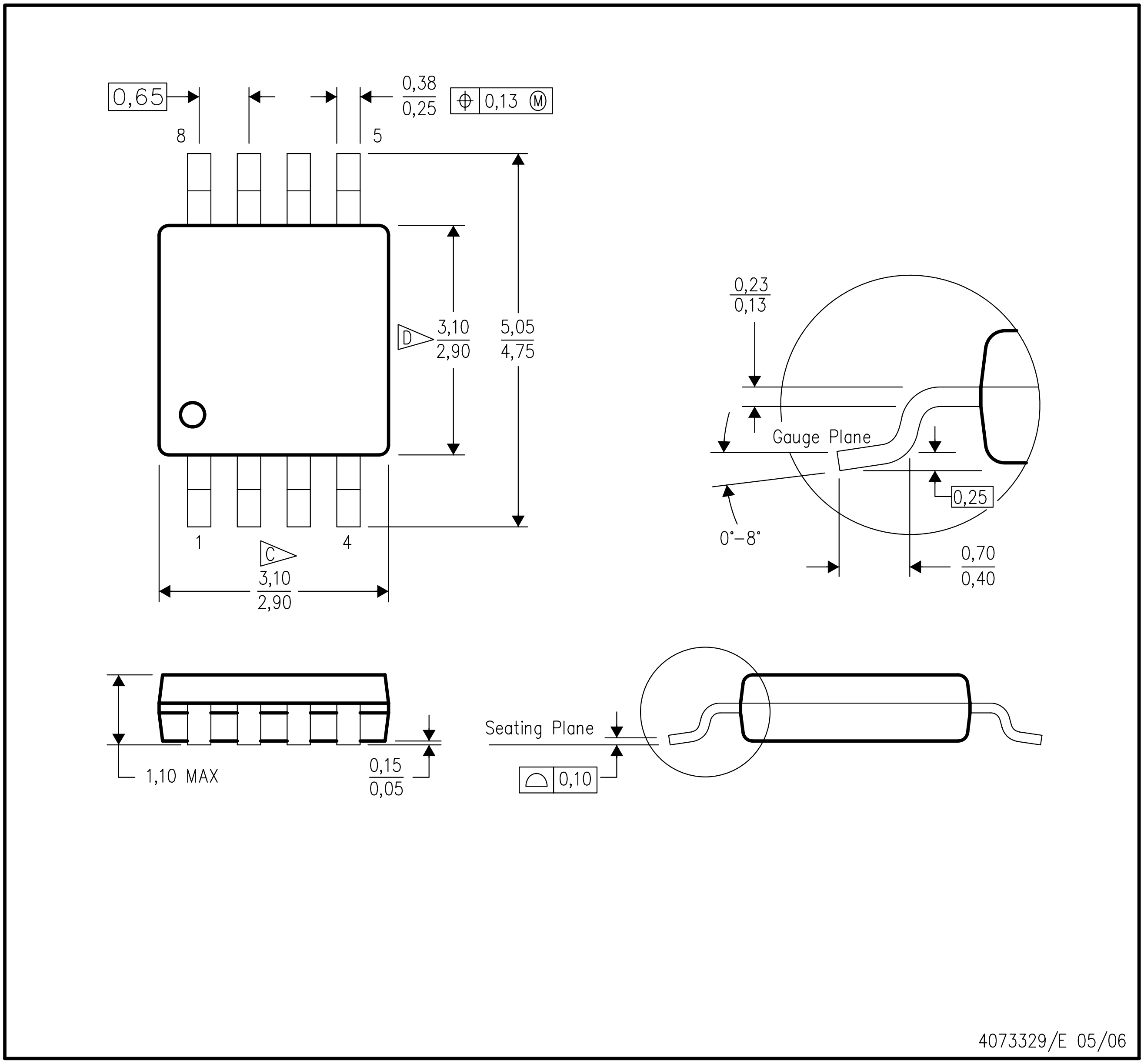
DBV (R-PDSO-G5) PLASTIC SMALL OUTLINE



4209593-3/C 08/11

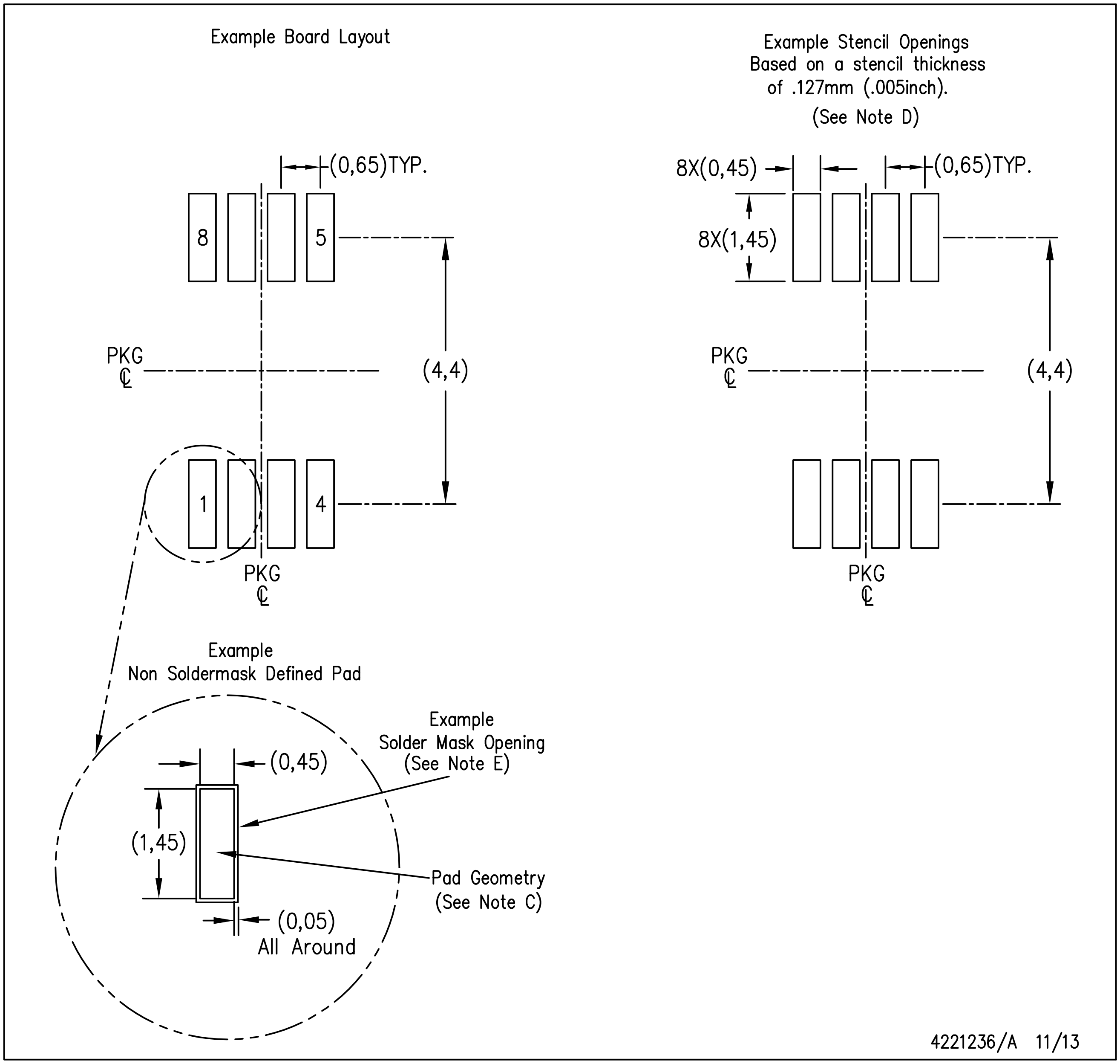
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.