PD70224

IdealBridge™ Dual MOSFET-Based Bridge Rectifier

Introduction

PD70224 is a dual pack of MOSFET-based full-bridge rectifiers. It contains low-RDS 0.16 Ω N-channel MOSFETs for much higher overall efficiency and higher output power, particularly when used in Powered Devices for Power over Ethernet (PoE) applications. The entire drive circuitry for driving the MOSFETs is on-chip, including a charge pump for driving the high-side N-channel MOSFETs. The total forward drop (bridge offset) introduced by the IdealBridge™ rectifier is only 192 mV at 0.6 A, compared to a standard bridge rectifier that typically presents 2000 mV of forward drop.

PD70224 IdealBridge™ can support over 2 A current, making it the ideal choice for IEEE®802.3bt (Type 3 and Type 4), IEEE 802.3at and IEEE 802.3af (Type 1 and Type 2). The PD70224 also supports legacy 4 pair standards such as UPoE (60 W) and POH (Power over HDBase-T, 95 W)..

In addition, PD70224 is capable of helping to identify at the physical layer itself whether a 2-pair PSE or a 4-pair PSE is providing power over the cable. It does that by sensing the voltage on the line (un-rectified) side of the pairs.

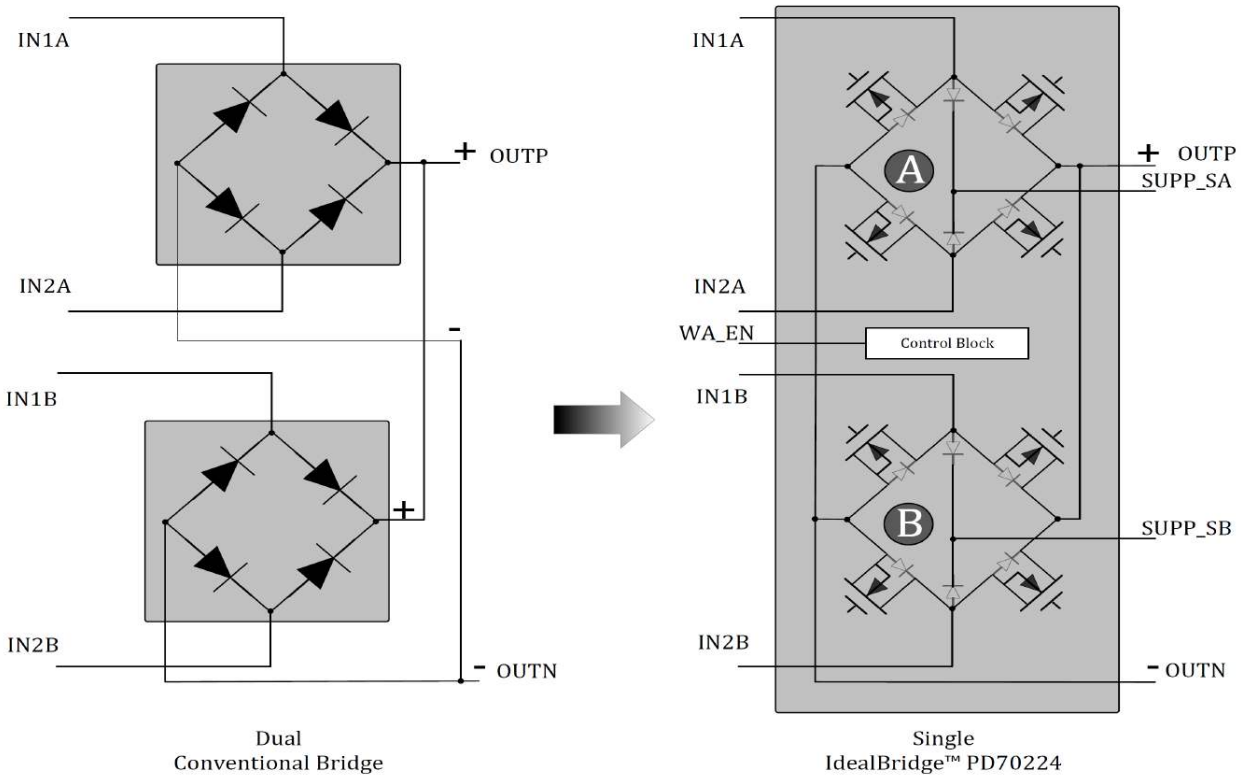
Features

- Active circuit with low forward-drop to replace dissipative passive diode bridges
- Self-contained drive circuitry for MOSFETs
- Designed to support IEEE 802.3af/at/bt, Universal PoE (UPOE), and Power over HDBase-T (PoH)
- Integrated 0.16 Ω N-Channel MOSFETs for 0.32 Ω total path resistance
- “Power present” indicator signals for identifying 4-pair bridge power
- Dedicated pin to implement adapter priority
- Low leakage, <10 µA during detection
- Wide operating voltage range up to 57 V
- -40 °C to 85 °C ambient
- Available in 40-pin package
- MSL3, RoHS compliant

Applications

- Power over Ethernet IEEE 802.3bt/at/af
- Proprietary 4-pair standards, UPOE, and POH

Figure 1. Dual Conventional Bridge Versus Single Ideal Bridge



Technical Support and Documentation

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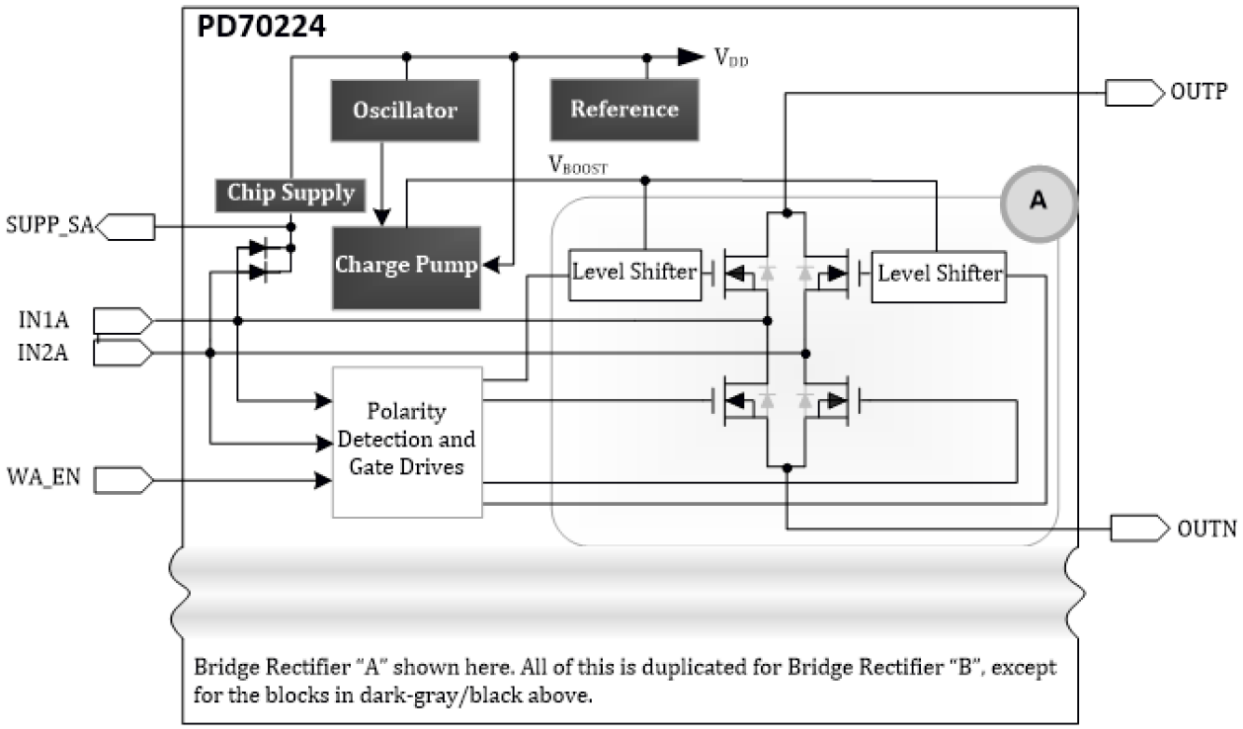
For access to any related application note or documentation please consult your local Microchip Client Engagement Manager or visit our website at www.microchip.com/poe.

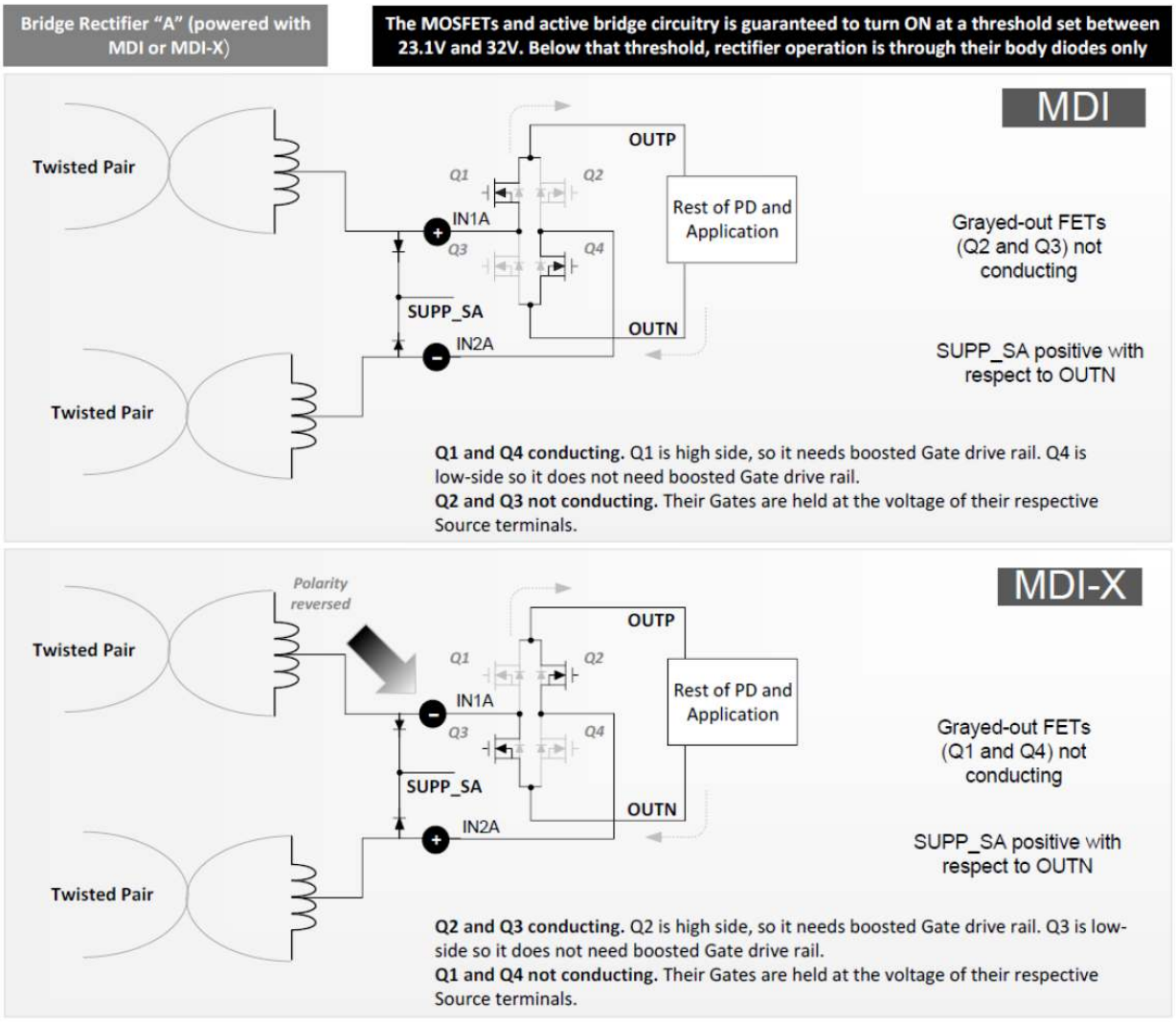
Table of Contents

1. Functional Descriptions

The following figure shows the functional blocks of PD70224.

Figure 1-1. Block Diagram





1.1 Purpose of Charge Pump

In the case that follows, the FETs connected to OUTP (the "high-side" FETs) are the ones that require a boosted gate drive rail so they can be turned ON. The on-chip charge pump provides the boosted gate drive rail for the high-side FETs. The FETs connected to OUTN ("low-side" FETs) do not need a boosted drive rail to be turned ON.

1.2 Purpose and Use of Supply Pins

Since the twisted pair set is delivering power, in the following case, SUPP_SA is positive with respect to OUTN. But if these two twisted pairs were not connected to a PSE, SUPP_SA would be low. For a standard 2-pair or 4-pair PDs with two bridge rectifiers (4-pairs), one connected to the data pairs, the other to the spare pairs, the presence of high voltage on SUPP_SA and/or SUPP_SB will indicate whether the data pairs or spare pairs, or both, are connected to PSEs. So SUPP_SA and SUP_SA and/or SUPP_SB will indicate whether the data pairs or spare pairs, or both, are connected to PSEs. So SUPP_SA and SUPP_SB can be used to indicate 2-pair or 4-pair PoE operation.

2. Electrical Specifications

The following section describes the electrical specifications of the device.

2.1 Absolute Maximum Ratings

Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability.

Table 2-1. Absolute Maximum Ratings

Parameter		Min	Max	Units
IN1A, IN1B, IN2A, IN2B to OUTN		–0.3	74	V
IN1A to IN2A		–0.3	74	V
IN1B to IN2B		–0.3	74	V
IN1A, IN1B, IN2A, IN2B to OUTP		–74		V
IN1A, IN2A to IN1B		–0.3	74	V
IN1A, IN2A to IN2B		–0.3	74	V
OUTP to OUTN		–0.3	74	V
OUTP to IN1A, IN1B, IN2A, IN2B		–0.3	74	V
SUPP_SA, SUPP_SB to OUTN		–0.3	74	V
WA_EN to OUTN		–0.3	5.5	V
I_{INA}, I_{INB} (currents through bridge A or B)			1.5	A
Junction temperature			150	°C
Lead soldering temperature (40 s, reflow)			260	°C
Storage temperature		–65	150	°C
ESD rating	HBM		±1250[1]	V
	MM		±100	V
	CDM		±2000	V

1. All pins pass 1250 V, except IN1A and IN2A that pass 1000 V.

Note: EPAD1 is connected by copper plane on PCB to OUTP, and EPAD2 is similarly connected to OUTN. OUTN is ground for IC.

2.2 Operating Ratings

Performance is generally guaranteed over this range as provided under Electrical Characteristics.

Table 2-2. Operating Ratings

Parameter	Min	Max	Units
IN1A, IN1B to OUTN		57	V
IN2A, IN2B to OUTN		57	V
WA_EN to OUTN	–0.3	5	V
Junction temperature	–40	125	°C
Port Current (I_{INx})	0	1.5	A

2.3 Electrical Characteristics

Unless otherwise specified under conditions, the Min and Max ratings stated below apply over the entire specified operating ratings of the device. Typ values stated are either by design or by production testing at 25 °C ambient.

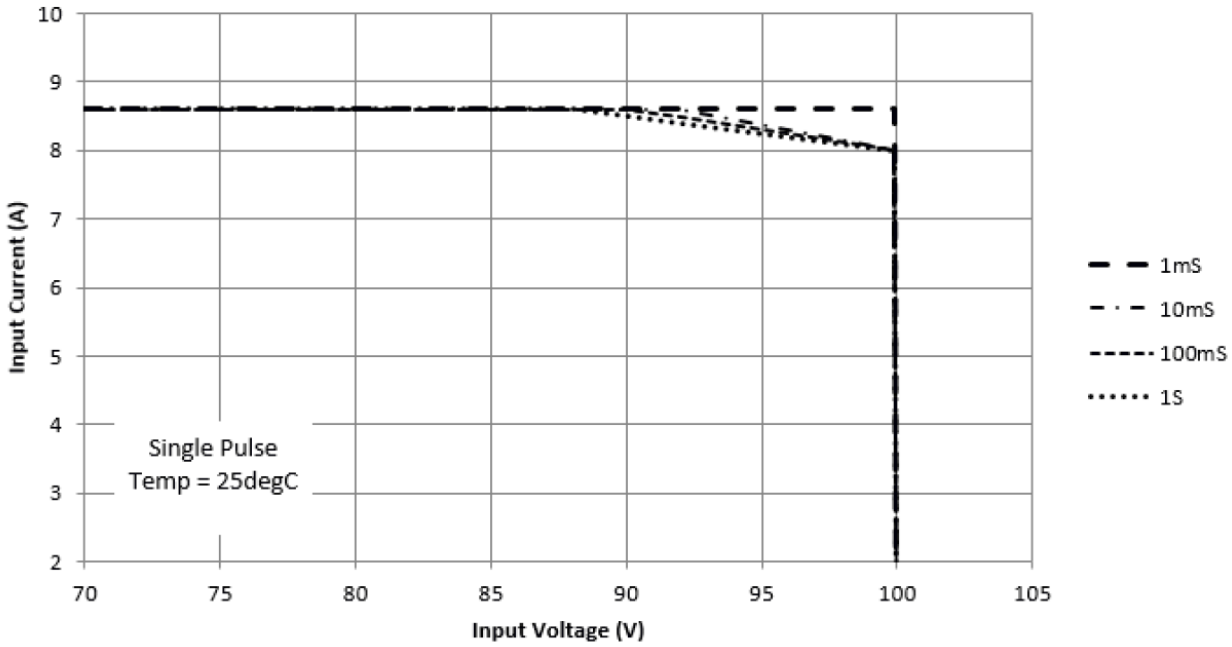
Table 2-3. Typical Electrical Performance

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{INx}	Input Voltage for Bridge “x”, where x is “A” or “B”.				57	V
ΔI_Q	Differential Quiescent Current $I(V_{IN}=10.1\ V) – I(V_{IN}=2.5\ V)$;	2.5 V < V_{INx} < 10.1 V; No load between OUTP and OUTN; No load on SUPP_Sx pins.		6	10	µA
I_Q	Quiescent Current (single bridge)	10.2 V < V_{INx} < 23 V; No load between OUTP & OUTN; No load on SUPP_Sx pins.			85	µA
	Quiescent Current (both bridge combined)	V_{INx} = 55 V; No load between OUTP & OUTN; No load on SUPP_Sx pins.			900	µA
V_{TURN_ON}	Active turn-on voltage of FETs		23.1	27.5	32	V
V_{HYST}	Turn-on voltage hysteresis			0.4		V
T_{ALT}	Alternate input voltage polarity – Delay time required (V_{IN} = 0 V) while alternating input voltage polarity.		200			ms
V_{OFFSET}	Bridge offset @ Off state	V_{INx} < V_{TURN_ON}, two body diodes in series I_{INx} = 40 mA			1.8	V

.....continued

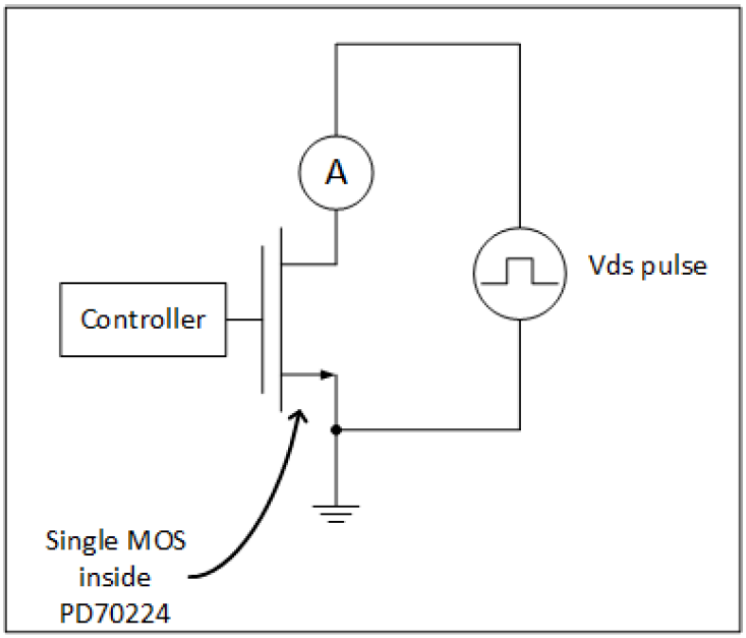
Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{DS}	FET drain to source resistance	I_D = 0.6 A T_J = 25 °C		0.16	0.26	Ω
		I_D = 0.6 A; –40 °C ≤ T_J ≤ 125 °C			0.38	Ω
I_R	Leakage current (reverse)	$V_{OUTP} – V_{OUTN}$ = 57 V			80	µA
V_{BFD}	Backfeed voltage	Between input terminals with 100 kΩ resistor across them and 57 V between OUTP and OUTN			2.7	V
I_{MAX_Off}	Maximum Forward Current (per bridge) below V_{TURN_ON}				0.45	A
I_{MAX_On}	Maximum forward current (per bridge) above V_{TURN_ON}. Per bridge, while only one bridge out of the two is active.				1.5	A
I_{MAX_LOAD}	Maximum load current (per device) above V_{TURN_ON}. Per device while two bridges are active and each bridge is supporting half load.				2	A
V_{D_SUPP}	Maximum voltage drop between INx to SUPP_Sx pins.	Supp_Sx loaded with 100 kΩ resistor			2	V
I_{MAX_SUPP}	Maximum current to consume from SUPP_Sx pins.				10	mA
V_{IH}	WA_EN – Input high logic		1.35			V
V_{IL}	WA_EN – Input low logic				1.05	V

Figure 2-1. Safe Operating Area



The PD70224 SOA is based on measuring the SOA of a single NMOS device that is used to construct the diode bridge.

Figure 2-2. SOA Test Setup



This data is provided for information purposes. For additional information on Surge Immunity and Microchip Recommendations, see AN3410 PD Surge Protection for ITU-T k.21 2019.

3. Pin Descriptions

The following illustration is a representation of PD70224 device, as seen from the top and bottom view.

Figure 3-1. Internal Construction and Pinout

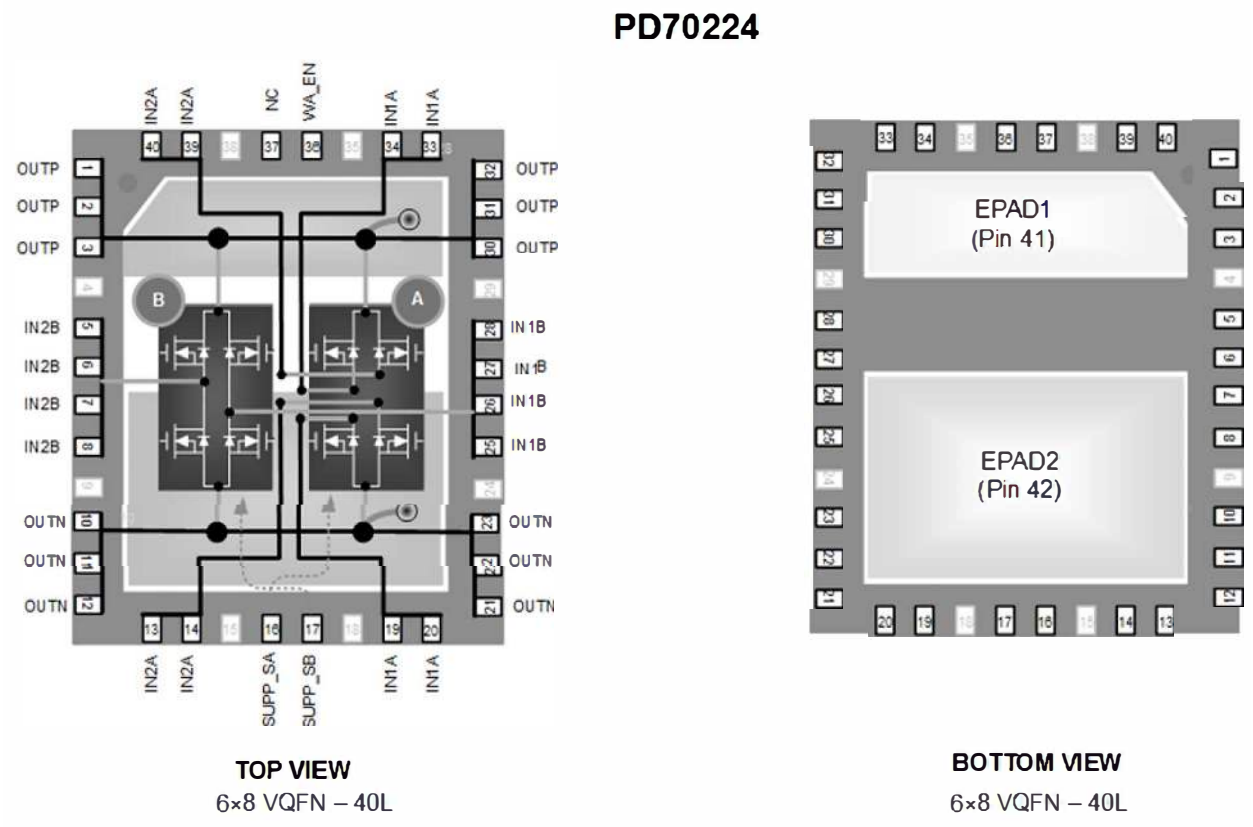


Table 3-1. Pin Description

Pin Number PD70224 VQFN 40 Lead	Pin Designator	Description
1, 2, 3	OUTP	Rectified positive (upper) rail shared by both bridges
4	N.A.	Not applicable (pin not present)
5, 6, 7, 8	IN2B	Input “2” of bridge rectifier number B
9	N.A.	Not applicable (pin not present)
10, 11, 12	OUTN	Rectified negative (lower) rail shared by both bridges
13, 14	IN2A	Input “2” of bridge rectifier number A (same as pins 39 and 40)[1]
15	N.A.	Not applicable (pin not present)
16	SUPP_SA	Input power supply detect pin for bride rectifier number A. Goes high when pairs connected to this bridge are powered by the PSE.
	N.A.	Not applicable (pin not present)
17	SUPP_SB	Input power supply detect pin for bride rectifier number B. Goes high when pairs connected to this bridge are powered by the PSE.

.....continued		
Pin Number PD70224 VQFN 40 Lead	**Pin Designator**	**Description**
18	N.A.	Not applicable (pin not present)
19, 20	IN1A	Input “1” of bridge rectifier number A.[2]
21, 22, 23	OUTN	Rectified negative (lower) rail shared by both bridges (same as pins 10, 11, and 12)
24	N.A.	Not applicable (pin not present)
25, 26, 27, 28	IN1B	Input “1” of bridge rectifier number B
29	N.A.	Not applicable (pin not present)
30, 31, 32	OUTP	Rectified positive (upper) rail shared by both bridges (same as pins 1, 2, and 3)
33, 34	IN1A	Input “1” of bridge rectifier number A (same as pins 19 and 20)[3]
35	N.A.	Not applicable (pin not present)
36	WA_EN	While this input is low (referenced to OUTN), the chip work according to internal flow diagram. When this input is high, it enable wall adapter feature, that is, turn OFF internal switches and act as regular diode bridge.
	N.A.	Not applicable (pin not present)
37	N.C.	Not connected; do not connect externally (leave floating)
38	N.A.	Not applicable (pin not present)
39, 40	IN2A	Input “2” of bridge rectifier number A (same as pins 13 and 14)[4]
41	EPAD1	Connect to OUTP on PCB
42	EPAD2	Connect to OUTN on PCB

Notes:

1. These pins are not shorted to pins 39 and 40 inside the device. The device functionality relies on a copper trace on the PCB, between pins 13, 14, 39, and 40.
2. These pins are not shorted to pins 33 and 34 inside the device. The device functionality relies on a copper trace on the PCB, between pins 33, 34, 19, and 20.
3. These pins are not shorted to pins 19 and 20 inside the device. The device functionality relies on a copper trace on the PCB, between pins 33, 34, 19, and 20.
4. These pins are not shorted to pins 13 and 14 inside the device. The device functionality relies on a copper trace on the PCB, between pins 13, 14, 39, and 40.

4. Package Information

4.1 Package Outline Drawing

Figure 4-1. PD70224 Package Outline Drawing 40-Pin QFN 6 mm × 8 mm

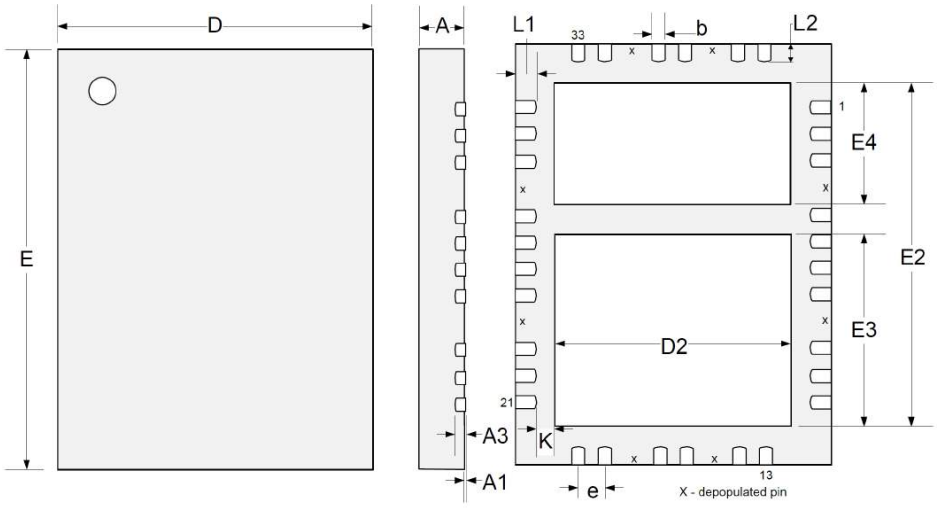


Table 4-1. Package Measurements

Dim	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	6.00 BSC		0.236 BSC	
E	8.00 BSC		0.315 BSC	
D2	4.25	4.50	0.167	0.177
E2	6.35	6.6	0.250	0.260
E3	3.50	3.75	0.138	0.148
E4	2.20	2.46	0.087	0.097
e	0.50 BSC		0.020 BSC	
K	0.30		0.012	
L1	0.37	0.57	0.014	0.022
L2	0.30	0.50	0.012	0.020

Notes:

1. Dimensions do not include protrusions; these shall not exceed 0.155 mm (.006") on any side. Lead dimension shall not include solder coverage.
2. Dimensions are in millimeters, inches for reference only.

4.2 Thermal Specifications

The following table lists the thermal specifications of PD70224.

Table 4-2. Thermal Properties

Thermal Resistance	Min	Typ	Max	Units
θ_{JA}		31		°C/W
θ_{JL}		2.5		°C/W
θ_{JC}		5		°C/W

Note: The θ_{JX} numbers assume no forced airflow. Junction temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

4.3 Recommended PCB Layout

The following figures show the PD70224 recommended PCB layout for 40-pin QFN 6 mm × 8 mm.

The pad for pins 4, 9, 15, 18, 24, 29, 35, and 38 is missing from the layout because it does not exist in package.

Figure 4-2. Top-Layer Copper (mm)

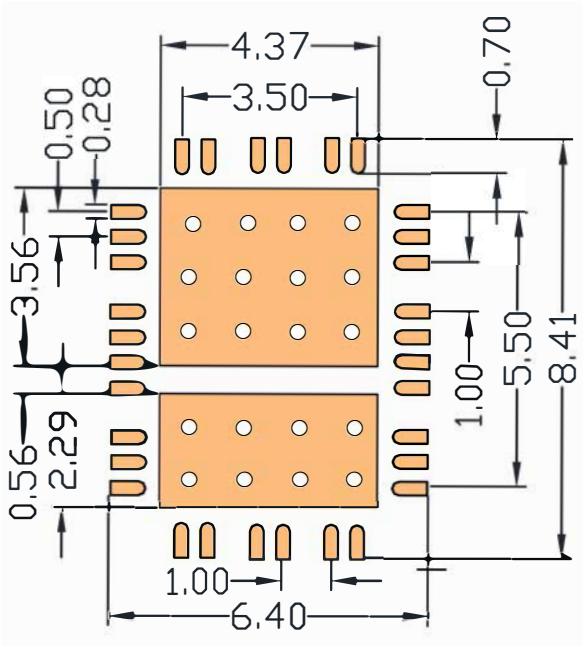


Figure 4-3. Top-Layer Solder Mask, Solder Paste, and Vias (mm)

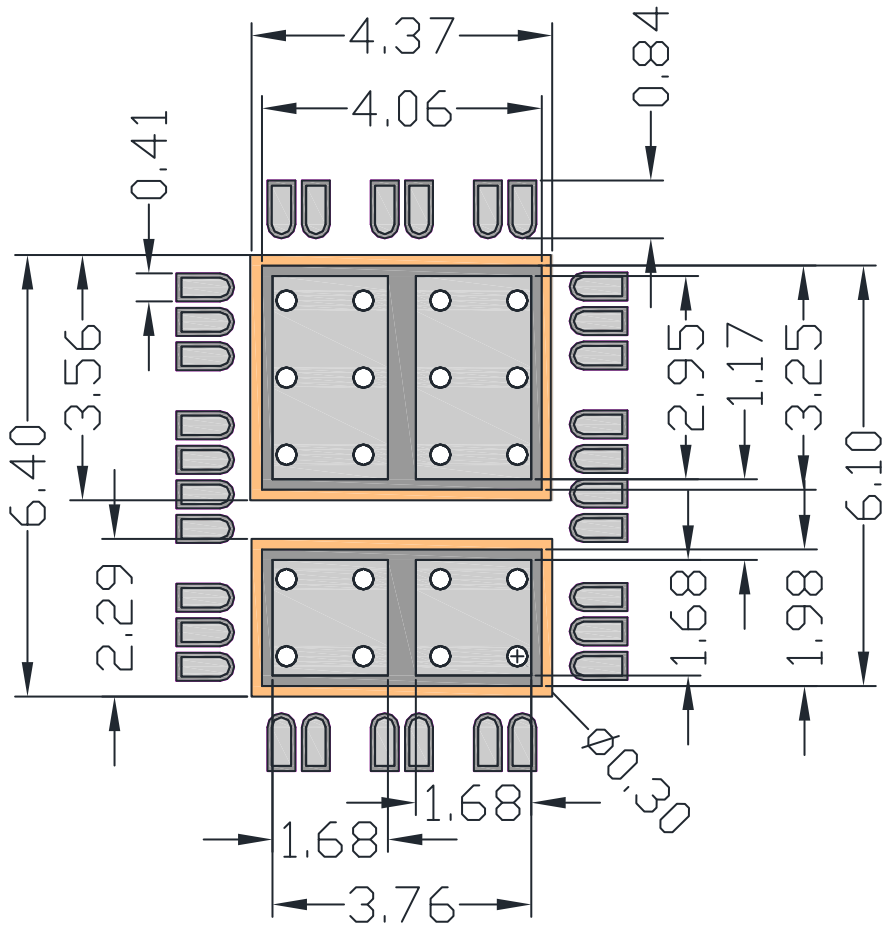
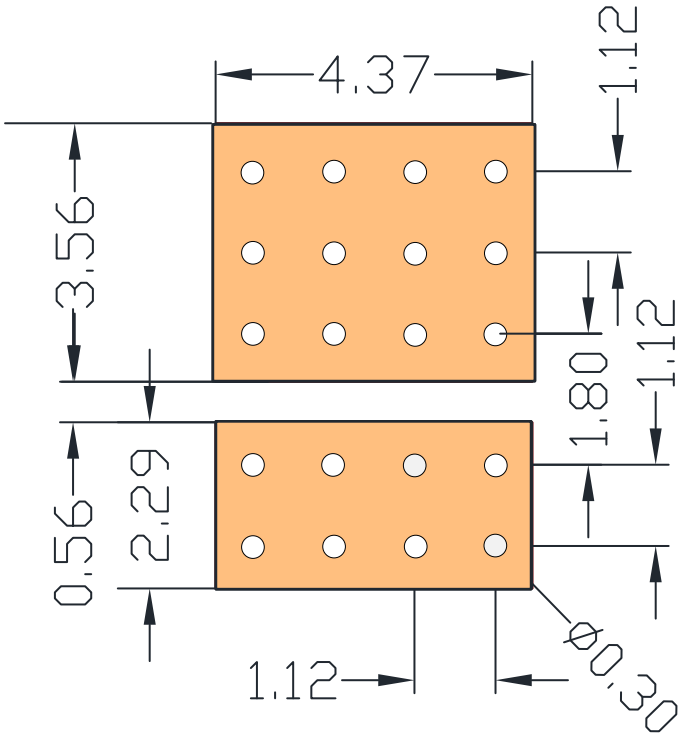


Figure 4-4. Bottom Layer Copper and Vias for Thermal Pad Array (mm)



Note: The contract manufacturer has latitude to modify the solder paste stencil for manufacturability reasons. The solder paste stencil covers 65% to 80% of the thermal pad and should not allow solder to be applied to the thermal vias under the QFN package using any method they deem appropriate. At the pin, the dimension of the paste mask should be 5-10% smaller than the PCB copper feature. Minimize the extension of the solder mask outside the edge of the package. Any design should be subject to system validation and qualification prior to commitment to mass production of field deployment. Use a 5 mil stencil.

5. Application Information

The following section describes the application information of the device.

5.1 Peripheral Devices

PD applications utilizing PD70224 IC should use 1 nF/100 V ceramic capacitor at Bridge A inputs and at Bridge B inputs.

For surge and ESD protection, refer to AN3410, Design for PD System Surge Immunity PD701xx PD702xx.

A 10 kΩ resistor should be placed on SUPP_SA and SUPP_SB lines between PD70224 and PD70210A.

When WA_EN function is not used, connect WA_EN pin to OUTN Pin.

When WA_EN function is used, connect a capacitor (1 nF to 100 nF/10V) between WA_EN pin and OUTN Pin.

The devices are presented in the figures PD70224 Package Outline Drawing 40-Pin QFN 6 mm × 8 mm and PD70224 Top layer Copper Recommended PCB Layout (mm).

5.2 Operation with an External DC Source

PD applications utilizing the PD70224 IC may be operated with an external power source (DC wall adaptor). There are two cases of providing power with an external source, as shown in the following figures.

Note: Protection is not shown in either figure, see application note “Design for PD System Surge Immunity" for recommended protection scheme.

1. External source connected to application’s low voltage supply rails. External source voltage level is dependent on DCDC output characteristics. This connection is not affected by the PD70224 use.
2. External source connected to PD device output connection toward the application (VPP to VPNOUT). External source voltage level is dependent on DCDC input requirements.

Figure 5-1. External Power Input Connected to Application Supply Rails

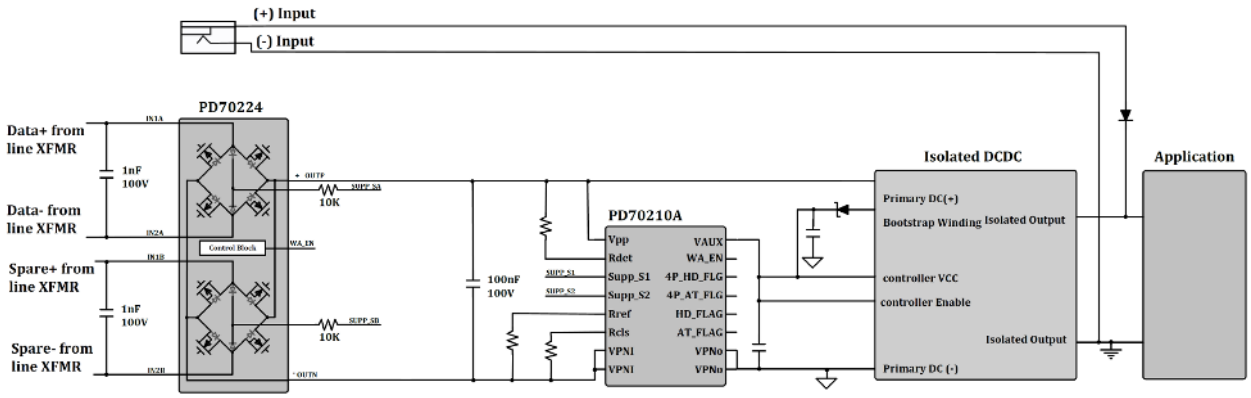
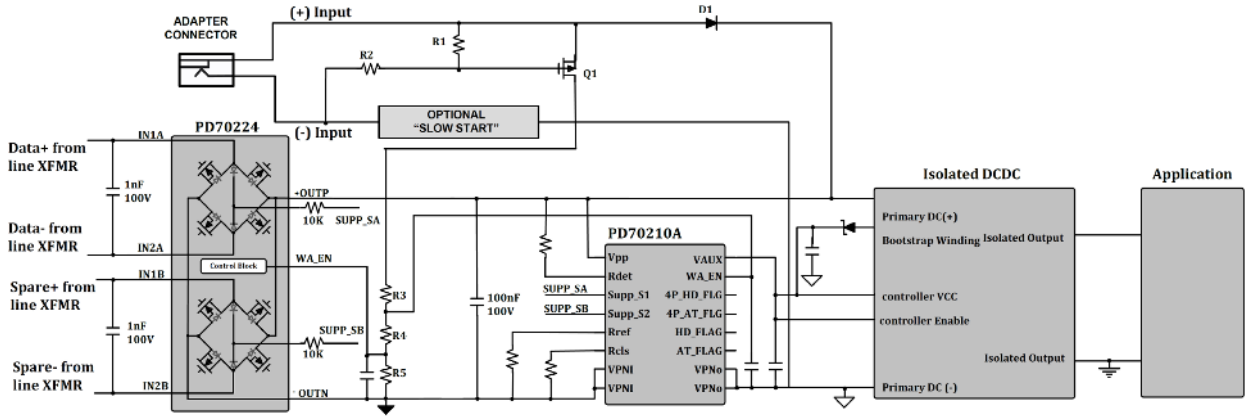


Figure 5-2. External Power Input Connected to PD70210A Output



5.2.1 External Source Connected to PD Device Output

The PD70224 WA_EN pin will be used for protecting the PSE when an external adapter is connected.

In this mode, the risk to PSE side exists when a higher voltage external adapter is hot connected to the system.

When the WA_EN input voltage is higher than its threshold level, PD70224 internal FETs are disabled, converting the device into standard diode bridge.

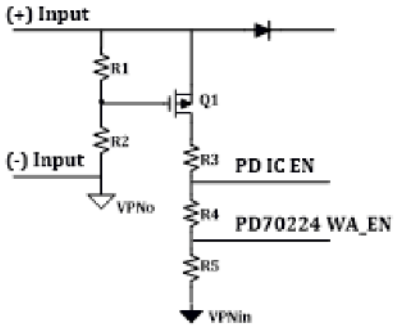
An optional “slow start” circuit prevents adapter jack contact arcing when an adapter is “hot plugged” by limiting its surge current. For the detailed circuit, see AN3472, Implementing Aux Power in PoE.

The PD70210A also has a specific input pin, to disable the isolation switch, when an external adapter is connected.

In this case, WA_EN resistors divider depends on the “turn off” threshold of the PD70210A and PD70224.

Zooming into the resistors to be selected in external adapter connection.

Figure 5-3. External Power Input Resistors Dividers



R1 and R2 sets a rough threshold for PFET Q1 enable to detect whether external adapter exists or not. It should be set to be lower threshold than PD70224 and PD70210A disable levels.

R3, R4, and R5 set PD70210A disable threshold and PD70224 disable threshold.

PD70210A disable threshold should be set so that it will always be lower than PD70224 disable threshold.

1 V is a good choice for the margin between the two.

So, in case of 44 V–57 V external adapter, the disable setting can be selected as follows:

PFET enable threshold = 35 V

PD70224 disable threshold = 43 V

R1 and R2 setting should be so that the value of Q1 VGS < 20 V at max voltage condition of external adapter.

While external adapter voltage is above 35 V, Q1 will be above its VGSth value.

$$VGS = Vext\_adapter \times \frac{R1}{R1 + R2}$$

Suppose VGSth is 3.5 V, thus we will set VGS= 5 V.

R1 is selected as 2 kΩ.

$$R2 = R1 \times \frac{Vext\_adapter - VGS}{VGS}$$

Using R1= 2 kΩ, Vext_adapter= 30 V and VGS= maximum VGSth= 3.5 V. We get R2 value.

$$R2 = 15K\Omega$$

$$= PD70210A\_Wa\_en = Vext\_adapter\_PD70210A \text{ x } \frac{R4}{(R3 + R4)}$$

$$R2 = R1 \times \frac{Vext\_adapter - VGS}{VGS}$$

R3, R4, and R5 are set using the following two equations.

$$(I) \qquad PD70224\_Wa\_en = Vext\_adapter\_PD70224 \text{ x } \frac{R5}{(R3+R4+R5)}$$

$$(II) \qquad PD70210A\_Wa\_en = Vext\_adapter\_PD70210A \text{ x } \frac{R4+R5}{(R3+R4+R5)}$$

Set R3, R4, and R5 up to few KΩ.

At equation (I) set Vext_adapter_PD70224= 44 V and from PD70224 datasheet PD70224 _WA_EN=1. 35 V.

At equation (II) set Vext_adapter_PD70210A= (minimum Vext_adapter_PD70224 -1 V) and from PD_IC data sheet PD70210A_WA_EN= 2.4 V.

R5 is selected as 620.

Solving the two equations plus accuracy and verifying that PD70210A is always disconnected before PD70224, we get the optimum resistors values for an adapter of adapter of 36 V and above.

$$R3 = 15K\Omega$$

$$R4 = 820\Omega$$

$$R5 = 620\Omega$$

6. Design Example

The following four figures show the layout of PD70224 EVB evaluation board.

The board is two layers PCB. U2 is PD70224.

This board can be ordered from Microchip.

Figure 6-1. PD70224 EVB PCB Silk Top

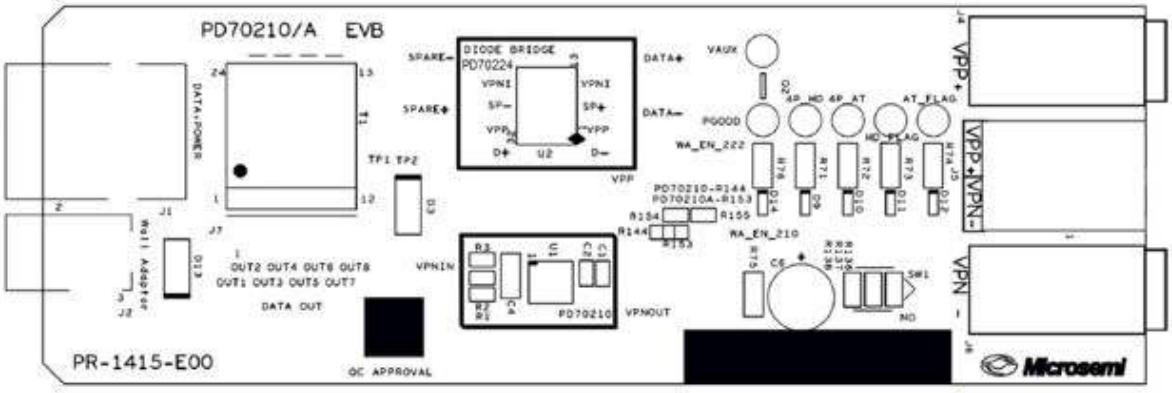


Figure 6-2. PD70224 EVB PCB Silk Bottom

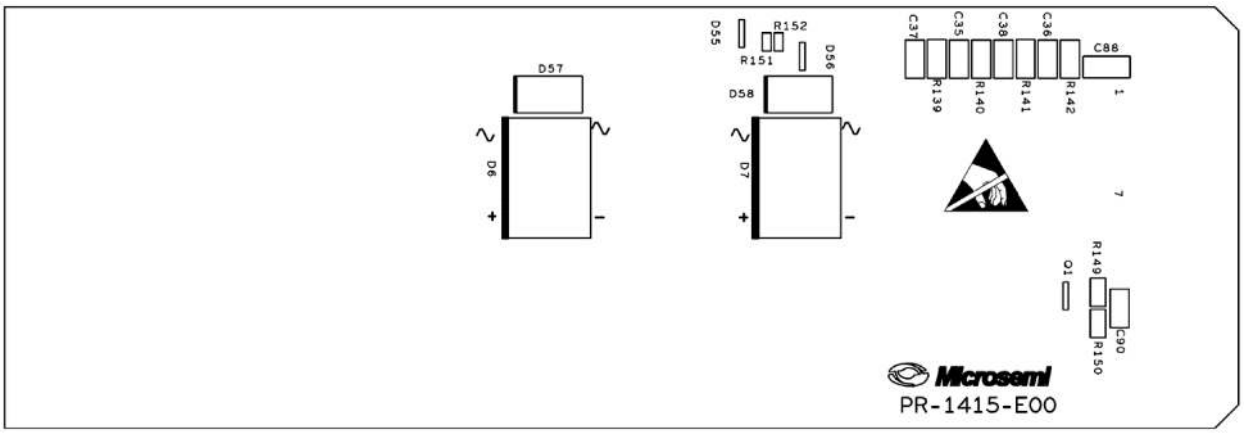


Figure 6-3. PD70224 EVB PCB Top Copper

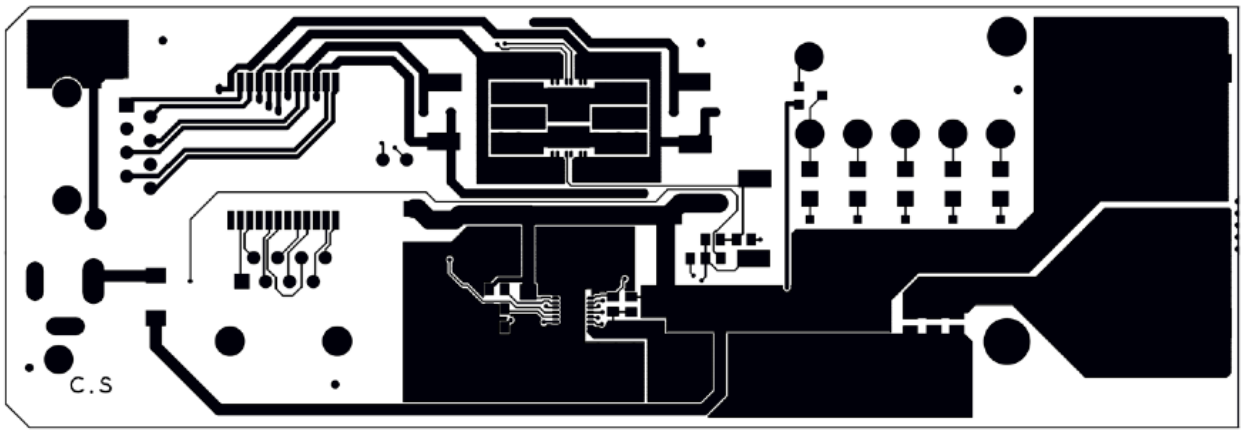
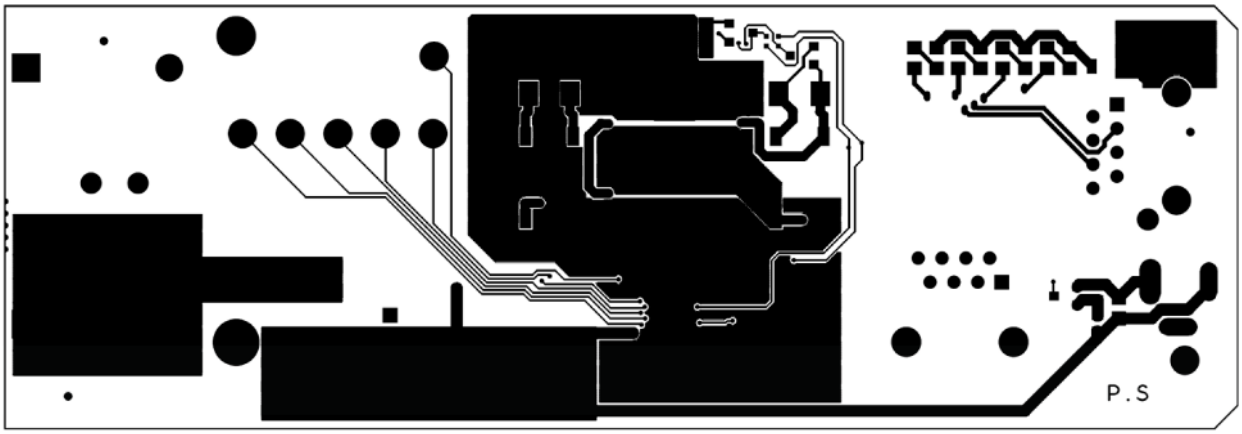


Figure 6-4. PD70224 EVB PCB Bottom Copper



7. Ordering Information

The following table lists the ordering information of the PD70224 device.

Table 7-1. Ordering Information

Part Number	Ambient Temperature	Type	Package	Packaging Type	Part Marking
PD70224ILQ-TR	–40 °C to 85 °C	RoHS compliant Pb free MSL3	QFN (40 lead)	Tape and reel	Microsemi Logo PD70224 ZZ e4[1] YYWWNNN

1. ZZ e4: ZZ= Random character with no meaning, e4 = Second-level interconnect.
2. YY= Year, WW= Week, NNN= Trace code.

8. Revision History

Revision	Date	Description
C	October 2020	Updated a typo for a value of K in the Package Measurements table.
B	September 2020	The following is a summary of changes in revision C of this document. • Updated the Introduction section. • Added Technical Support and Documentation section. • Updated the values of K in the Package Measurements table. • Updated the Internal Construction and Pinout figure. • Updated the 4.3 Recommended PCB Layout section. • Updated the PD70224 EVB PCB Silk Top figure. • Updated the Ordering Information table.
A	July 2020	• Updated to Microchip format. • Updated document number from PD-000307871 to DS00003590. • Deleted figure "PD70224 Bottom Layer Copper and Solder Paste Recommended PCB Layout for Thermal Pad Array (mm)" in the Recommended PCB Layout section.
3.0	August 2019	Updated the package marking in the Ordering Information section.
2.0	February 2018	• Updated part marking. • Updated figure External Power Input Connected to PD70210A Output. • Added MSL3 compliance. • Updated Safe Operating Area graph to show test methodology and discuss protection recommendations. • Moved Recommended Protection Scheme to the application note “Design for PD System Surge Immunity".
1.3	May 2016	Updated Figure 7 with optional slow start circuit.
1.2	November 2014	• Removed watermark. • Updated ESD with IN1A/IN2A 1000 V note.
1.1	July 2015	Updated ESD.
1.0	August 2014	• Added maximum SUPP_Sx current, application information, and SOA graph. • Updated MSL level.
0.73	June 2014	Updated leadframe for thermal pad.
0.72	May 2014	Added dimensions to recommended layout IMAX_LOAD.
0.7	May 2014	Initial Revision

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