LMV2011 High Precision, Rail-to-Rail Output Operational Amplifier

Check for Samples: LMV2011

FEATURES

- **(For Vs = 5V, Typical Unless Otherwise Noted)**
- **Low Ensured V_{os} Over Temperature 35µV**
- **Low Noise with no 1/f 35nV/$\sqrt{Hz}$**
- **High CMRR 130dB**
- **High PSRR 120dB**
- **High A_{VOL} 130dB**
- **Wide Gain-Bandwidth Product 3MHz**
- **High Slew Rate 4V/µs**
- **Low Supply Current 930µA**
- **Rail-to-Rail Output 30mV**
- **No External Capacitors Required**

APPLICATIONS

- **Precision Instrumentation Amplifiers**
- **Thermocouple Amplifiers**
- **Strain Gauge Bridge Amplifier**

DESCRIPTION

The LMV2011 is a new precision amplifier that offers unprecedented accuracy and stability at an affordable price and is offered in a miniature (5-pin SOT-23) package and in an 8-lead SOIC package. This device utilizes patented techniques to measure and continually correct the input offset error voltage. The result is an amplifier which is ultra stable over time and temperature. It has excellent CMRR and PSRR ratings, and does not exhibit the familiar 1/f voltage and current noise increase that plagues traditional amplifiers. The combination of the LMV2011 characteristics makes it a good choice for transducer amplifiers, high gain configurations, ADC buffer amplifiers, DAC I-V conversion, and any other 2.7V-5V application requiring precision and long term stability.

Other useful benefits of the LMV2011 are rail-to-rail output, a low supply current of 930µA, and wide gain-bandwidth product of 3MHz. These extremely versatile features found in the LMV2011 provide high performance and ease of use.

Connection Diagrams

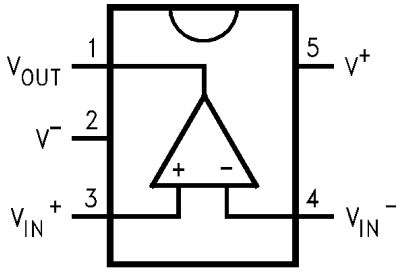

Figure 1. 5-Pin SOT-23 (Top View)
See DBV Package

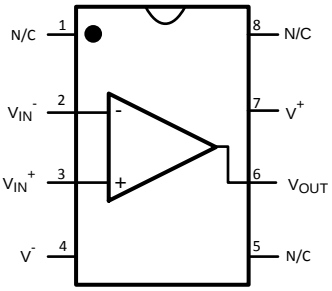

Figure 2. 8-Pin SOIC (Top View)
See D Package

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance	Human Body Model	2000V
	Machine Model	200V
	Supply Voltage	5.5V
Common-Mode Input Voltage		$-0.3 \le V_{CM} \le V_{CC} +0.3V$
Differential Input Voltage		± Supply Voltage
Current At Input Pin		30mA
Current At Output Pin		30mA
Current At Power Supply Pin		50mA
Junction Temperature (T_J)		150°C
Lead Temperature (soldering 10 sec.)		+300°C

(1) Absolute Maximum Ratings indicate limits beyond which damage may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Operating Ratings(1)

Supply Voltage	2.7V to 5.25V
Storage Temperature Range	−65°C to 150°C
Operating Temperature Range	0°C to 70°C

(1) Absolute Maximum Ratings indicate limits beyond which damage may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and test conditions, see the Electrical Characteristics.

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7V, V^-= 0V, V_{CM} = 1.35V, V_O = 1.35V and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage			0.8	25 **35**	µV
	Offset Calibration Time			0.5	10 **12**	ms
TCV_{OS}	Input Offset Voltage			0.015		µV/°C
	Long-Term Offset Drift			0.006		µV/month
	Lifetime V_{OS} Drift			2.5	5	µV
I_{IN}	Input Current			-3		pA
I_{OS}	Input Offset Current			6		pA
R_{IND}	Input Differential Resistance			9		MΩ
CMRR	Common Mode Rejection Ratio	$-0.3 \le V_{CM} \le 0.9V$ $0 \le V_{CM} \le 0.9V$		130	95 **90**	dB
PSRR	Power Supply Rejection Ratio	$2.7V \le V^+ \le 5V$		120	95 **90**	dB
A_{VOL}	Open Loop Voltage Gain	R_L = 10kΩ		130	95 **90**	dB
		R_L = 2kΩ		124	90 **85**	
V_O	Output Swing	R_L = 10kΩ to 1.35V V_{IN}(diff) = ±0.5V	2.665 **2.655**	2.68		V
				0.033	0.060 **0.075**	
		R_L = 2kΩ to 1.35V V_{IN}(diff) = ±0.5V	2.630 **2.615**	2.65		V
				0.061	0.085 **0.105**	

2.7V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7V, V^-= 0V, V_{CM} = 1.35V, V_O = 1.35V and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_O	Output Current	Sourcing, V_O = 0V V_{IN}(diff) = ±0.5V		12	5 **3**	mA
		Sinking, V_O = 5V V_{IN}(diff) = ±0.5V		18	5 **3**	
R_{OUT}	Output Impedance			0.05		Ω
I_S	Supply Current			0.919	1.20 **1.50**	mA

2.7V AC Electrical Characteristics

T_J = 25°C, V^+ = 2.7V, V^-= 0V, V_{CM} = 1.35V, V_O = 1.35V, and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
GBW	Gain-Bandwidth Product				3		MHz
SR	Slew Rate				4		V/µs
θ_m	Phase Margin				60		Deg
G_m	Gain Margin				−14		dB
e_n	Input-Referred Voltage Noise				35		nV/√Hz
i_n	Input-Referred Current Noise				150		fA/√Hz
e_np-p	Input-Referred Voltage Noise	R_S = 100Ω, DC to 10Hz			850		nV_{pp}
t_{rec}	Input Overload Recovery Time				50		ms
t_s	Output Settling Time	A_V = −1, R_L = 2kΩ 1V Step	1%		0.9		µs
			0.1%		49		
			0.01%		100		

5V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5V, V^-= 0V, V_{CM} = 2.5V, V_O = 2.5V and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage			0.12	25 **35**	µV
	Offset Calibration Time			0.5	10 **12**	ms
TCV_{OS}	Input Offset Voltage			0.015		µV/°C
	Long-Term Offset Drift			0.006		µV/month
	Lifetime V_{OS} Drift			2.5	5	µV
I_{IN}	Input Current			-3		pA
I_{OS}	Input Offset Current			6		pA
R_{IND}	Input Differential Resistance			9		MΩ
CMRR	Common Mode Rejection Ratio	−0.3 ≤ V_{CM} ≤ 3.2 0 ≤ V_{CM} ≤ 3.2		130	100 **90**	dB
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V		120	95 **90**	dB
A_{VOL}	Open Loop Voltage Gain	R_L = 10kΩ		130	105 **100**	dB
		R_L = 2kΩ		132	95 **90**	

5V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_O = 2.5V and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_O	Output Swing	R_L = 10kΩ to 2.5V V_{IN}(diff) = ±0.5V	4.96 **4.95**	4.978		V
				0.040	0.070 **0.085**	
		R_L = 2kΩ to 2.5V V_{IN}(diff) = ±0.5V	4.895 **4.875**	4.919		V
				0.091	0.115 **0.140**	
I_O	Output Current	Sourcing, V_O = 0V V_{IN}(diff) = ±0.5V		15	8 **6**	mA
		Sinking, V_O = 5V V_{IN}(diff) = ±0.5V		17	8 **6**	
R_{OUT}	Output Impedance			0.05		Ω
I_S	Supply Current per Channel			0.930	1.20 **1.50**	mA

5V AC Electrical Characteristics

T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_O = 2.5V, and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
GBW	Gain-Bandwidth Product				3		MHz
SR	Slew Rate				4		V/µs
θ_m	Phase Margin				60		deg
G_m	Gain Margin				−15		dB
e_n	Input-Referred Voltage Noise				35		nV/√Hz
i_n	Input-Referred Current Noise				150		fA/√Hz
e_np-p	Input-Referred Voltage Noise	R_S = 100Ω, DC to 10Hz			850		nV_{pp}
t_{rec}	Input Overload Recovery Time				50		ms
t_s	Output Settling Time	A_V = −1, R_L = 2kΩ 1V Step	1%		0.8		us
			0.1%		36		
			0.01%		100		

Typical Performance Characteristics

T_A=25C, V_S= 5V unless otherwise specified.

Supply Current vs. Supply Voltage

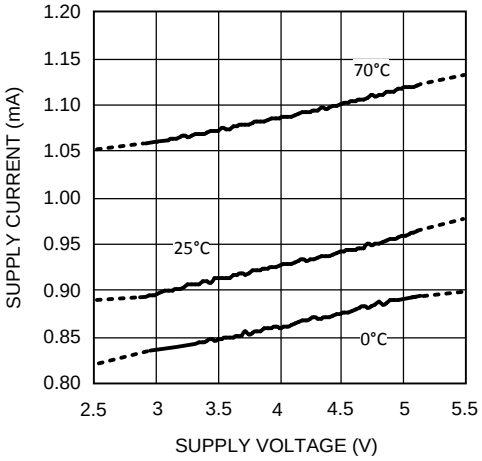

Figure 3.

Offset Voltage vs. Supply Voltage

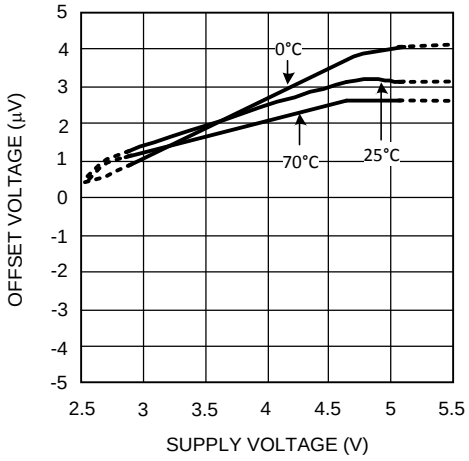

Figure 4.

Offset Voltage vs. Common Mode

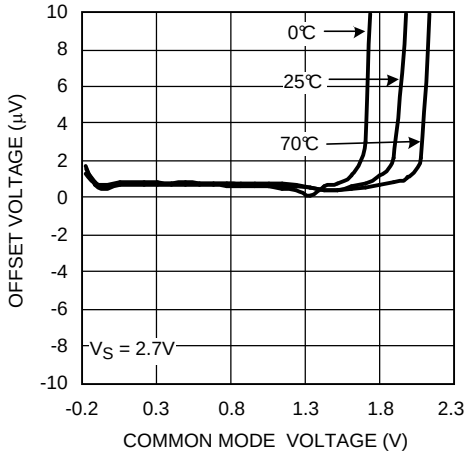

Figure 5.

Offset Voltage vs. Common Mode

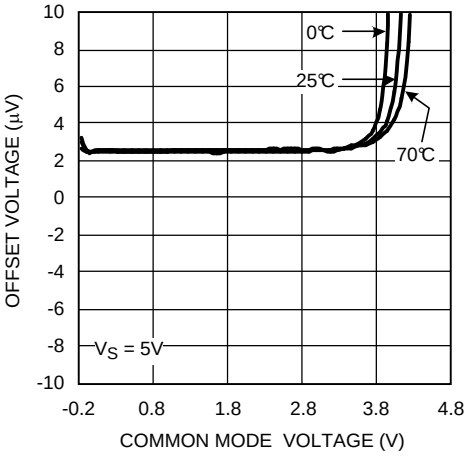

Figure 6.

Voltage Noise vs. Frequency

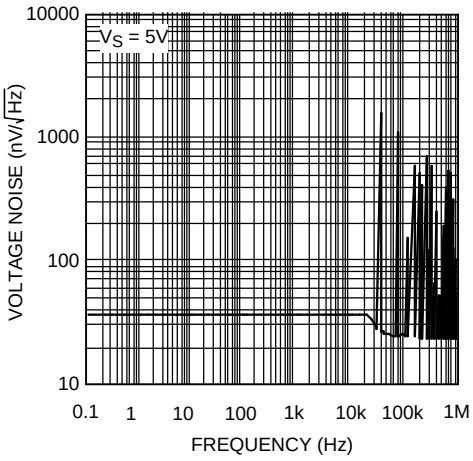

Figure 7.

Input Bias Current vs. Common Mode

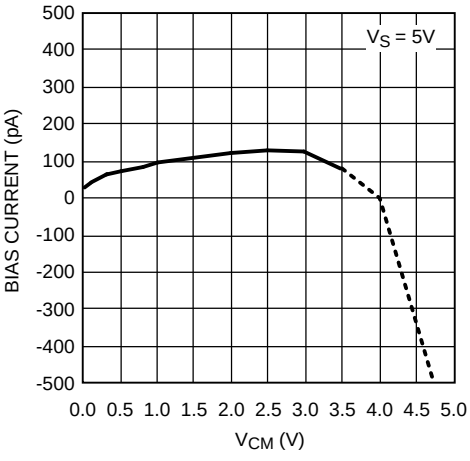

Figure 8.

Typical Performance Characteristics (continued)

T_A=25C, V_S= 5V unless otherwise specified.

PSRR vs. Frequency

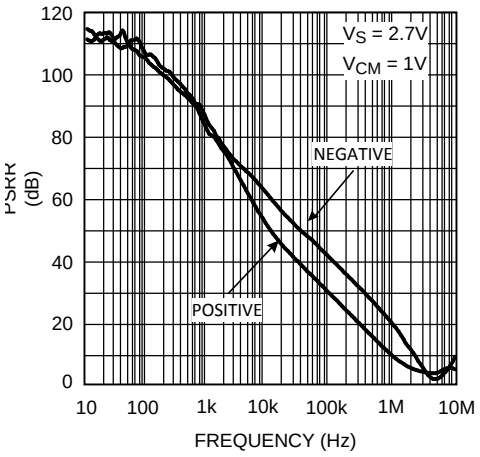

Figure 9.

PSRR vs. Frequency

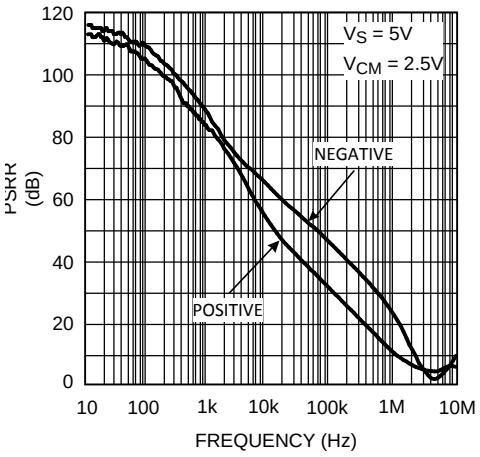

Figure 10.

Output Sourcing @ 2.7V

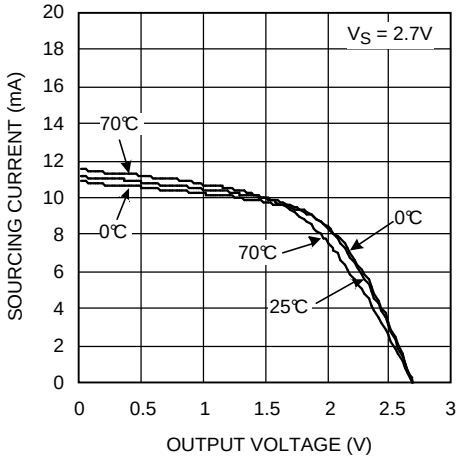

Figure 11.

Output Sourcing @ 5V

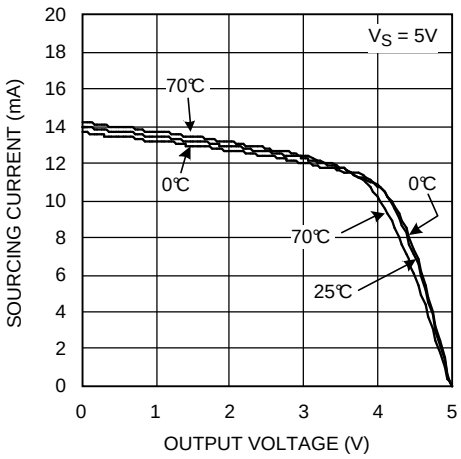

Figure 12.

Output Sinking @ 2.7V

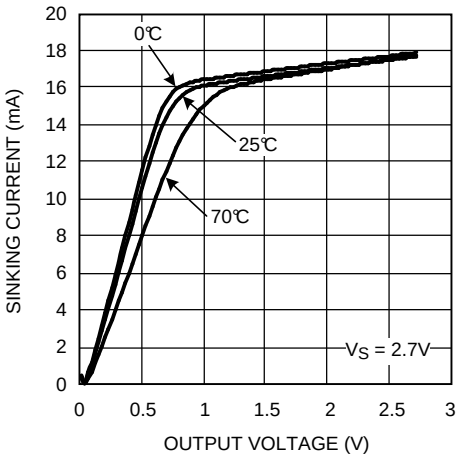

Figure 13.

Output Sinking @ 5V

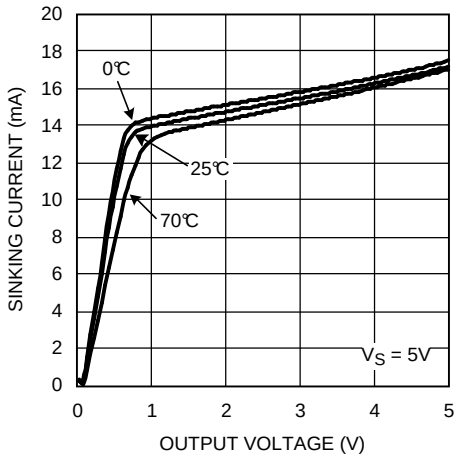

Figure 14.

Typical Performance Characteristics (continued)

T_A=25C, V_S= 5V unless otherwise specified.

Max Output Swing vs. Supply Voltage

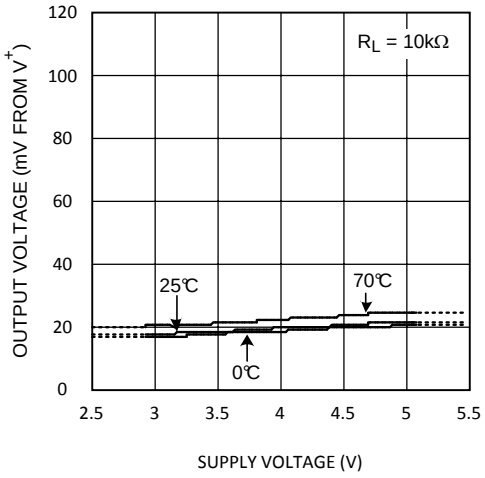

Figure 15.

Max Output Swing vs. Supply Voltage

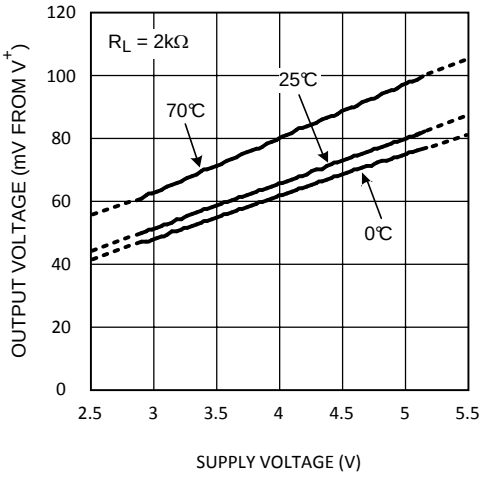

Figure 16.

Min Output Swing vs. Supply Voltage

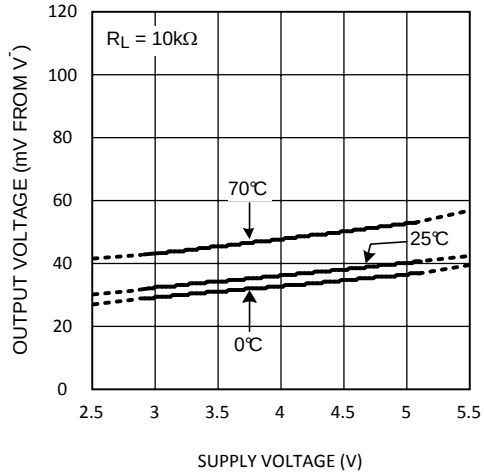

Figure 17.

Min Output Swing vs. Supply Voltage

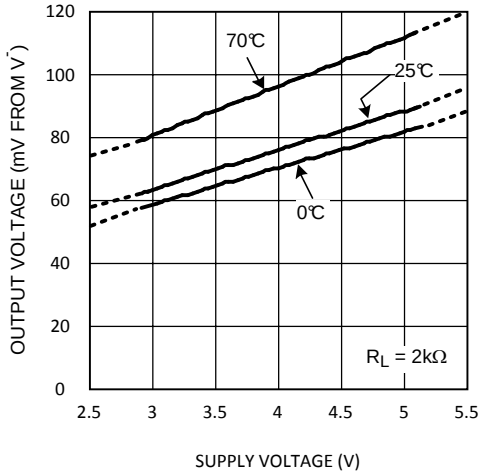

Figure 18.

CMRR vs. Frequency

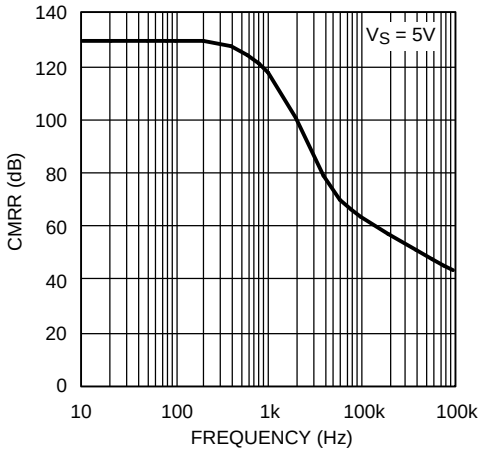

Figure 19.

Open Loop Gain and Phase vs. Supply Voltage

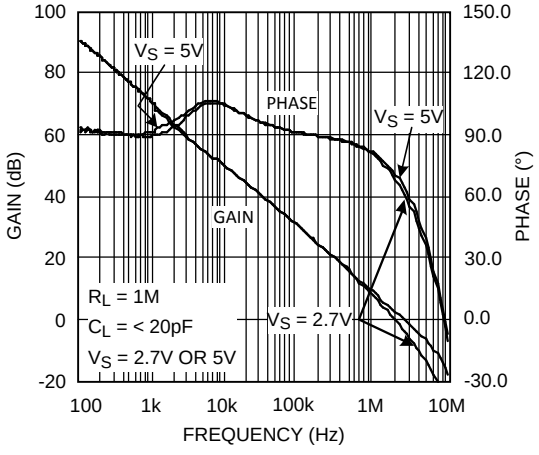

Figure 20.

Typical Performance Characteristics (continued)

T_A=25C, V_S= 5V unless otherwise specified.

Open Loop Gain and Phase vs. R_L @ 2.7V

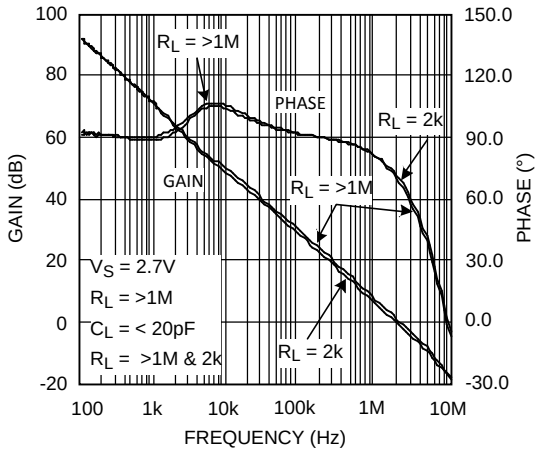

Figure 21.

Open Loop Gain and Phase vs. R_L @ 5V

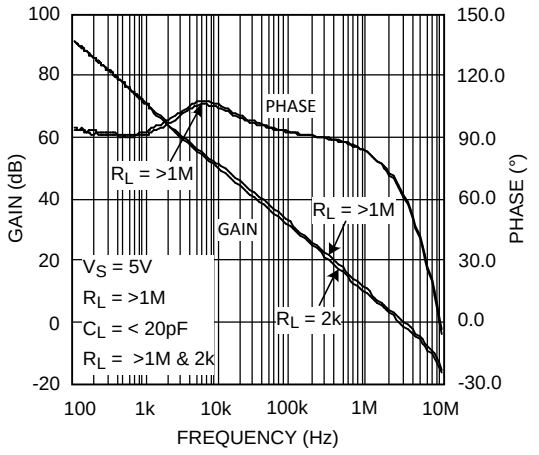

Figure 22.

Open Loop Gain and Phase vs. C_L @ 2.7V

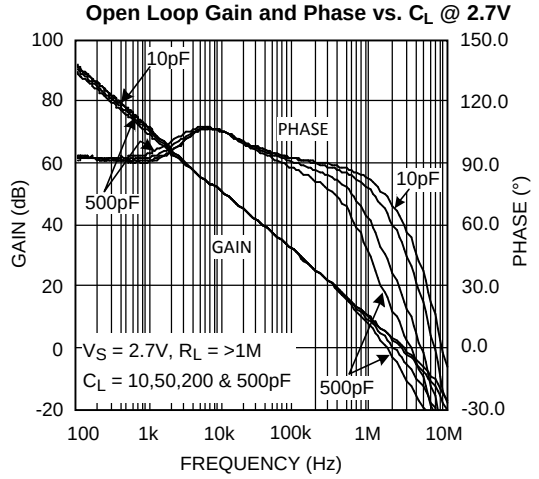

Figure 23.

Open Loop Gain and Phase vs. C_L @ 5V

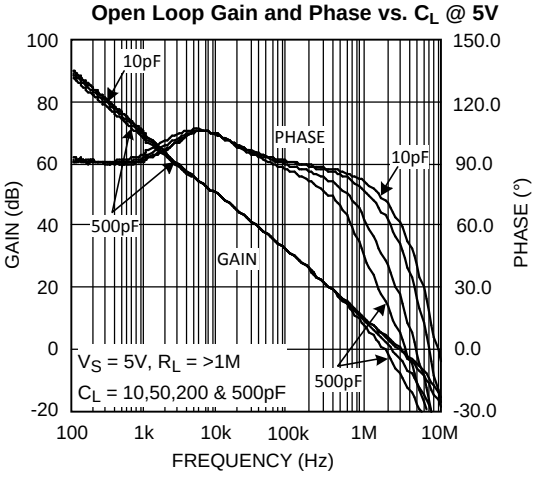

Figure 24.

Open Loop Gain and Phase vs. Temperature @ 2.7V

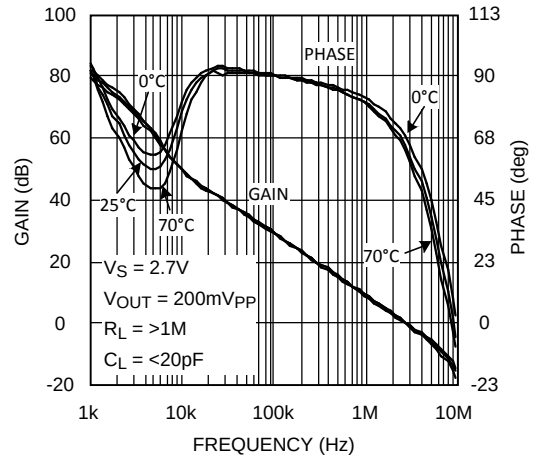

Figure 25.

Open Loop Gain and Phase vs. Temperature @ 5V

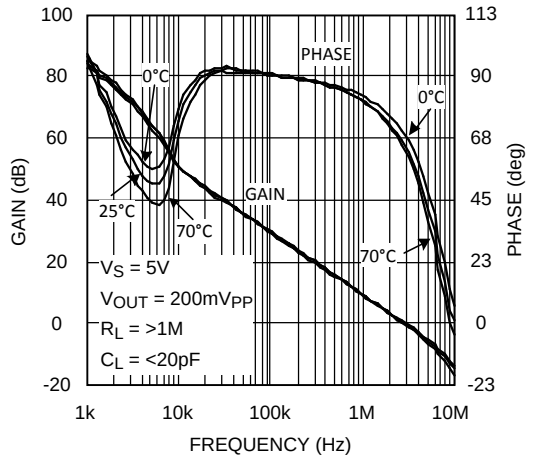

Figure 26.

Typical Performance Characteristics (continued)

T_A=25C, V_S= 5V unless otherwise specified.

THD+N vs. AMPL

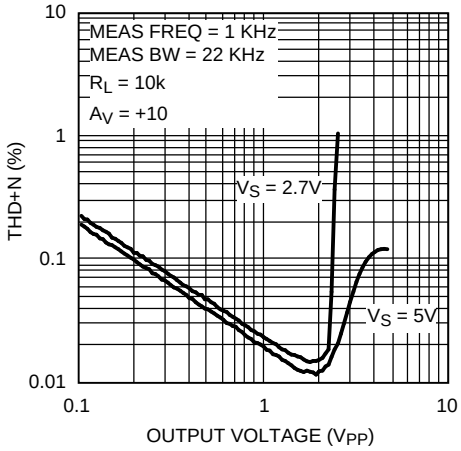

Figure 27.

THD+N vs. Frequency

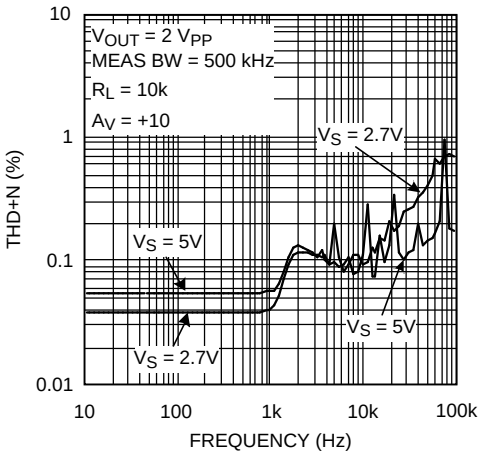

Figure 28.

0.1Hz − 10Hz Noise vs. Time

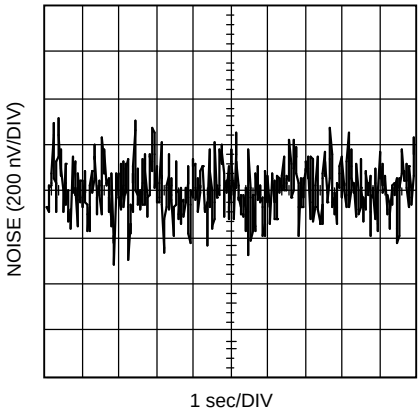

Figure 29.

APPLICATION INFORMATION

THE BENEFITS OF LMV2011 NO 1/f NOISE

Using patented methods, the LMV2011 eliminates the 1/f noise present in other amplifiers. That noise, which increases as frequency decreases, is a major source of measurement error in all DC-coupled measurements. Low-frequency noise appears as a constantly-changing signal in series with any measurement being made. As a result, even when the measurement is made rapidly, this constantly-changing noise signal will corrupt the result. The value of this noise signal can be surprisingly large. For example: If a conventional amplifier has a flat-band noise level of 10nV/$\sqrt{Hz}$ and a noise corner of 10Hz, the RMS noise at 0.001Hz is 1µV/$\sqrt{Hz}$. This is equivalent to a 0.50µV peak-to-peak error, in the frequency range 0.001 Hz to 1.0 Hz. In a circuit with a gain of 1000, this produces a 0.50mV peak-to-peak output error. This number of 0.001 Hz might appear unreasonably low, but when a data acquisition system is operating for 17 minutes, it has been on long enough to include this error. In this same time, the LMV2011 will only have a 0.21mV output error. This is smaller by 2.4 x. Keep in mind that this 1/f error gets even larger at lower frequencies. At the extreme, many people try to reduce this error by integrating or taking several samples of the same signal. This is also doomed to failure because the 1/f nature of this noise means that taking longer samples just moves the measurement into lower frequencies where the noise level is even higher.

The LMV2011 eliminates this source of error. The noise level is constant with frequency so that reducing the bandwidth reduces the errors caused by noise.

Another source of error that is rarely mentioned is the error voltage caused by the inadvertent thermocouples created when the common "Kovar type" IC package lead materials are soldered to a copper printed circuit board. These steel-based leadframe materials can produce over 35µV/°C when soldered onto a copper trace. This can result in thermocouple noise that is equal to the LMV2011 noise when there is a temperature difference of only 0.0014°C between the lead and the board!

For this reason, the lead-frame of the LMV2011 is made of copper. This results in equal and opposite junctions which cancel this effect. The extremely small size of the SOT-23 package results in the leads being very close together. This further reduces the probability of temperature differences and hence decreases thermal noise.

OVERLOAD RECOVERY

The LMV2011 recovers from input overload much faster than most chopper-stabilized opamps. Recovery from driving the amplifier to 2X the full scale output, only requires about 40ms. Many chopper-stabilized amplifiers will take from 250ms to several seconds to recover from this same overload. This is because large capacitors are used to store the unadjusted offset voltage.

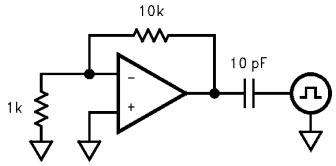

Figure 30. Overload Recovery Test

The wide bandwidth of the LMV2011 enhances performance when it is used as an amplifier to drive loads that inject transients back into the output. ADCs (Analog-to-Digital Converters) and multiplexers are examples of this type of load. To simulate this type of load, a pulse generator producing a 1V peak square wave was connected to the output through a 10pF capacitor (Figure 30). The typical time for the output to recover to 1% of the applied pulse is 80ns. To recover to 0.1% requires 860ns. This rapid recovery is due to the wide bandwidth of the output stage and large total GBW.

NO EXTERNAL CAPACITORS REQUIRED

The LMV2011 does not need external capacitors. This eliminates the problems caused by capacitor leakage and dielectric absorption, which can cause delays of several seconds from turn-on until the amplifier's error has settled.

MORE BENEFITS

The LMV2011 offers the benefits mentioned above and more. It has a rail-to-rail output and consumes only 950µA of supply current while providing excellent DC and AC electrical performance. In DC performance, the LMC2001 achieves 130dB of CMRR, 120dB of PSRR and 130dB of open loop gain. In AC performance, the LMV2011 provides 3MHz of gain-bandwidth product and 4V/µs of slew rate.

HOW THE LMV2011 WORKS

The LMV2011 uses new, patented techniques to achieve the high DC accuracy traditionally associated with chopper-stabilized amplifiers without the major drawbacks produced by chopping. The LMV2011 continuously monitors the input offset and corrects this error. The conventional chopping process produces many mixing products, both sums and differences, between the chopping frequency and the incoming signal frequency. This mixing causes large amounts of distortion, particularly when the signal frequency approaches the chopping frequency. Even without an incoming signal, the chopper harmonics mix with each other to produce even more trash. If this sounds unlikely or difficult to understand, look at the plot (Figure 31), of the output of a typical (MAX432) chopper-stabilized opamp. This is the output when there is no incoming signal, just the amplifier in a gain of -10 with the input grounded. The chopper is operating at about 150Hz; the rest is mixing products. Add an input signal and the noise gets much worse. Compare this plot with Figure 32 of the LMV2011. This data was taken under the exact same conditions. The auto-zero action is visible at about 30kHz but note the absence of mixing products at other frequencies. As a result, the LMV2011 has very low distortion of 0.02% and very low mixing products.

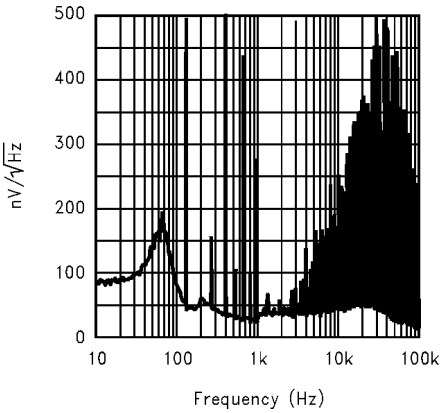

Figure 31. The Output of a Chopper Stabilized Op Amp (MAX432)

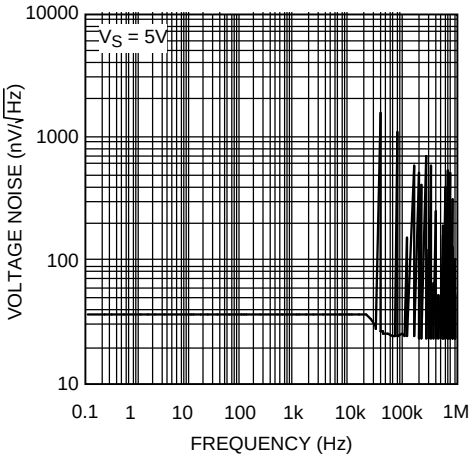

Figure 32. The Output of the LMV2011

INPUT CURRENTS

The LMV2011's input currents are different than standard bipolar or CMOS input currents in that it appears as a current flowing in one input and out the other. Under most operating conditions, these currents are in the picoamp level and will have little or no effect in most circuits. These currents tend to increase slightly when the common-mode voltage is near the minus supply (See the Typical Performance Characteristics). At high temperatures such as 85°C, the input currents become larger, 0.5nA typical, and are both positive except when the V_{CM} is near V^-. If operation is expected at low common-mode voltages and high temperature, do not add resistance in series with the inputs to balance the impedances. Doing this can cause an increase in offset voltage. A small resistance such as 1kΩ can provide some protection against very large transients or overloads, and will not increase the offset significantly.

PRECISION STRAIN-GAUGE AMPLIFIER

This Strain-Gauge amplifier (Figure 32) provides high gain (1006 or ~60 dB) with very low offset and drift. Using the resistors' tolerances as shown, the worst case CMRR will be greater than 108 dB. The CMRR is directly related to the resistor mismatch. The rejection of common-mode error, at the output, is independent of the differential gain, which is set by R3. The CMRR is further improved, if the resistor ratio matching is improved, by specifying tighter-tolerance resistors, or by trimming.

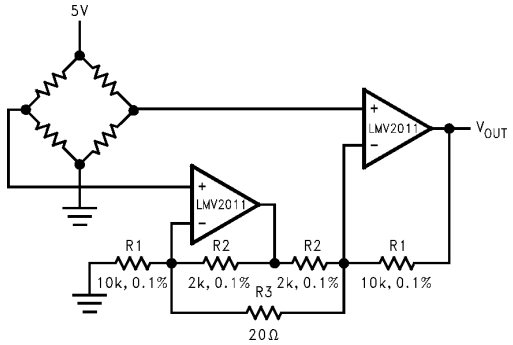

Figure 33. Precision Strain Gauge Amplifier

Extending Supply Voltages and Output Swing by Using a Composite Amplifier Configuration:

In cases where substantially higher output swing is required with higher supply voltages, arrangements like the ones shown in Figure 34 and Figure 35 could be used. These configurations utilize the excellent DC performance of the LMV2011 while at the same time allow the superior voltage and frequency capabilities of the LM6171 to set the dynamic performance of the overall amplifier. For example, it is possible to achieve ±12V output swing with 300MHz of overall GBW (A_V = 100) while keeping the worst case output shift due to V_{OS} less than 4mV. The LMV2011 output voltage is kept at about mid-point of its overall supply voltage, and its input common mode voltage range allows the V- terminal to be grounded in one case (Figure 34, inverting operation) and tied to a small non-critical negative bias in another (Figure 35, non-inverting operation). Higher closed-loop gains are also possible with a corresponding reduction in realizable bandwidth. Table 1 shows some other closed loop gain possibilities along with the measured performance in each case.

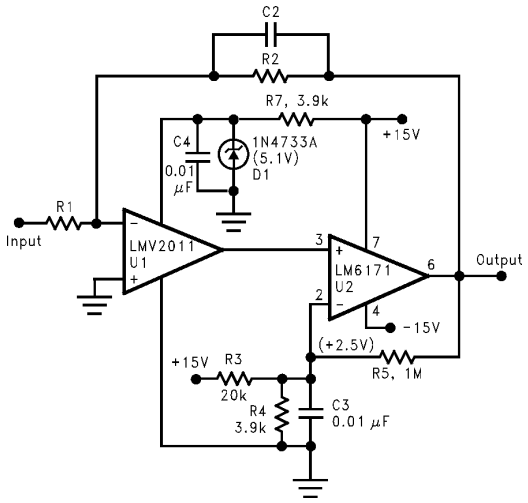

Figure 34. Composite Amplifier Configuration

Table 1. Composite Amplifier Measured Performance

A_V	R1 (Ω)	R2 (Ω)	C2 (pF)	BW (MHz)	SR (V/µs)	en p-p (mV_{PP})
50	200	10k	8	3.3	178	37
100	100	10k	10	2.5	174	70
100	1k	100k	0.67	3.1	170	70
500	200	100k	1.75	1.4	96	250
1000	100	100k	2.2	0.98	64	400

In terms of the measured output peak-to-peak noise, the following relationship holds between output noise voltage, e_n p-p, for different closed-loop gain, A_V, settings, where −3dB Bandwidth is BW:

$$\frac{e_{npp1}}{e_{npp2}} = \sqrt{\frac{BW1}{BW2}} \bullet \frac{A_V1}{A_V2} \quad (1)$$

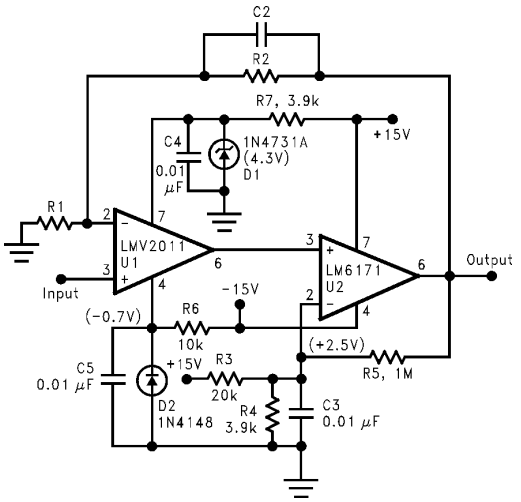

Figure 35. Composite Amplifier Configuration

It should be kept in mind that in order to minimize the output noise voltage for a given closed-loop gain setting, one could minimize the overall bandwidth. As can be seen from Equation 1 above, the output noise has a square-root relationship to the Bandwidth.

In the case of the inverting configuration, it is also possible to increase the input impedance of the overall amplifier, by raising the value of R1, without having to increase the feed-back resistor, R2, to impractical values, by utilizing a "Tee" network as feedback. See the LMC6442 data sheet (Application Notes section) for more details on this.

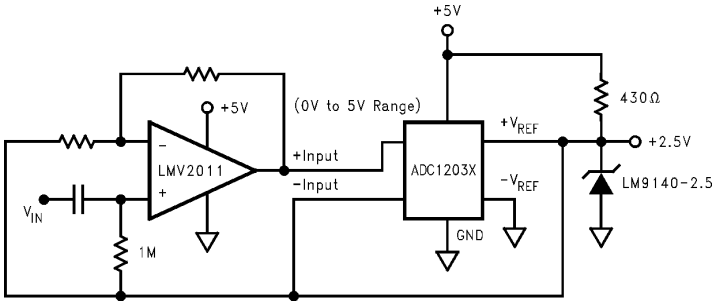

Figure 36. AC Coupled ADC Driver

LMV2011 AS ADC INPUT AMPLIFIER

The LMV2011 is a great choice for an amplifier stage immediately before the input of an ADC (Analog-to-Digital Converter), whether AC or DC coupled. See Figure 36 and Figure 37. This is because of the following important characteristics:

A) Very low offset voltage and offset voltage drift over time and temperature allow a high closed-loop gain setting without introducing any short-term or long-term errors. For example, when set to a closed-loop gain of 100 as the analog input amplifier for a 12-bit A/D converter, the overall conversion error over full operation temperature and 30 years life of the part (operating at 50°C) would be less than 5 LSBs.

B) Fast large-signal settling time to 0.01% of final value (1.4µs) allows 12 bit accuracy at 100KH$_Z$ or more sampling rate.

C) No flicker (1/f) noise means unsurpassed data accuracy over any measurement period of time, no matter how long. Consider the following opamp performance, based on a typical low-noise, high-performance commercially-available device, for comparison:
Opamp flatband noise = 8nV/√Hz
1/f corner frequency = 100Hz
A_V = 2000
Measurement time = 100 sec
Bandwidth = 2Hz
This example will result in about 2.2 mV$_{PP}$ (1.9 LSB) of output noise contribution due to the opamp alone, compared to about 594µV$_{PP}$ (less than 0.5 LSB) when that opamp is replaced with the LMV2011 which has no 1/f contribution. If the measurement time is increased from 100 seconds to 1 hour, the improvement realized by using the LMV2011 would be a factor of about 4.8 times (2.86mV$_{PP}$ compared to 596µV when LMV2011 is used) mainly because the LMV2011 accuracy is not compromised by increasing the observation time.

D) Copper leadframe construction minimizes any thermocouple effects which would degrade low level/high gain data conversion application accuracy (see THE BENEFITS OF LMV2011 NO 1/f NOISE).

E) Rail-to-Rail output swing maximizes the ADC dynamic range in 5-Volt single-supply converter applications. Below are some typical block diagrams showing the LMV2011 used as an ADC amplifier (Figure 36 and Figure 37).

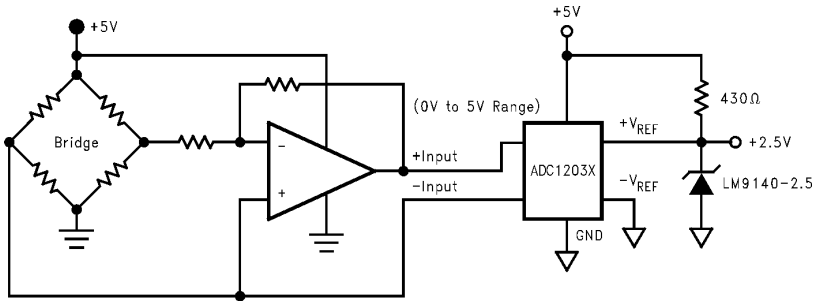

Figure 37. DC Coupled ADC Driver

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV2011MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	LMV20 11MA	Samples
LMV2011MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	LMV20 11MA	Samples
LMV2011MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	A84A	Samples
LMV2011MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	A84A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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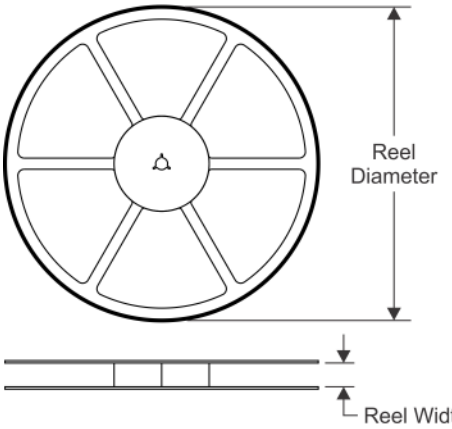
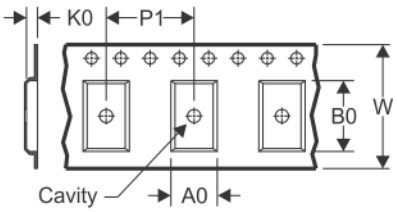
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

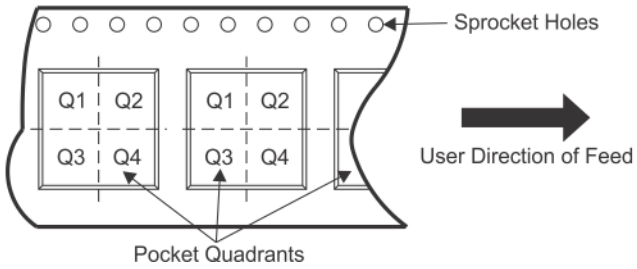


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

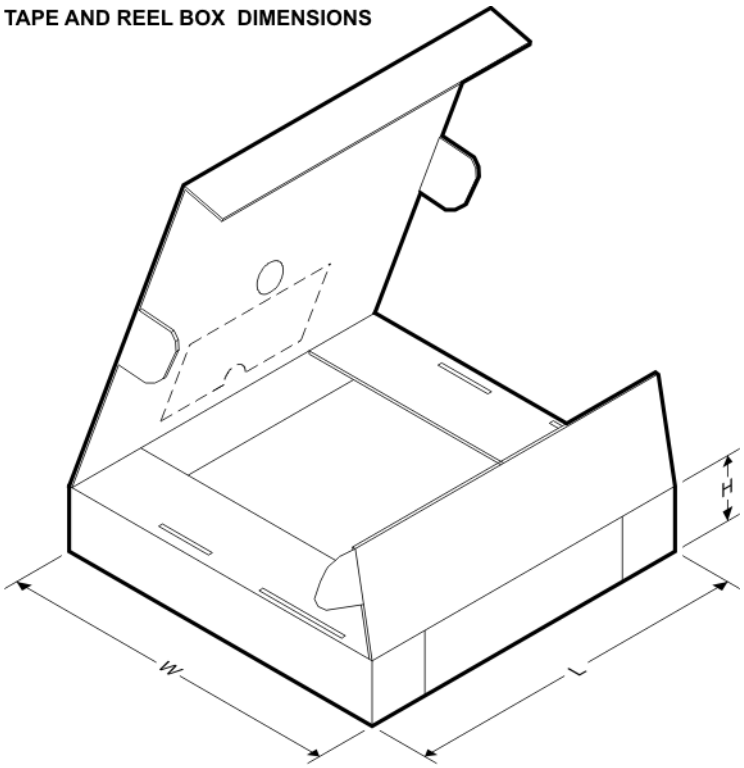
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV2011MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV2011MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV2011MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

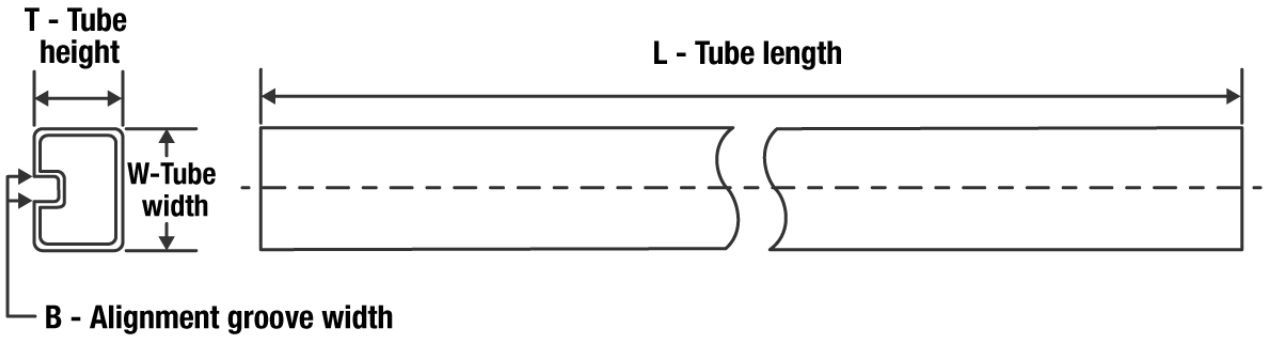
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV2011MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV2011MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV2011MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

TUBE



*All dimensions are nominal

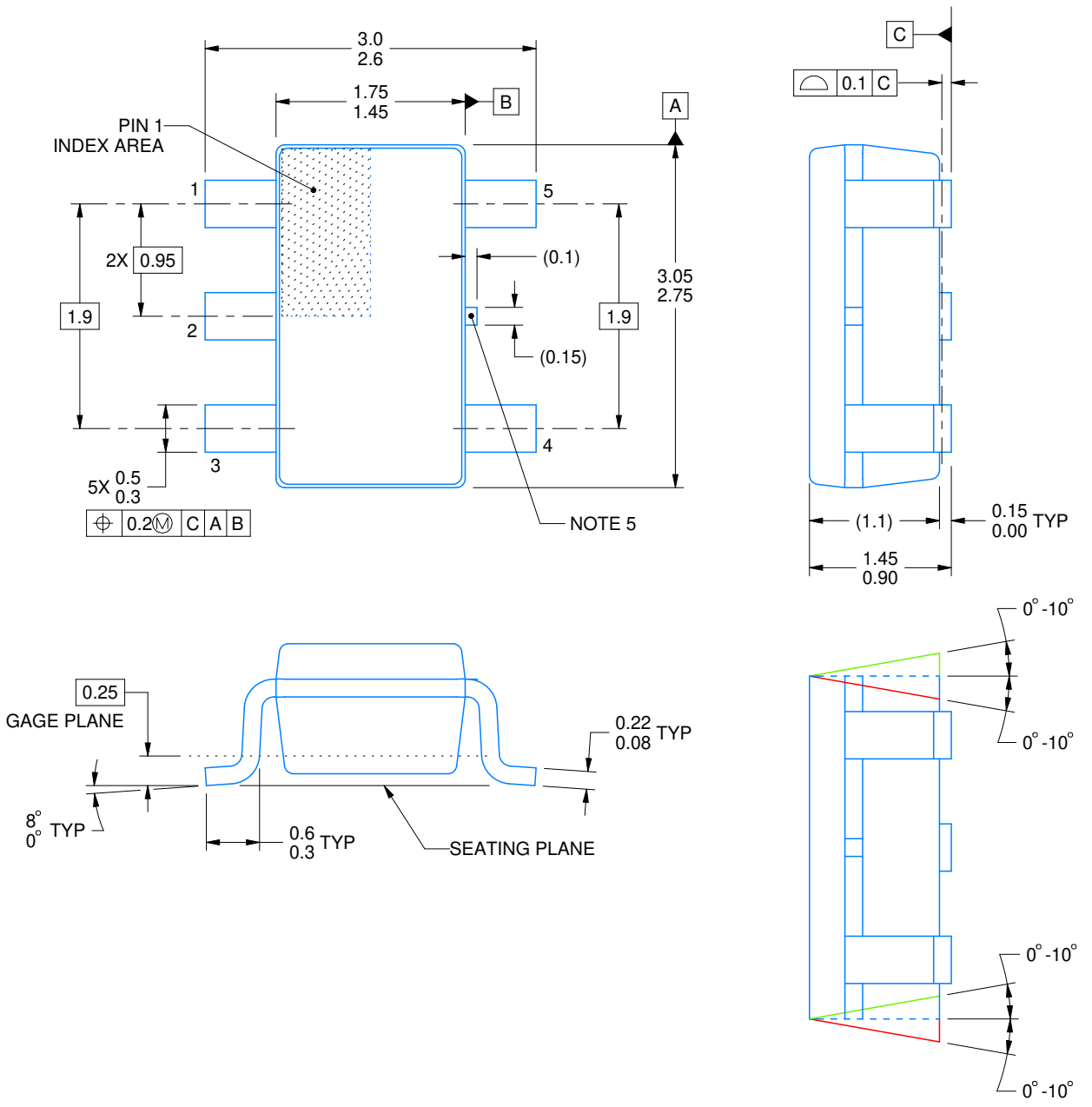
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMV2011MA/NOPB	D	SOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

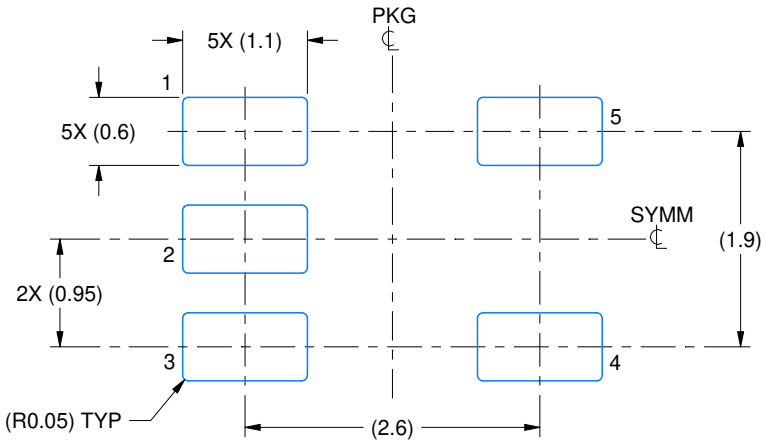


ALTERNATIVE PACKAGE SINGULATION VIEW

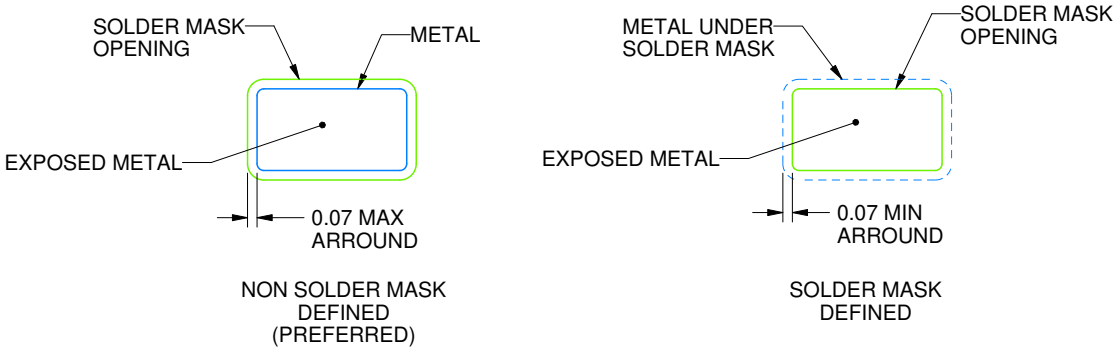
4214839/H 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

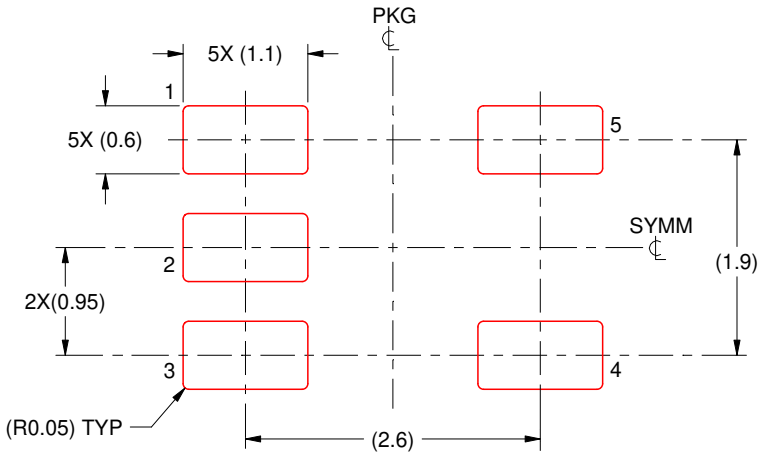


SOLDER MASK DETAILS

4214839/H 09/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

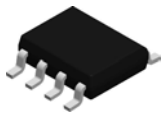


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/H 09/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

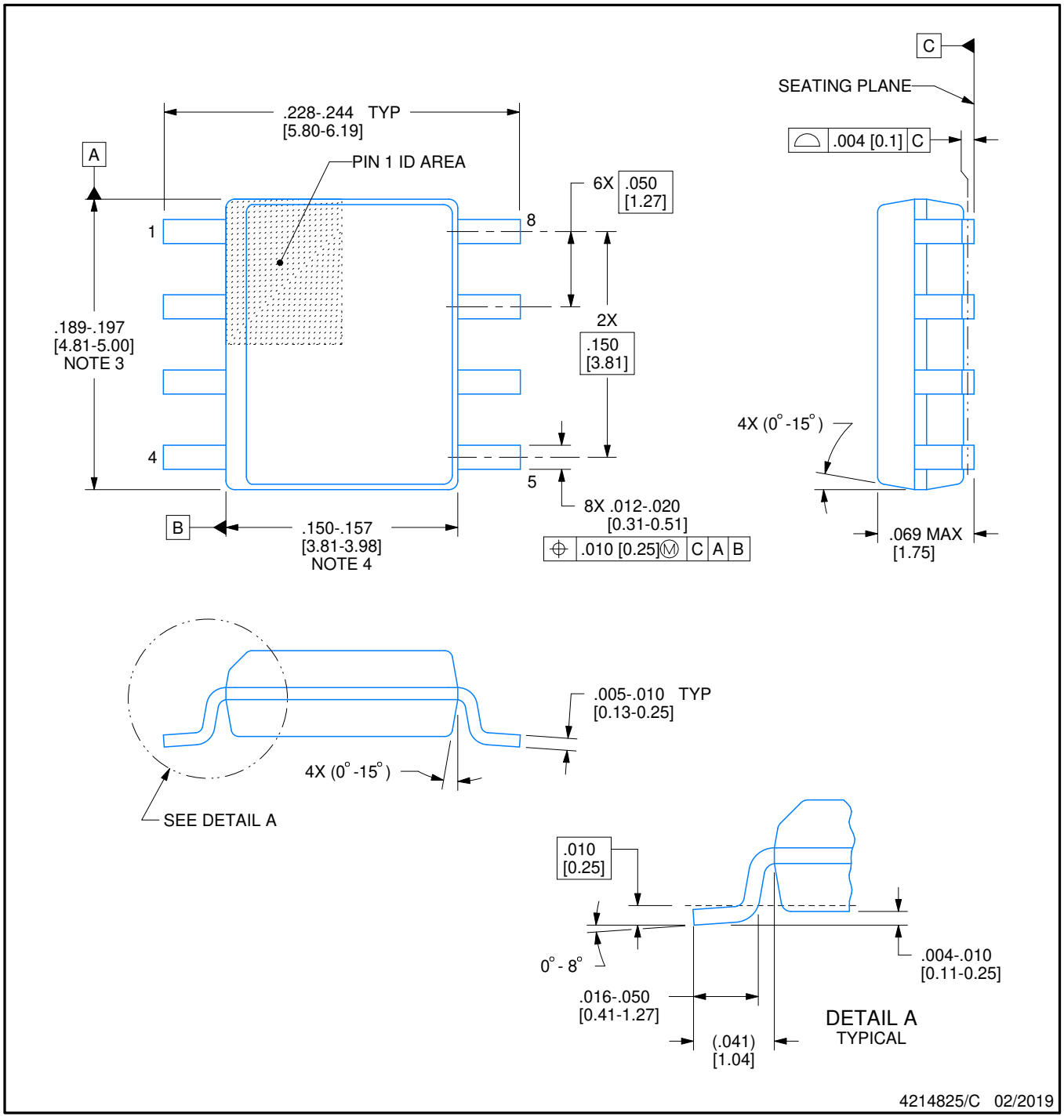


PACKAGE OUTLINE

D0008A

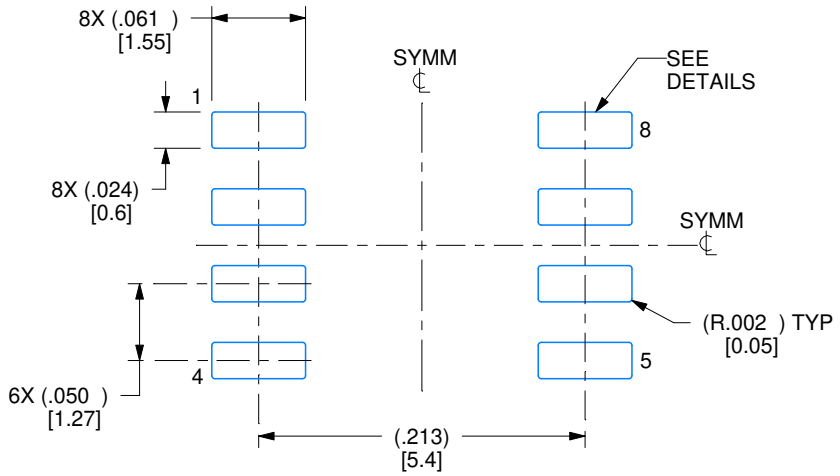
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

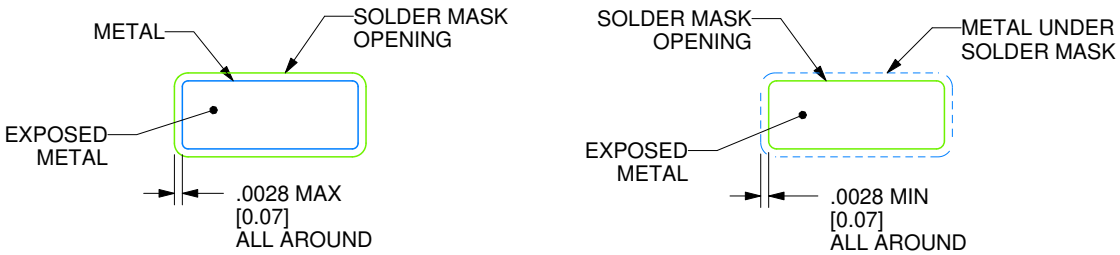


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

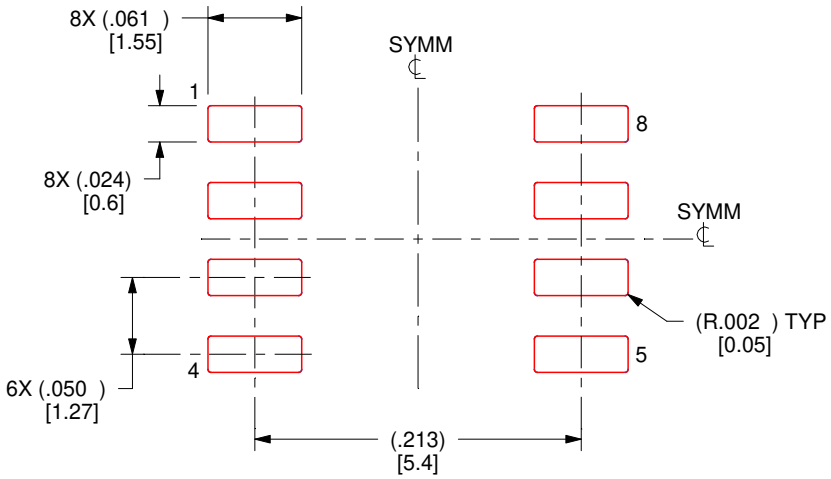
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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