Single Output Mobile-Friendly PWM Controller

The ISL6224 provides power control and protection for a single, adjustable output voltage required to power chip-sets and memory banks in high-performance notebooks and PDAs. This output voltage is adjustable in the range from 0.9-5.5V.

The hysteretic or PWM controller regulates the output voltage from battery voltages ranging from 4V to 24V. Synchronous rectification and hysteretic operation at light loads contribute to a high efficiency over a wide range of input voltages and loads. Efficiency is even further enhanced by using MOSFET's $r_{DS(ON)}$ as a current sense component. Feed-forward ramp modulation, average current mode control and internal feed-back compensation provide fast and firm handling of transients when powering advanced chip sets.

Two-stage conversion using system 5V voltage is possible at a higher frequency (600kHz) to minimize the output filter size.

The ISL6224 monitors the output voltage. A PGOOD (power good) signal is issued when soft-start is completed and the output is within ±10% of the set point.

A built-in overvoltage protection prevents output voltage from going above 120% of the set point. Undervoltage protection latches the chip off when the output drops below 70% of its setting value after soft-start sequence is completed. The PWM controller's overcurrent circuitry monitors the output current by sensing the voltage drop across the lower MOSFET. If higher precision sense technique is required, an optional external current-sense resistor may be used.

Ordering Information

PART NUMBER	PART MARKING	TEMP. (°C)	PACKAGE	PKG. DWG. #
ISL6224CA	ISL6224CA	-10 to 85	16 Ld SSOP	M16.15A
ISL6224CAZ (Note 1)	6224CAZ	-10 to 85	16 Ld SSOP (Pb-free)	M16.15A

NOTES:

1. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add "-T" for Tape and Reel.

Features

- Adjustable output voltgage: 0.9-5.5V
- High efficiency over wide load range
  - Higher efficiency in hysteretic mode at light load
- Lossless current sense scheme
  - Uses MOSFET's $r_{DS(ON)}$
  - Optional current sense method higher precision
- Supply operation mode
  - Wide V_{IN} range: 4V-24V
  - Single 5V system rail
- Input undervoltage lock-out on VCC pin (UVLO)
- Excellent dynamic response
  - Combined voltage feed-forward and current mode control
- Power-good indicator
- 300/600kHz switching frequency
- Thermal shut-down
- Pb-free plus anneal available (RoHS compliant)

Applications

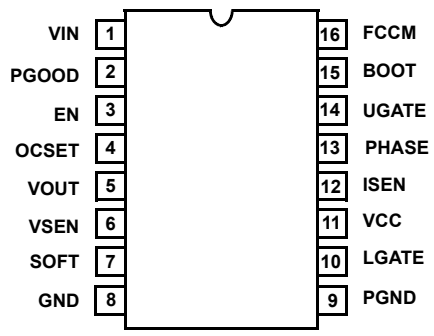
- Mobile PCs
- Graphic cards
- Hand-held portable instruments

Related Literature

- Application Note AN9983

Pinout

ISL6224 (SSOP)
TOP VIEW



Absolute Maximum Ratings

Bias Voltage, V_{CC} . . . . . -0.3V to +7V
Input Voltage, Vin . . . . . +27.0V
Phase and Isen Pins . . . . . GND -0.3V to +29.0V
BOOT and Ugate Pins . . . . . + 32.0V
BOOT with respect to PHASE . . . . . + 7.0V
All other pins . . . . . GND -0.3V to 15V
ESD Classification . . . . . Class 2

Recommended Operating Conditions

Bias Voltage, V_{CC} . . . . . +5.0V ±5%
Input Voltage, Vin . . . . . 4.0V to +24.0V
Ambient Temperature Range . . . . . -10°C to 85°C
Junction Temperature Range . . . . . -10°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SSOP Package	112

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

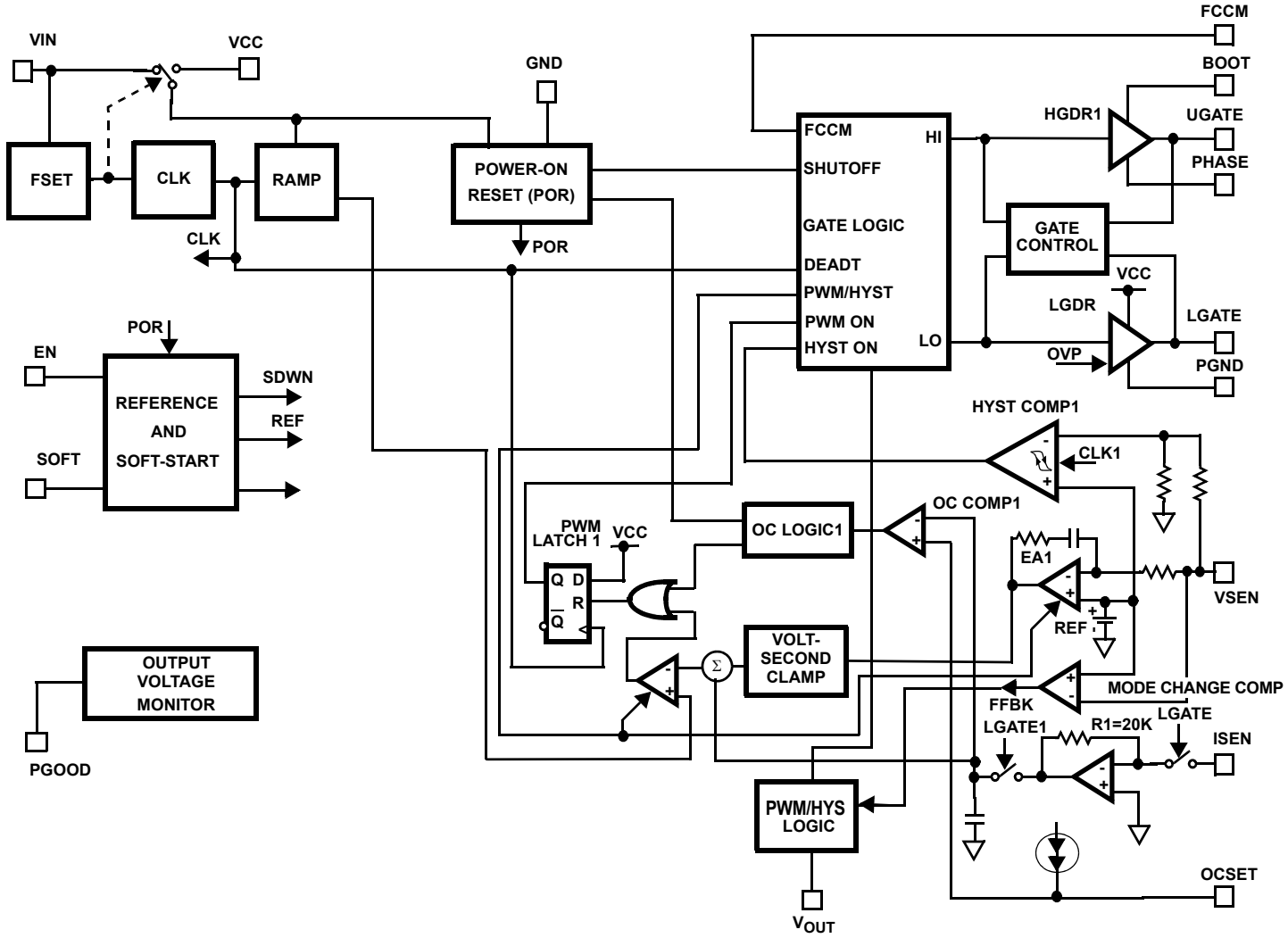
Operating Conditions: V_{CC} = 5V, T_A = 10°C to 85°C, Unless Otherwise Noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY						
Bias Current	I_{CC}	LGATE, UGATE Open, VSEN forced above regulation point	-	850	1300	µA
Shutdown Current	I_{CCSN}		-	5	15	µA
VCC UVLO						
Rising Vcc Threshold			4.3	-	4.75	V
Falling Vcc Threshold			4.1	-	4.5	V
Vcc UVLO Hysteris			0.1	-	0.5	V
VIN						
Input Voltage Pin Current (Sink)	I_{VIN}	VIN pin connected to the input voltage source	10	20	30	µA
Input Voltage Pin Current (Source)	I_{VIN}	VIN pin connected to ground	-7	-15	-20	µA
Shutdown Current	I_{VIN}		-	-	1	µA
OSCILLATOR						
PWM Oscillator Frequency	F_{c1}	V_{IN} = 3.5V - 24V	255	300	345	kHz
PWM Oscillator Frequency	F_{c2}	$V_{IN} \leq 0.5V$	510	600	690	kHz
Ramp Amplitude, pk-pk	V_{R1}	V_{IN} = 16V, By Design	-	2	-	V
Ramp Amplitude, pk-pk	V_{R2}	$V_{IN} \leq 5V$, By Design	-	1.25	-	V
Ramp Offset	V_{ROFF}		-	0.5	-	V
REFERENCE AND SOFT-START						
Internal Reference Voltage	V_{REF}		-	0.9	-	V
Reference Voltage Accuracy			-1.0	-	+1.0	%
Soft-Start Current During Start-up	I_{SOFT}		-	5	-	µA
Soft-Start Threshold	V_{SOFT}		-	1.5	-	V
PWM CONVERTER						
Load Regulation		0.0mA < I_{VOUT1} < 3.0A; 5.0V < V_{IN} < 24.0V	-1.0	-	+1.0	%
VSEN pin bias current	I_{VSEN}		-	80	-	nA

Electrical Specifications Operating Conditions: V_{CC} = 5V, T_A = 10°C to 85°C, Unless Otherwise Noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VOUT pin input impedance	I_{VOUT}		40	55	65	kΩ
Undervoltage Shutdown Level	V_{UV1}	Fraction of the set point; ~3µs noise filter	70	-	80	%
Overvoltage Protection	V_{OVP1}	Fraction of the set point; ~1µs noise filter	113	-	120	%
PWM CONTROLLER GATE DRIVERS						
Upper Drive Pull-Up Resistance	R_{2UGPUP}		-	8	15	Ω
Upper Drive Pull-Down Resistance	R_{2UGPDN}		-	3.2	5	Ω
Lower Drive Pull-Up Resistance	R_{2LGPUP}		-	8	15	Ω
Lower Drive Pull-Down Resistance	R_{2LGPDN}		-	1.5	2.4	Ω
POWER GOOD AND CONTROL FUNCTIONS						
Power-Good Lower Threshold	V_{PG-}	Fraction of the set point; ~3µs noise filter	-14	-	-8	%
Power-Good Higher Threshold	V_{PG+}	Fraction of the set point; ~3µs noise filter	10	-	15	%
PGOOD Leakage Current	I_{PGLKG}	V_{PULLUP} = 5.5V	-	-	1	µA
PGOOD Voltage Low		I_{PGOOD} = -4mA	-	-	0.5	V
EN - Low (Off)			-	-	0.8	V
EN - High (On)			2.0	-	-	V
FCCM -Hysteretic Operation Enabled			-	Vcc/2	-	V

Functional Block Diagram



Functional Pin Description

VIN (Pin 1)

Provides battery voltage to the oscillator for feed-forward rejection of the input voltage variation. Also, this pin programs frequency of the internal clock and gain of the ramp generator. When connected to the battery, which voltage varies from 4V to 24V, the clock frequency is set to 300kHz and the ramp gain is set accordingly to accommodate the wide input voltage range.

For two step conversion from the system 5V power rail, the Vin pin is connected to ground via a 150kΩ resistor. This arrangement changes the gain of the ramp generator to accommodate the lower input voltage but does not change the clock frequency.

When the Vin pin is connected to ground, the clock frequency is set to 600kHz. The ramp generator gain is also changed accordingly. This circuit arrangement enables the designer to choose smaller output filter components.

PGOOD (Pin 2)

PGOOD is an open collector output used to indicate the status of the output voltage. This pin is pulled high when the system output is within ±10% of its respective nominal voltage.

EN (Pin 3)

This pin provides the enable/disable function for the chip. The IC is enabled when this pin is pulled over 2V or left open. Note: a pulldown resistance of 100kΩ or less is required to disable the controller.

OCSET (Pin 4)

A resistor from this pin to GND sets the overcurrent protection threshold.

VOUT (Pin 5)

This pin is used for feedback of the output voltage to properly position output voltage during operational mode change.

VSEN (Pin 6)

This pin is connected to the output via a resistive divider and provides the voltage feedback signal for the PWM controller. The PGOOD, UVP, and OVP circuits use this signal to report output voltage status.

SOFT (Pin 7)

This pin provides soft-start of the PWM controller. When the EN pin is pulled high, the voltage on the capacitor connected to the soft-start pin is rising linearly due to the 5μA pull-up current. The output voltage follows the voltage on the capacitor until it reaches the value of 0.9V. The further rise of the voltage on the soft-start capacitor does not affect the output voltage.

GND (Pin 8)

Signal ground for the IC.

PGND (Pin 9)

This is the power ground connection for PWM converter. This pin is connected to the lower MOSFET's source terminal.

LGATE (Pin 10)

This pin provides the gate drive for the lower MOSFET.

VCC (Pin 11)

This pin provides power to the chip.

ISEN (Pin 12)

This pin is used to monitor the voltage drop across the lower MOSFET for current feedback and overcurrent protection. For precise current detection this input can be connected to an optional current sense resistor placed in series with the source of the lower MOSFET.

PHASE (Pin 13)

Connect this pin to the PHASE node of the converter. The PHASE node is the junction point of the upper MOSFET source, output filter inductor, and lower MOSFET drain.

UGATE (Pin 14)

This pin provides the gate drive for the upper MOSFET.

BOOT (Pin 15)

This pin powers the upper MOSFET drivers of the PWM converter. Connect this pin to the junction of bootstrap capacitor with the cathode of the bootstrap diode. Anode of the bootstrap diode is connected to the VCC pin.

FCCM (Pin 16)

This pin, when pulled to VCC, restrains hysteretic operation in light loads.

General Description

Operational Overview

The ISL6224 is a single-channel PWM controller intended for chipset, DRAM, or other low voltage power needs of modern notebook and sub-notebook PCs. The IC integrates control circuits and feedback compensation for a single synchronous buck converter. The output voltage is set in the range of 0.9–5.5V by an external resistive divider.

The synchronous buck converter can be configured for either 300kHz or 600kHz switching frequencies. When operated from battery, a switching frequency of 300kHz is recommended. When operating from 5V, switching frequencies of 300kHz or 600kHz are an option. For 300kHz operation, pin 1 should be connected through a resistor (150K) to gnd. For 600kHz operation, pin 1 should simply be

grounded. Table 1. shows the configuration for different modes of operation. Figure 1 below shows plots of the ramp speed compensation.

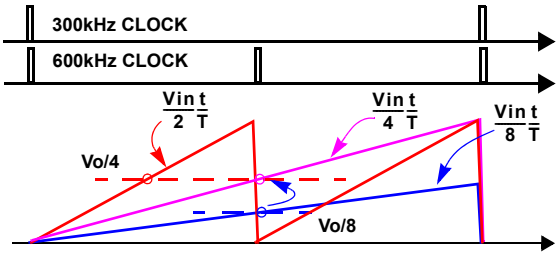


FIGURE 1. RAMP SPEED COMPENSATION Vo = 2.5V

TABLE 1. CONFIGURATION FOR MODES OF OPERATION

OPERATION	PIN 1 CONNECTION	PIN 1 POTENTIAL
One-stage 300kHz	Vin	V1 > 4V
Two-stage 300kHz	150K-GND	1V < V1 < 2V
Two-stage 600kHz	GND	V1 < 0.5V

The synchronous converter light-load efficiency is enhanced by a hysteretic mode of operation which is automatically engaged at light loads when the inductor current becomes discontinuous. As the filter inductor resumes continuous current, the PWM mode of operation is automatically restored.

The ISL6224 control IC employs an average current mode control scheme with input voltage feedforward ramp programming for better rejection of input voltage variations.

Current Sensing and Current Limit Protection

The PWM converter uses the lower MOSFET on-state resistance, $r_{DS(ON)}$, as the current-sensing element. This technique eliminates the need for a current sense resistor and the associated power losses. If more accurate current protection is desired, current sense resistors may be used in series with the lower MOSFET's source.

A current proportional signal is used to provide average current mode control and overcurrent protection. The gain in the current sense circuit is set by the resistor connected from ISEN (pin 12) to the PHASE node of the buck converter. The value of this resistor can be estimated by the following expression:

$$Risen = \frac{Iomax \bullet Rdson}{75\mu A} - 100$$

where Iomax is the maximum inductor current. The value of R_{ISEN} should be specified for the expected maximum operating temperature.

An overcurrent protection threshold is set by an external resistor connected from OCSET (pin 4) to ground. The value of this resistor can be obtained from the following expression:

$$Rocset = \frac{11 \bullet Risen}{Ioc \bullet Rdson}$$

where Ioc is the value of overcurrent. The resulting current out of the ISEN pin through R_{ISEN}, is used for current feedback and current limit protection. This is compared with an internal current limit threshold. When a sampled value of the output current is determined to be above the current limit threshold, the PWM drive is terminated and a counter is initiated. This limits the inductor current build-up and essentially switches the converter into current-limit mode. If an overcurrent is detected between 26ms to 53ms later, an overcurrent shutdown is initiated. If during the 26ms to 53ms period, an overcurrent is not detected, the counter is reset and sampling continues as normal.

This current limit scheme has proven to be very robust in applications like portable computers where fast inductor current build-up is common due to a large difference between input and output voltages and a low value of the inductor.

Light-Load (Hysteretic) Operation

In the light-load (hysteretic) mode the output voltage is regulated by the hysteretic comparator which regulates the output voltage by maintaining the output voltage ripple as shown in Figure 2. In hysteretic mode, the inductor current flows only when the output voltage reaches the lower limit of the hysteretic comparator and turns off at the upper limit. Hysteretic mode saves converter energy at light loads by supplying energy only at the time when the output voltage requires it. This mode conserves energy by reducing the power dissipation associated with continuous switching.

During the time between inductor current pulses, both the upper and lower MOSFETs are turned off. This is referred to as 'diode emulation mode' because the lower MOSFET performs the function of a diode. This diode emulation mode prevents the output capacitor from discharging through the lower MOSFET when the upper MOSFET is not conducting.

NOTE: the PWM only operation can intentionally be forced by tying pin 16, FCCM, to VCC.

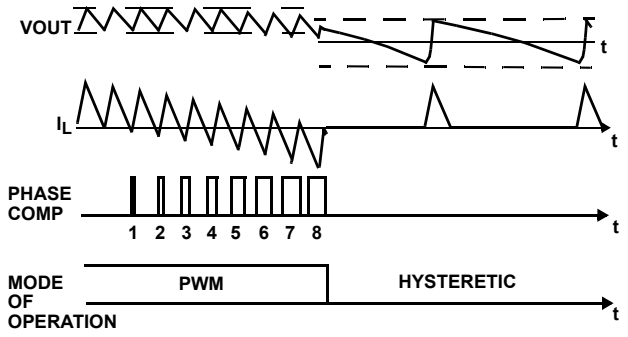


FIGURE 2. HYSTERETIC OPERATION MODE

Operation-Mode Control

The mode-control circuit changes the converter's mode of operation based on the voltage polarity of the phase node when the lower MOSFET is conducting and just before the upper MOSFET turns on. For continuous inductor current, the phase node is negative when the lower MOSFET is conducting and the converters operate in fixed-frequency PWM mode as shown in Figure 3. When the load current decreases to the point where the inductor current flows through the lower MOSFET in the 'reverse' direction, the phase node becomes positive, and the mode is changed to hysteretic.

A phase comparator handles the timing of the phase node voltage sensing. A low level on the phase comparator output indicates a negative phase voltage during the conduction time of the lower MOSFET. A high level on the phase comparator output indicates a positive phase voltage.

When the phase node is positive (phase comparator high), at the end of the lower MOSFET conduction time, for eight consecutive clock cycles, the mode is changed to hysteretic as shown in Figure 3. The dashed lines indicate when the phase node goes positive and the phase comparator output goes high. The solid vertical lines at 1,2,...8 indicate the sampling time, of the phase comparator, to determine the polarity (sign) of the phase node. At the transition between PWM and hysteretic mode both the upper and lower MOSFETs are turned off. The phase node will 'ring' based on the output inductor and the parasitic capacitance on the phase node and settle out at the value of the output voltage.

The mode change from hysteretic to PWM can be caused by one of two events. One event is the same mechanism that causes a PWM to hysteretic transition. But instead of looking for eight consecutive positive occurrences on the phase node, it is looking for eight consecutive negative occurrences on the phase node. The operation mode will be changed from hysteretic to PWM when these eight consecutive pulses occur. This transition technique prevents jitter of the operation mode at load levels close to boundary.

The other mechanism for changing from hysteretic to PWM is due to a sudden increase in the output current. This step load causes an instantaneous decrease in the output voltage due to the voltage drop on the output capacitor ESR. If the decrease causes the output voltage to drop below the hysteretic regulation level, the mode is changed to PWM on the next clock cycle. This insures the full power required by the increase in output current.

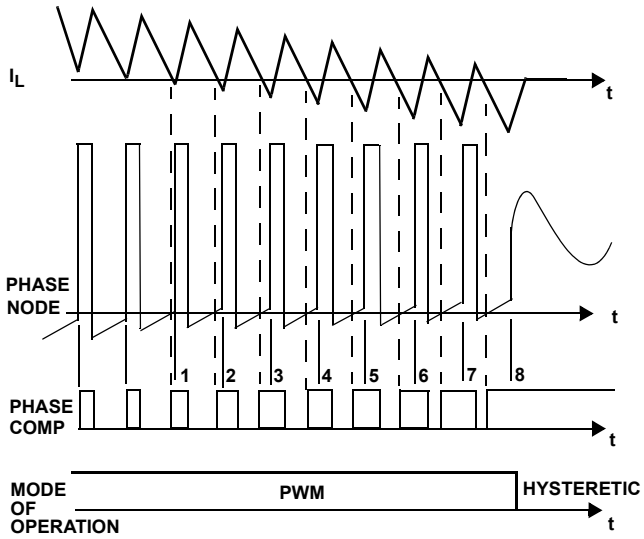


FIGURE 3. MODE CONTROL WAVEFORMS

Gate Control Logic

The gate control logic translates generated PWM control signals into the MOSFET gate drive signals providing necessary amplification, level shifting and shoot-through protection. Also, it has functions that help optimize the IC performance over a wide range of operational conditions. Since MOSFET switching time can vary dramatically from type to type and with the input voltage, the gate control logic provides adaptive dead time by monitoring the gate-to-source voltages of both upper and lower MOSFETs. The lower MOSFET is not turned on until the gate-to-source voltage of the upper MOSFET has decreased to less than approximately 1V. Similarly, the upper MOSFET is not turned on until the gate-to-source voltage of the lower MOSFET has decreased to less than approximately 1V. This allows a wide variety of upper and lower MOSFETs to be used without a concern for simultaneous conduction, or shoot-through.

Soft-Start Operation

Soft-start of the Synchronous Buck Converter is accomplished by means of a capacitor connected from pin 7, SOFT to ground. The soft-start time can be obtained from the following equation:

$$Tss = \frac{1.5V \times Css}{5.0\mu A}$$

Figure 4 shows the soft-start initiated by the ENABLE pin being pulled high with the VIN input at 5.6V and the resulting 3.3V output and PGOOD signal. While the ENABLE pin is held low, prior to t0, the output is off. When the EN pin is pulled high, at t0, the voltage on the capacitor connected to the soft-start pin rises linearly due to the internal 5µA current source starts charging the capacitor. The output voltage follows the voltage on the capacitor till it reaches the value of 0.9V at t1. At this moment, t1, the output voltage started regulation. The soft-start is complete when PGOOD pin is high at t2 and further rise of the voltage on the soft-start capacitor does not affect the output voltage.

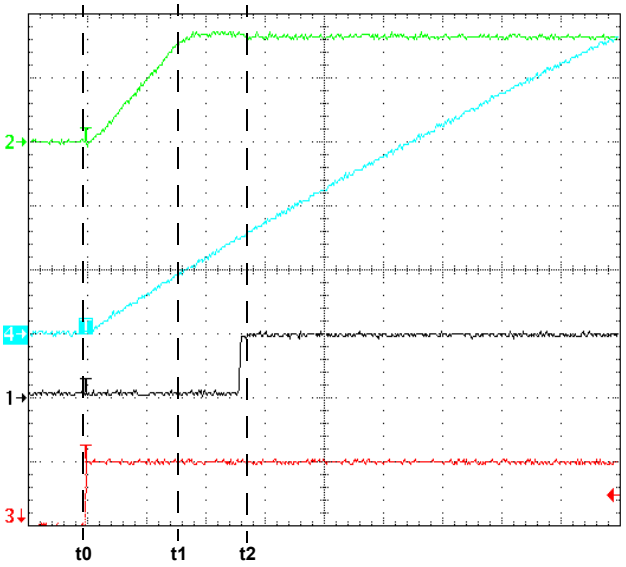


FIGURE 4. MODE CONTROL WAVEFORMS

Power Good Status

The ISL6224 monitors the output voltage. A single power-good signal, PGOOD, is issued when soft-start is completed and the output is within 10% of it's set point. After the soft-start sequence is completed, undervoltage protection latches the chip off when any of the monitored outputs drop below 70% of its set point.

A 'soft-crowbar' function is implemented for an overvoltage on the output. If the output voltage goes above 120% of its nominal output level, the upper MOSFET is turned off and the lower MOSFET is turned on. This 'soft-crowbar' condition will be maintained until the output voltage returns to the regulation window and then normal operation will continue.

This 'soft-crowbar' and monitoring of the output, prevents the output voltage from ringing negative as the inductor current flows in the 'reverse' direction through the lower MOSFET and output capacitors.

Component Selection Guidelines

Output Capacitor Selection

The output capacitors have unique requirements. In general, the output capacitors should be selected to meet the dynamic regulation requirements including ripple voltage and load transients.

Selection of the output capacitors is also dependent on the output inductor so some inductor analysis is required to select the output capacitors.

One of the parameters limiting the converter's response to a load transient is the time required for the inductor current to slew to its new level. Given a sufficiently fast control loop design, the ISL6224 will provide either 0% or 94% duty cycle in response to a load transient. The response time is the time interval required to slew the inductor current from an initial current value to the load current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor(s). Minimizing the response time can minimize the output capacitance required. If the load transient rise time is slower than the inductor response time, as in a hard drive or CD drive, this reduces the requirement on the output capacitor.

The maximum capacitor value required to provide the full, rising step, transient load current during the response time of the inductor is:

$$C_{OUT} = \frac{L_O \times I_{TRAN}}{(V_{IN} - V_{OUT}) \times 2} \times \frac{I_{TRAN}}{DV_{OUT}}$$

Where: C_{OUT} is the output capacitor(s) required, L_O is the output inductor, I_{TRAN} is the transient load current step, V_{IN} is the input voltage, V_{OUT} is output voltage, and DV_{OUT} is the drop in output voltage allowed during the load transient.

High frequency capacitors initially supply the transient current and slow the load rate-of-change seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (equivalent series resistance) and voltage rating requirements as well as actual capacitance requirements. The output voltage ripple is due to the inductor ripple current and the ESR of the output capacitors as defined by:

$$V_{RIPPLE} = \Delta I_L \times ESR$$

where, ΔI_L is calculated in the *Inductor Selection* section.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that

could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load circuitry for specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications, at 300kHz, for the bulk capacitors. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

The stability requirement on the selection of the output capacitor is that the 'ESR zero', f_Z, be between 1.2kHz and 30kHz. This range is set by an internal, single compensation zero at 6kHz. The ESR zero can be a factor of five on either side of the internal zero and still contribute to increased phase margin of the control loop. Therefore:

$$C_{OUT} = \frac{1}{2 \times \pi \times ESR \times f_Z}$$

In conclusion, the output capacitors must meet three criteria:

1. They must have sufficient bulk capacitance to sustain the output voltage during a load transient while the output inductor current is slewing to the value of the load transient
2. The ESR must be sufficiently low to meet the desired output voltage ripple due to the output inductor current, and
3. The ESR zero should be placed, in a rather large range, to provide additional phase margin.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current and output capacitor(s) ESR. The ripple voltage expression is given in the capacitor selection section and the ripple current is approximated by the following equation:

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{F_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

where F_S is the switching frequency.

Input Capacitor Selection

The important parameters for the bulk input capacitor(s) are the voltage rating and the RMS current rating. For reliable operation, select bulk input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and 1.5 times is a conservative guideline.

The AC RMS input current varies with load. Depending on the specifics of the input power and it's impedance, most (or all) of this current is supplied by the input capacitor(s).

Use a mix of input bypass capacitors to control the voltage ripple across the MOSFETs. Use ceramic capacitors for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors can be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedances.

For board designs that allow through-hole components, the Sanyo OS-CON® series offer low ESR and good temperature performance.

For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX is surge current tested.

MOSFET Considerations

The logic level MOSFETs are chosen for optimum efficiency given the potentially wide input voltage range and output power requirements. One dual N-Channel or two N-Channel MOSFETs are used in each of the synchronous rectified buck converters for the outputs. These MOSFETs should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management considerations.

The power dissipation includes two loss components; conduction loss and switching loss. These losses are distributed between the upper and lower MOSFETs according to duty cycle (see the following equations). The conduction losses are the main component of power dissipation for the lower MOSFETs. Only the upper MOSFET has significant switching losses, since the lower device turns on and off into near-zero voltage.

$$P_{UPPER} = \frac{I_O^2 \times r_{DS(ON)} \times V_{OUT}}{V_{IN}} + \frac{I_O \times V_{IN} \times t_{SW} \times F_S}{2}$$

$$P_{LOWER} = \frac{I_O^2 \times r_{DS(ON)} \times (V_{IN} - V_{OUT})}{V_{IN}}$$

The equations assume linear voltage-current transitions and do not model power loss due to the reverse-recovery of the lower MOSFET's body diode.

The gate-charge losses are dissipated by the ISL6224 and do not heat the MOSFETs. However, a large gate-charge increases the switching time, t_{SW} which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications.

Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device overvoltage stress. Careful component layout and printed circuit design minimizes the voltage spikes in the converter. Consider, as an example, the turn-off transition of one of the upper PWM MOSFETs. Prior to turn-off, the upper MOSFET is carrying the full load current. During the turn-off, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET. Any inductance in the switched current path generates a voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes. See the Application Note AN9983 for the evaluation board component placement and the printed circuit board layout details.

There are two sets of critical components in a DC/DC converter using an ISL6224 controller. The switching power components are the most critical because they switch large amounts of energy, and as such, they tend to generate equally large amounts of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bias currents.

Power Components Layout Considerations

The power components and the controller IC should be placed first. Locate the input capacitors, especially the high-frequency ceramic decoupling capacitors, close to the power MOSFETs. Locate the output inductor and output capacitors between the MOSFETs and the load. Locate the PWM controller close to the MOSFETs.

Insure the current paths from the input capacitors to the MOSFETs, to the output inductors and output capacitors are as short as possible with maximum allowable trace widths.

A multi-layer printed circuit board is recommended. Dedicate one solid layer for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes, but do not unnecessarily oversize these particular islands. Since the phase nodes are subjected to very high dV/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry will tend to couple switching noise. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the control IC to the MOSFET gate and source should be sized to carry 2A peak currents.

Small Components Signal Layout Considerations

The Vin pin 1 input should be bypassed with a 1.0µF capacitor. The bypass capacitors for Vin and the soft-start capacitor, should be located close to their connecting pins on the control IC.

Refer to the Application Note AN9983 for a recommended component placement and interconnections.

Figures 5, 6 and 7 show application circuits for the three modes of operation. Mode 1 is operating from battery voltage and operating at 300kHz switching frequency. Mode 2 is operating off of 5V and operating at 300kHz switching frequency. Mode 3 is operating off of 5V and operating at 600kHz switching frequency.

ISL6224 DC-DC Converter Application Circuits

Figure 5 shows an application circuit of a DC/DC converter for a notebook PC. The power supply provides +V2_5S from either +4V–24V_{DC} battery voltage or system +5V bus. For detailed information on the circuit, including a bill of materials and circuit board description, see Application Note AN9983. Also see Intersil's web site (http://www.intersil.com) for the latest information.

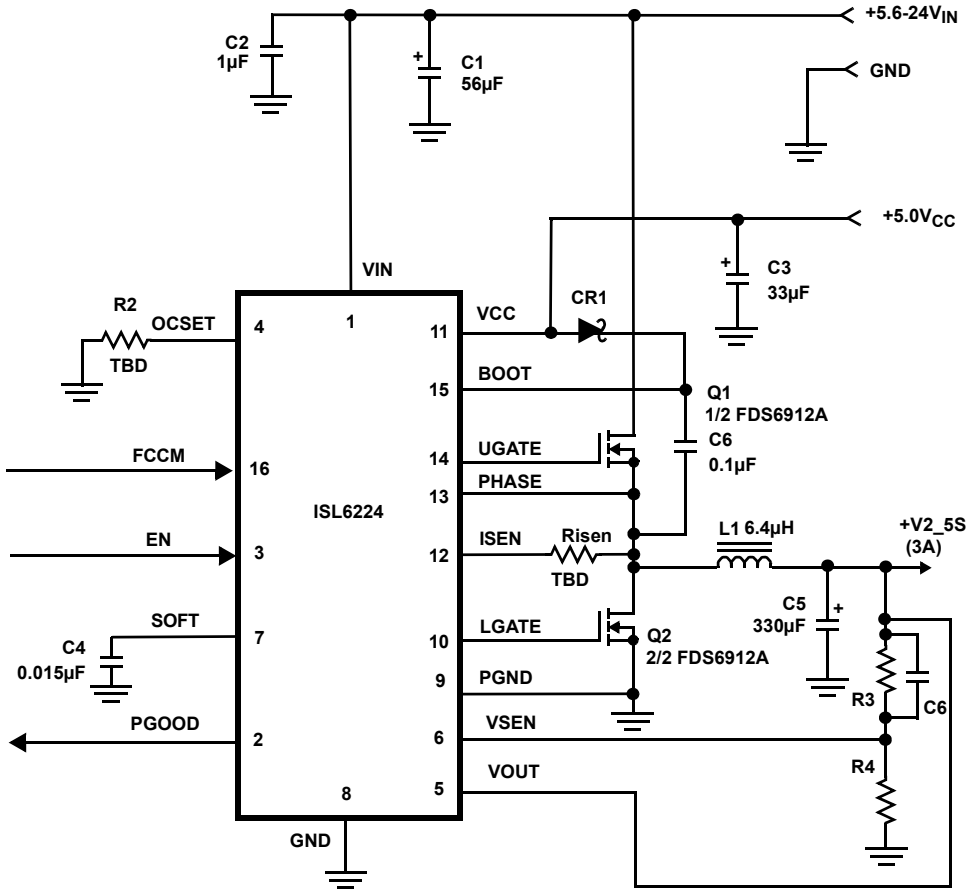


FIGURE 5. APPLICATION CIRCUIT FOR ONE-STEP CONVERSION (MODE 1)

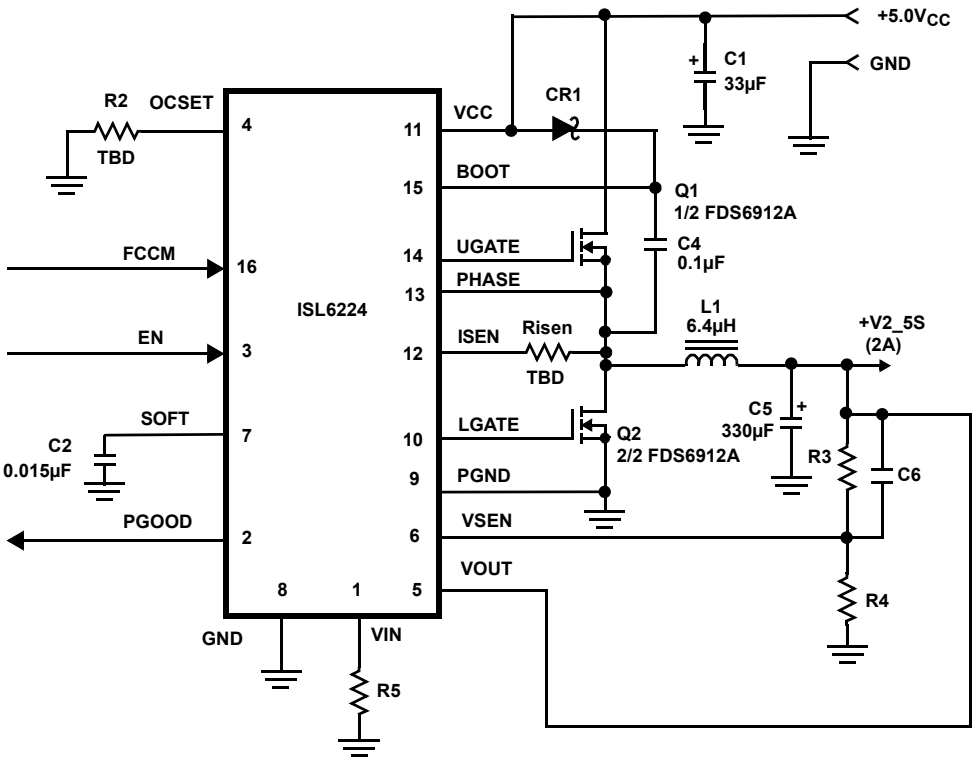


FIGURE 6. APPLICATION CIRCUIT FOR TWO-STEP 300kHz CONVERSION (MODE 2)

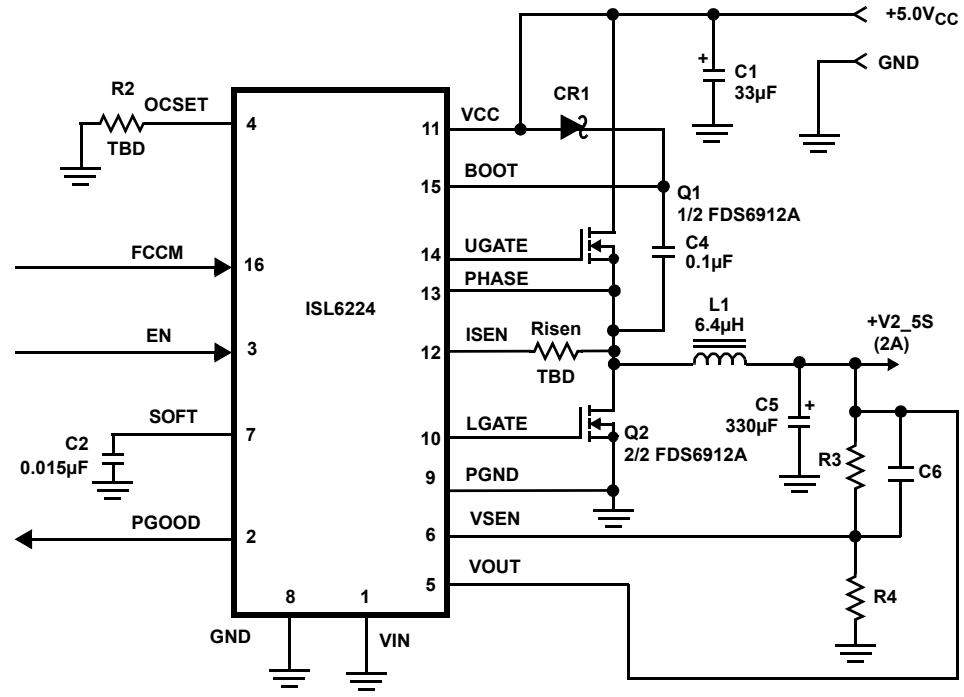
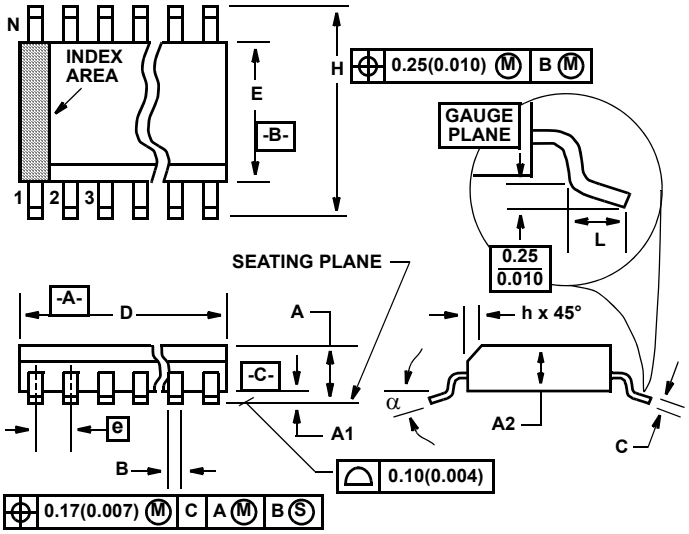


FIGURE 7. APPLICATION CIRCUIT FOR TWO-STEP 600kHz CONVERSION (MODE 3)

Shrink Small Outline Plastic Packages (SSOP)
Quarter Size Outline Plastic Packages (QSOP)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

M16.15A

16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (0.150” WIDE BODY)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.061	0.068	1.55	1.73	-
A1	0.004	0.0098	0.102	0.249	-
A2	0.055	0.061	1.40	1.55	-
B	0.008	0.012	0.20	0.31	9
C	0.0075	0.0098	0.191	0.249	-
D	0.189	0.196	4.80	4.98	3
E	0.150	0.157	3.81	3.99	4
e	0.025 BSC		0.635 BSC		-
H	0.230	0.244	5.84	6.20	-
h	0.010	0.016	0.25	0.41	5
L	0.016	0.035	0.41	0.89	6
N	16		16		7
α	0°	8°	0°	8°	-

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