ISL85014EVAL1Z Evaluation Board User Guide

Description

The ISL85014 is a 3.8V to 18V input, 14A synchronous buck regulator for applications with input voltage from multi-cell batteries or regulated 5V and 12V power rails. The device also provides an integrated bootstrap diode for the high-side gate driver to reduce the external parts count. The ISL85014EVAL1Z platform allows quick evaluation of the high-performance features of the ISL85014 buck regulator.

Specifications

This board has been configured and optimized for the following operating conditions:

- Input voltage ranges from 4.5V to 18V
- 1.8V nominal output voltage
- Up to 14A output current capability
- Default internally set to 600kHz switching frequency
- Default internally set to 3ms soft-start
- Operating temperature range: -40°C to +85°C

Key Features

- Switch selectable EN (enabled/disabled)
- Frequency synchronization option
- Jumper selectable mode (DEM/Forced CCM)
- Jumper selectable OCP mode (Hiccup/Latch-off)
- Jumper selectable frequency (600kHz/300kHz)
- Connectors and test points for easy probing
- Compact design

Related Literature

- For a full list of related documents, visit our website
  - ISL85014 product pages

Ordering Information

PART NUMBER	DESCRIPTION
ISL85014EVAL1Z	Evaluation board for ISL85014FRZ

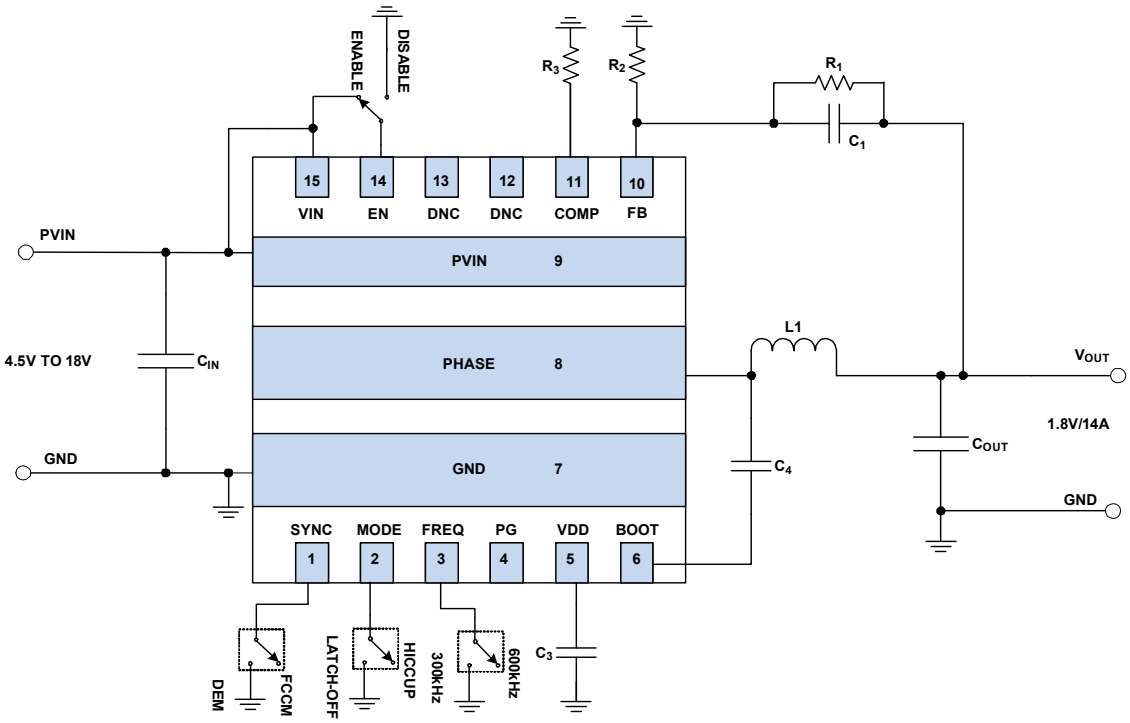

FIGURE 1. BLOCK DIAGRAM

Connector and Test Point Descriptions

The ISL85014EVAL1Z evaluation board includes I/O connectors and test points as shown in Table 1.

TABLE 1. CONNECTORS AND TEST POINTS

REFERENCE DESIGNATOR	DESCRIPTION
J1	Input voltage positive connection
J2	Output voltage positive connection
J3	Input voltage return connection
J4	Output voltage return connection
J6	Two-position socket connector for PHASE to GND test
J7	Two-position socket connector for VOUT to GND test
PVIN	PVIN positive test point
GND	GND test point
VIN	VIN positive test point
VOUT	Output voltage positive test point
SYNC	External synchronization clock connection
EN	Enable test point
VDD	Internal LDO output test point
PG	Power-good output

Selection Switch and Jumper Descriptions

- Switch SW5 (Enable)
  The switch enables and disables the ISL85014:
  - When the switch is in the ON position, the ISL85014 is enabled.
  - When the switch is in the OFF position, the ISL85014 is disabled.
- Jumper J9
  The jumper provides the selection of different operating modes, detailed as follows:
  - When the jumper is in the FCCM position, the ISL85014 operates in Forced CCM.
  - When the jumper is in the DEM position, the ISL85014 operates in Diode Emulation mode and enables automatic transition from CCM to DCM at light-load conditions.
- Jumper J10 sets the switching frequency at either 600kHz or 300kHz.
- Jumper J11 sets the OCP scheme in either Hiccup mode or Latch-Off mode.

Quick Setup Guide

Refer to the following instructions to configure and power-up the board for proper operation.

1. Set the power supply voltage to 12V and turn off the power supply. Connect the positive output of the power supply to J1 (PVIN) and the negative output to J3 (GND).
2. Connect an electronic load to J2 (VOUT) for the positive connection and J4 (GND) for the negative connection.
3. Measure the output voltage (test points VOUT and GND) with the voltmeter.
4. Place scope probes on VOUT test point (J7) and other test points of interest.
5. Toggle selection switch SW5 to ON position.
6. Set the load current to 0.1A and turn on the power supply. The output voltage should be in regulation with a nominal 1.8V output.
7. Slowly increase the load up to 14A while monitoring the output voltage, which should remain in regulation with a nominal 1.8V output.
8. Slowly sweep VIN from 4.5V to 18V. The output voltage should remain in regulation with a nominal 1.8V output.
9. Decrease the input voltage to 0V to shut down the regulator.

Frequency Synchronization

The ISL85014 can be synchronized to an external clock with frequency ranges from 100kHz to 1MHz by applying the external clock to test point SYNC on the ISL85014EVAL1Z evaluation board. The external clock should meet the specifications of pulse width and voltage level described in the ISL85014 datasheet.

Evaluating Other Output Voltages

The ISL85014EVAL1Z has a nominal 1.8V output voltage. The output voltage is programmable by an external resistor divider formed by R_1 and R_2 as shown in Figure 1 on page 1. R_1 is usually chosen first, then the value for R_2 can be calculated based on R_1 and the desired output voltage using Equation 1:

$$R_2 = \frac{R_1 \cdot 0.6V}{V_{OUT} - 0.6V} \quad \text{(EQ. 1)}$$

PCB Layout Considerations

The PCB layout is critical for proper operation of the ISL85014. The following guidelines should be followed to achieve good performance.

1. Use a multilayer PCB structure to achieve optimized performance. A four-layer PCB is recommended for this design.
2. Use a combination of bulk capacitors and smaller ceramic capacitors with lower ESL for the input capacitors, and place them as close to the IC as possible.
3. Place the VDD decoupling capacitor close to the IC between VDD and GND. A 1µF ceramic capacitor is typically used.
4. Place a bootstrap capacitor close to the IC between the BOOT and PHASE pins. A 0.1µF ceramic capacitor is typically used.
5. Connect the feedback resistor divider between the output capacitor positive terminal and AGND pin of the IC, and place the resistors close to the FB pin of the IC.
6. Connect the GND of the IC to the ground planes underneath using multiple thermal vias to improve thermal performance.

ISL85014EVAL1Z Evaluation Board

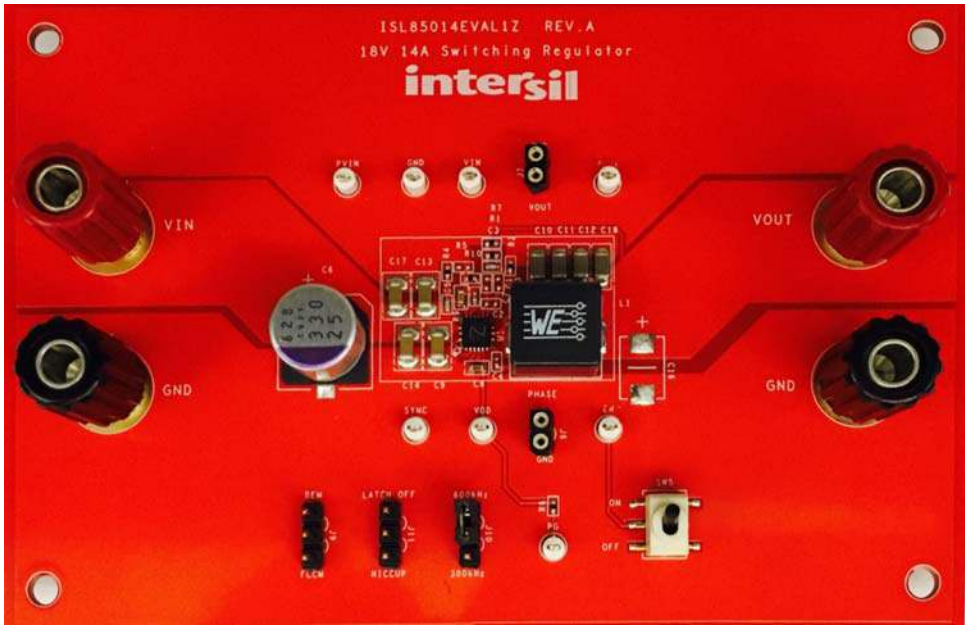

FIGURE 2. TOP VIEW

ISL85014EVAL1Z Schematic

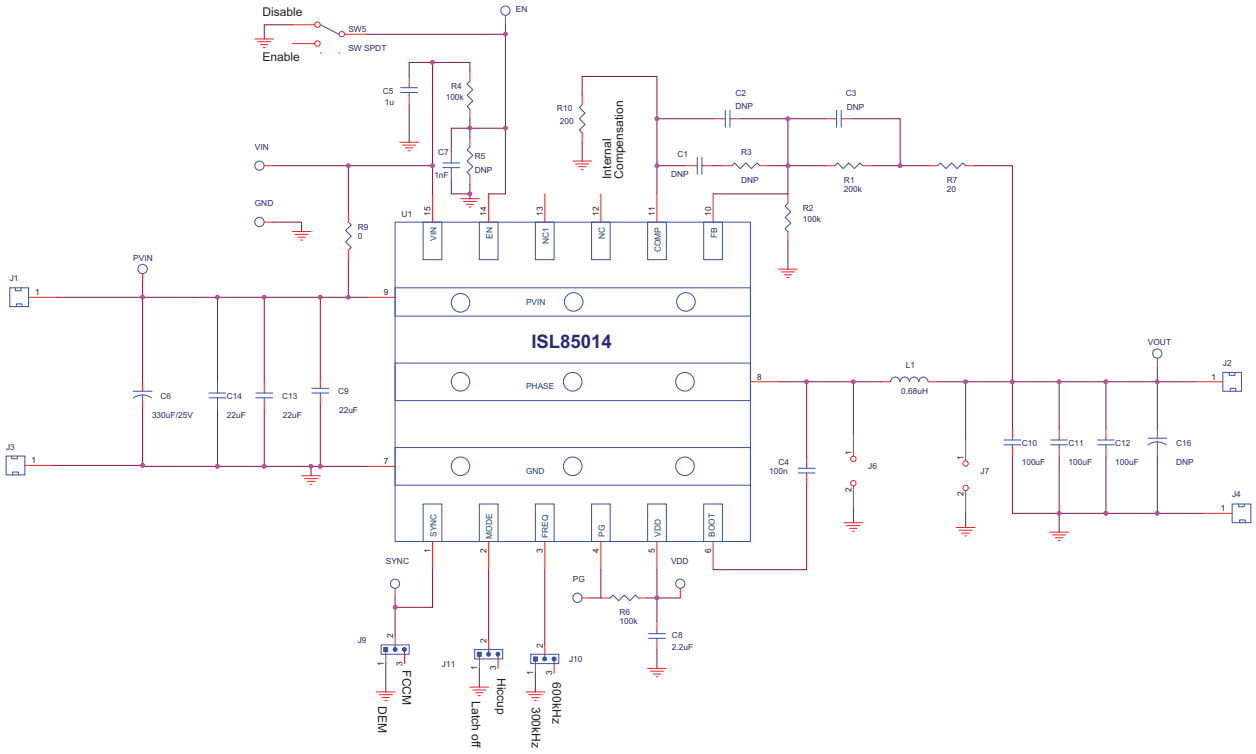

FIGURE 3. ISL85014EVAL1Z SCHEMATIC

Bill of Materials

REFERENCE DESIGNATOR	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
U1	1	IC-14A BUCK REGULATOR, 15P, TDFN, 3.5x3.5, ROHS	ISL85014FRZ	INTERSIL
C6	1	CAP-OSCON, SMD, 10.3x10.3mm, 330µF, 25V, 20%, 14mΩ, ROHS	25SVPF330M	SANYO
C4	1	CAP, SMD, 0402, 0.1µF, 50V, 10%, X7R, ROHS	C1005X7R1H104K	TDK
C5	1	CAP, SMD, 0603, 1.0µF, 25V, 10%, X5R, ROHS	GRM188R61E105KA12D	MURATA
C8	1	CAP, SMD, 0603, 2.2µF, 10V, 10%, X7R, ROHS	GRM188R71A225KE15D	MURATA
C10, C11, C12, C18	4	CAP, SMD, 1206, 100µF, 6.3V, 20%, X5R, ROHS	GRM31CR60J107ME39L	MURATA
C9, C13, C14, C17	4	CAP, SMD, 1210, 22µF, 25V, 10%, X7R, ROHS	GRM32ER71E226KE15L	MURATA
J6, J7	2	CONN-SOCKET STRIP, TH, 2P, 2.54mmPITCH, ROHS	310-87-102-41-001101	PRECI-DIP
VDD, SYNC, PG, EN, GND, VIN, PVIN, VOUT	8	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	5002	KEYSTONE
J9, J10, J11	3	CONN-HEADER, 1x3, BREAKAWY 1x36, 2.54mm, ROHS	68001-203HLF	BERG/FCI
L1	1	COIL-PWR CHOKE, SMD, 10x10x9.0mm, 0.68µH, 20%, ROHS	7443330068	WURTH ELEKTRONIK
R7	1	RES, SMD, 0402, 20Ω, 1/16W, 1%, TF, ROHS	ERJ2RKF20R0	PANASONIC
R9	1	RES, SMD, 0402, 0Ω, 1/16W, 5%, TF, ROHS	CR0402-16W-00T	VENKEL
R2, R4, R6	3	RES, SMD, 0402, 100k, 1/16W, 1%, TF, ROHS	ERJ2RKF1003	PANASONIC
R10	1	RES, SMD, 0402, 200Ω, 1/16W, 1%, TF, ROHS	ERJ-2RKF2000X	PANASONIC
R1	1	RES, SMD, 0402, 200k, 1/16W, 1%, TF, ROHS	MCR01MZPF2003	ROHM
C7	1	CAP, SMD, 0402, 1nF, 50V, 10%, X7R, ROHS		MURATA
SW5	1	SWITCH-TOGGLE, SMD, 6PIN, SPDT, 2POS, ON-NONE-ON, ROHS	GT11MSCBE-T	ITT INDUSTRIES/C&K DIVISION
J1, J2	2	CONN-GEN, BIND. POST, INSUL-RED, THMBNUT-GND	111-0702-001	JOHNSONS
J3, J4	2	CONN-GEN, BIND. POST, INSUL-BLK, THMBNUT-GND	111-0703-001	JOHNSONS
Jumper	1	CONN-JUMPER, SHORTING, 2PIN, BLK, OPEN TOP, 2.54mmPITCH, ROHS	929950-00	3M
R3, R5	0	RES, SMD, 0402, DNP, TF, ROHS		
C1, C2, C3, C16	0	CAP, SMD DNP-PLACE HOLDER, ROHS		
PCB	1	PWB-PCB, ISL85014EVAL1Z, REVA, ROHS	ISL85014EVAL1Z	Any

ISL85014EVAL1Z PCB Layout

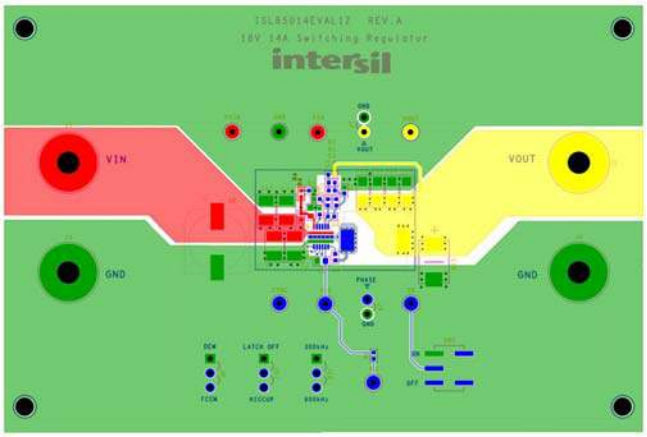

FIGURE 4. TOP LAYER

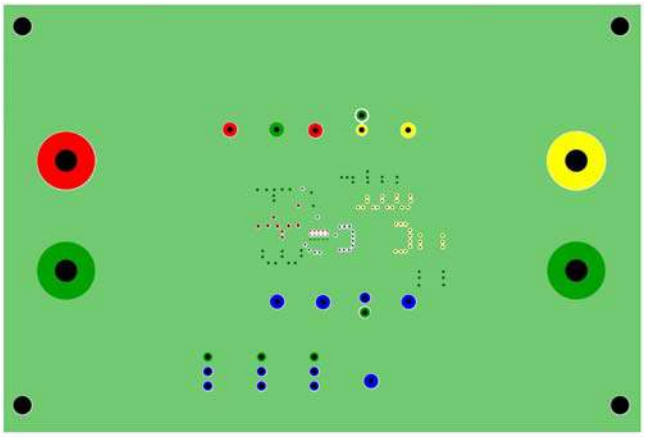

FIGURE 5. LAYER 2

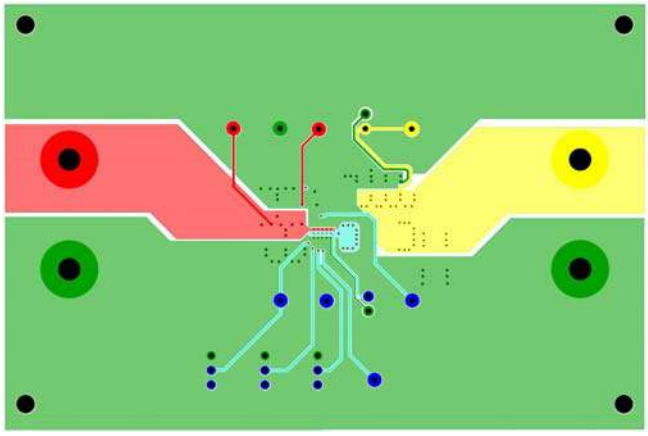

FIGURE 6. LAYER 3

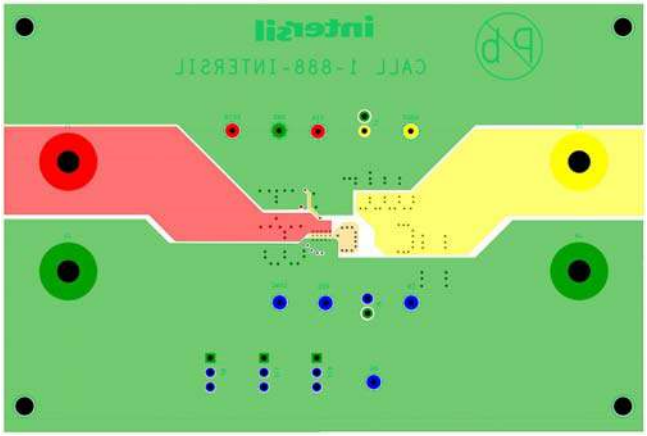

FIGURE 7. BOTTOM LAYER

Typical Performance Curves

V_{IN} = 12V, V_{OUT} = 1.8V, L = 0.68µH, f_{SW} = 600kHz, T_A = +25°C, unless otherwise noted.

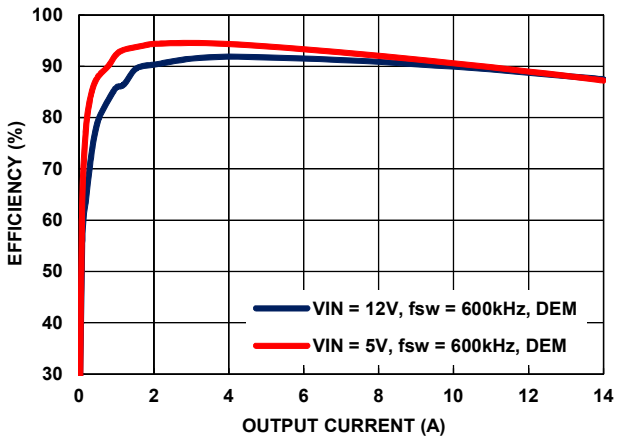

FIGURE 8. EFFICIENCY vs LOAD

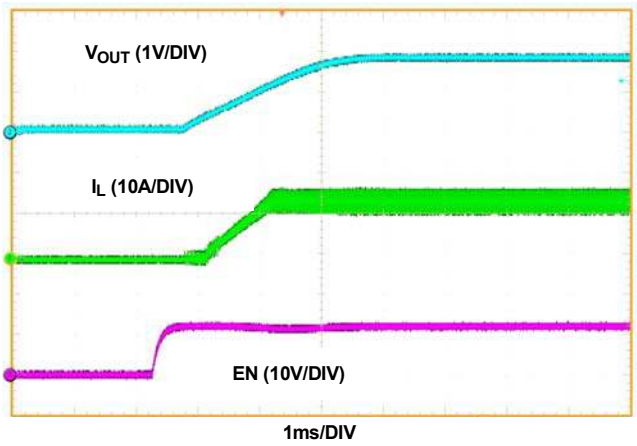

FIGURE 9. START-UP WITH EN, I_{OUT} = 14A

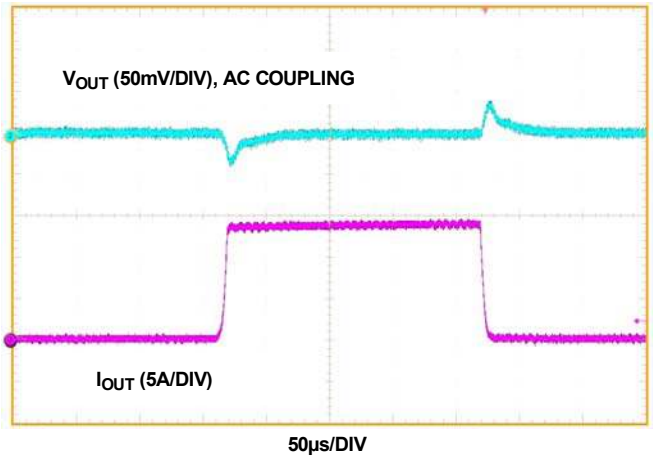

FIGURE 10. LOAD TRANSIENT, 0A → 14A → 0A, 2.5A/µs

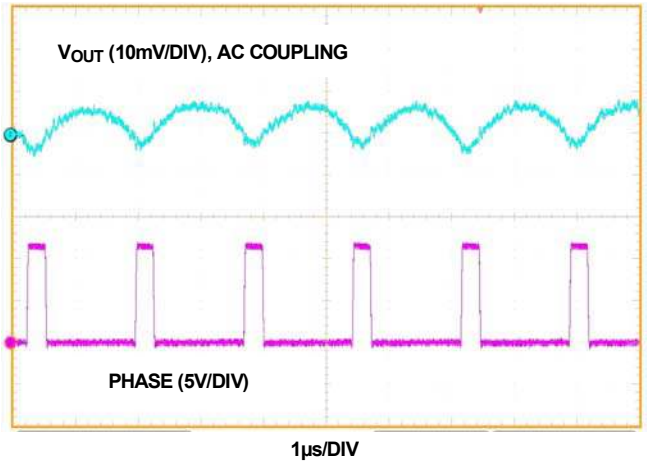

FIGURE 11. OUTPUT VOLTAGE RIPPLE, I_{OUT} = 14A