MGSF1N02L, MVGSF1N02L

[MOSFET](#) - Power:
750 mAmps, 20 Volts

N–Channel SOT–23

These miniature surface mount MOSFETs low $R_{DS(on)}$ assure minimal power loss and conserve energy, making these devices ideal for use in space sensitive power management circuitry. Typical applications are dc–dc converters and power management in portable and battery–powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

Features

- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SOT–23 Surface Mount Package Saves Board Space
- MVGSF Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q101 Qualified and PPAP Capable*
- These Devices are Pb–Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

| Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	Vdc
Gate–to–Source Voltage – Continuous	V_{GS}	± 20	Vdc
Drain Current – Continuous @ T_A = 25°C – Pulsed Drain Current ($t_p \leq 10$ μs)	I_D I_{DM}	750 2000	mA
Total Power Dissipation @ T_A = 25°C	P_D	400	mW
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	300	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
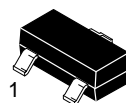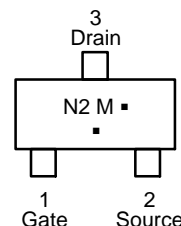
ON Semiconductor®

750 mAMPS, 20 VOLTS
$R_{DS(on)}$ = 90 mΩ

N–Channel
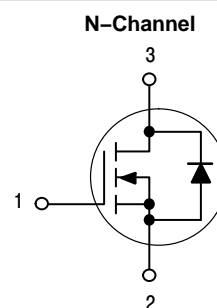
MARKING DIAGRAM/ PIN ASSIGNMENT

SOT–23
CASE 318
STYLE 21

3
Drain

N2 M ▪

1   2
Gate   Source

N2 = Device Code
M = Date Code*
▪ = Pb–Free Package

(Note: Microdot may be in either location)
*Date Code orientation and overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
MGSF1N02LT1G	SOT–23 (Pb–Free)	3000 / Tape & Reel
MVGSF1N02LT1G*	SOT–23 (Pb–Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MGSF1N02L, MVGSF1N02L

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μAdc)	$V_{(BR)DSS}$	20	–	–	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)	I_{DSS}	 – –	 – –	 1.0 10	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	–	–	±100	nAdc
ON CHARACTERISTICS (Note 1)					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)	$V_{GS(th)}$	1.0	1.7	2.4	Vdc
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.2 Adc) (V_{GS} = 4.5 Vdc, I_D = 1.0 Adc)	$r_{DS(on)}$	 – –	 0.075 0.115	 0.090 0.130	Ω
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 5.0 Vdc)	C_{iss}	–	125	–	pF
Output Capacitance (V_{DS} = 5.0 Vdc)	C_{oss}	–	120	–	
Transfer Capacitance (V_{DG} = 5.0 Vdc)	C_{rss}	–	45	–	
SWITCHING CHARACTERISTICS (Note 2)					
Turn–On Delay Time	$t_{d(on)}$	–	2.5	–	ns
Rise Time (V_{DD} = 15 Vdc, I_D = 1.0 Adc,	t_r	–	1.0	–	
Turn–Off Delay Time R_L = 50 Ω)	$t_{d(off)}$	–	16	–	
Fall Time	t_f	–	8.0	–	
Gate Charge (See Figure 6)	Q_T	–	6000	–	pC
SOURCE–DRAIN DIODE CHARACTERISTICS					
Continuous Current	I_S	–	–	0.6	A
Pulsed Current	I_{SM}	–	–	0.75	–
Forward Voltage (Note 2)	V_{SD}	–	0.8	–	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.
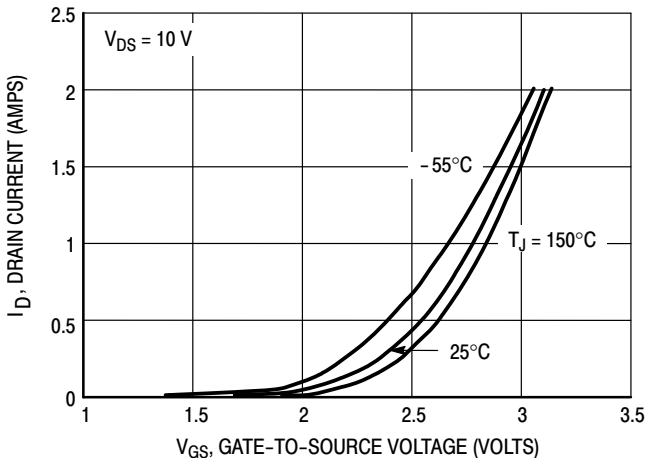
TYPICAL ELECTRICAL CHARACTERISTICS
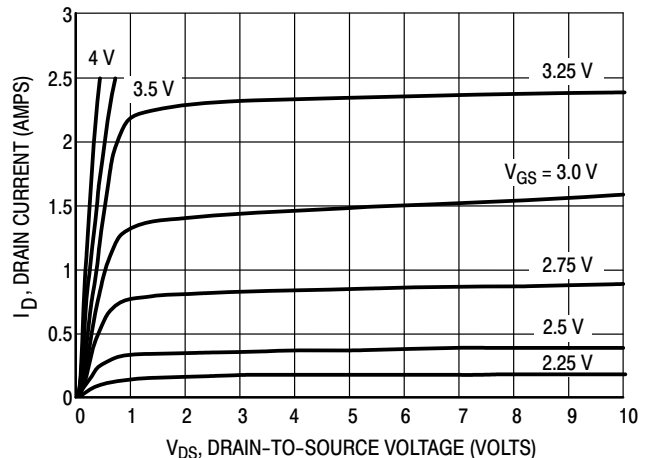

Figure 1. Transfer Characteristics

Figure 2. On–Region Characteristics

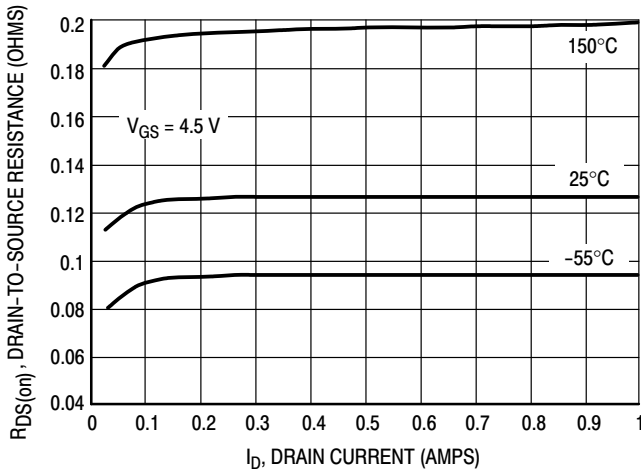## TYPICAL ELECTRICAL CHARACTERISTICS

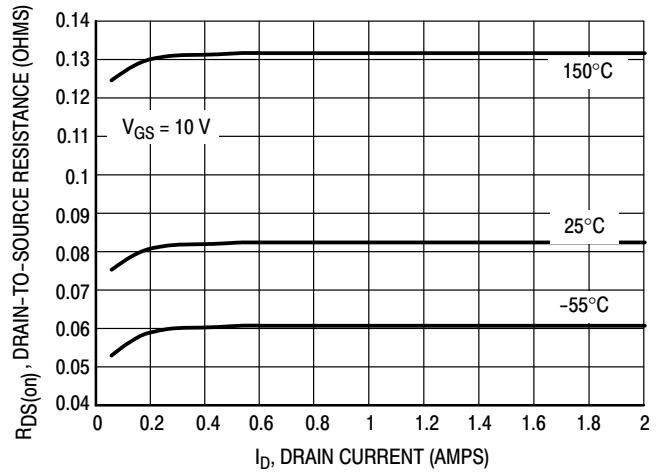Figure 3. On–Resistance versus Drain Current

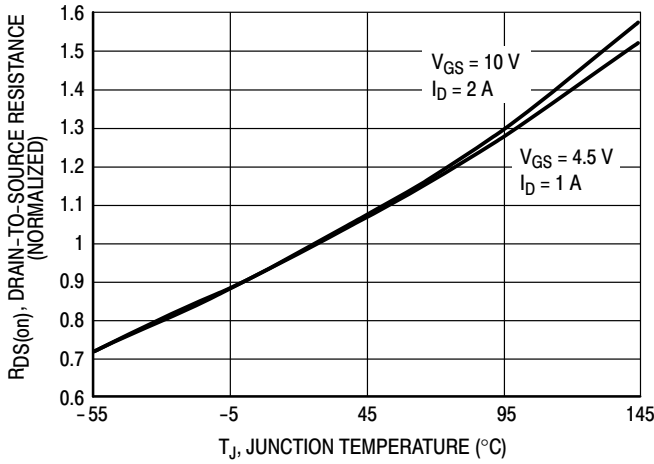Figure 4. On–Resistance versus Drain Current

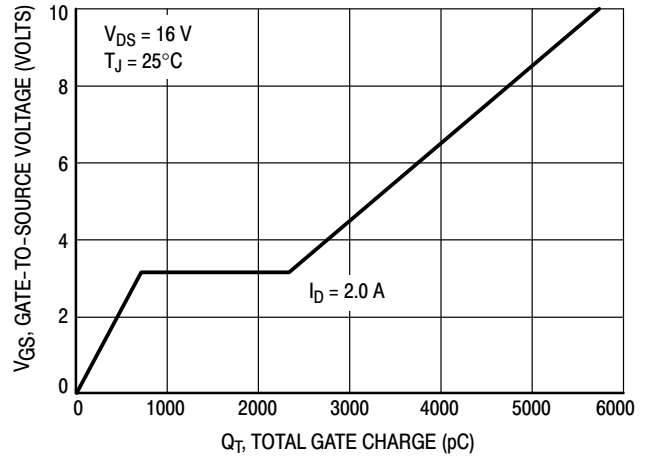Figure 5. On–Resistance Variation with Temperature

Figure 6. Gate Charge

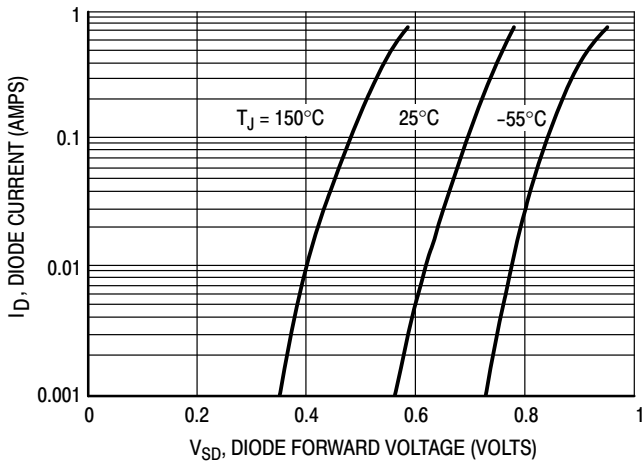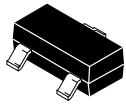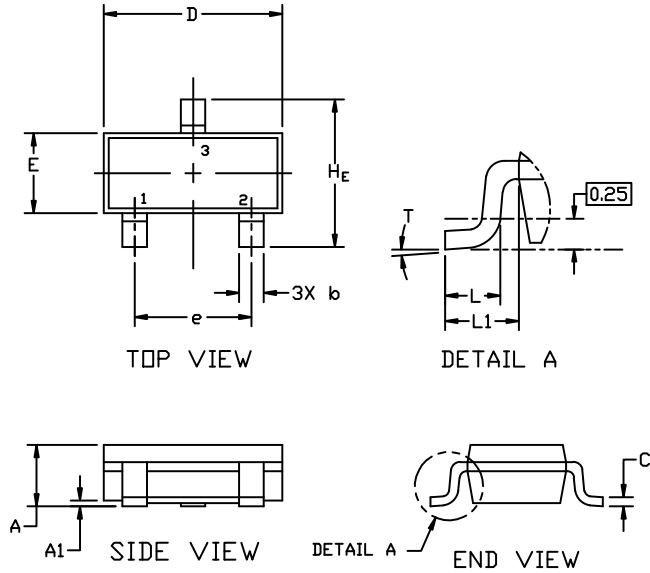Figure 7. Body Diode Forward Voltage
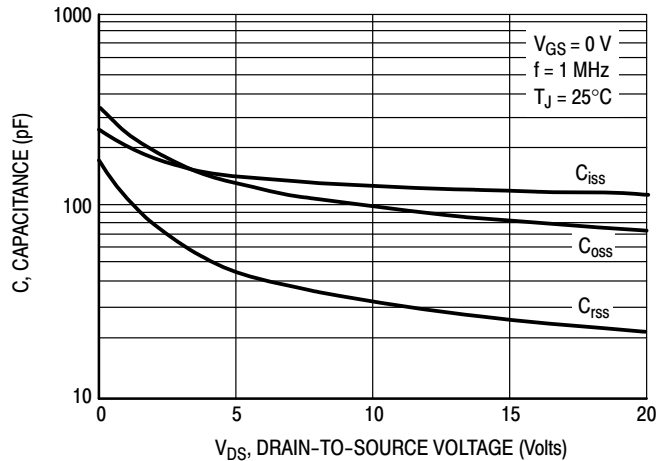
Figure 8. Capacitance

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

SCALE 4:1

TOP VIEW

DETAIL A

SIDE VIEW

DETAIL A

END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.

2. CONTROLLING DIMENSION: MILLIMETERS

3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.

4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*

XXXM▪

1

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

2.90

3X 0.95

3X 0.56

0.95

PITCH
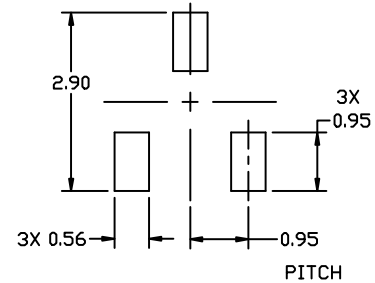
RECOMMENDED MOUNTING FOOTPRINT

∗ For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42226B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOT−23 (TO−236)		PAGE 1 OF 2

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
    2. EMITTER
    3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
    2. BASE
    3. COLLECTOR

STYLE 8:
PIN 1. ANODE
    2. NO CONNECTION
    3. CATHODE

STYLE 9:
PIN 1. ANODE
    2. ANODE
    3. CATHODE

STYLE 10:
PIN 1. DRAIN
    2. SOURCE
    3. GATE

STYLE 11:
PIN 1. ANODE
    2. CATHODE
    3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
    2. CATHODE
    3. ANODE

STYLE 13:
PIN 1. SOURCE
    2. DRAIN
    3. GATE

STYLE 14:
PIN 1. CATHODE
    2. GATE
    3. ANODE

STYLE 15:
PIN 1. GATE
    2. CATHODE
    3. ANODE

STYLE 16:
PIN 1. ANODE
    2. CATHODE
    3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
    2. ANODE
    3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
    2. CATHODE
    3. ANODE

STYLE 19:
PIN 1. CATHODE
    2. ANODE
    3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
    2. ANODE
    3. GATE

STYLE 21:
PIN 1. GATE
    2. SOURCE
    3. DRAIN

STYLE 22:
PIN 1. RETURN
    2. OUTPUT
    3. INPUT

STYLE 23:
PIN 1. ANODE
    2. ANODE
    3. CATHODE

STYLE 24:
PIN 1. GATE
    2. DRAIN
    3. SOURCE

STYLE 25:
PIN 1. ANODE
    2. CATHODE
    3. GATE

STYLE 26:
PIN 1. CATHODE
    2. ANODE
    3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
    2. CATHODE
    3. CATHODE

STYLE 28:
PIN 1. ANODE
    2. ANODE
    3. ANODE

DOCUMENT NUMBER:	98ASB42226B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOT−23 (TO−236)		PAGE 2 OF 2

ADDITIONAL INFORMATION

◊