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S1D13706 Embedded Memory LCD Controller

S5U13706P00C100 Evaluation Board User Manual

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Table of Contents

1 Introduction

This manual describes the setup and operation of the S5U13706P00C100 Evaluation Board. The board is designed as an evaluation platform for the S1D13706 Embedded Memory LCD Controller.

This user manual is updated as appropriate. Please check the Epson Research and Development website at www.erd.epson.com for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

2 Features

Following are some features of the S5U13706P00C100 Evaluation Board:

- 100-pin TQFP S1D13706F00A Embedded Memory LCD Controller with 80K bytes of embedded SRAM.

- Headers for connecting to various Host Bus Interfaces.

- Configuration options.

- Software adjustable backlight intensity support.

- 4/8-bit 3.3V or 5V single monochrome passive LCD panel support.

- 4/8/16-bit 3.3V or 5V single color passive LCD panel support.

- 9/12/18-bit 3.3V or 5V active matrix TFT LCD panel support.

- Direct interface for 18-bit Epson D-TFD LCD panel support.

- Direct interface for 18-bit Sharp HR-TFT LCD panel support.

- Software initiated power save mode.

- Hardware or software Video Invert support.

- External oscillator for CLKI and CLKI2.

3 Installation and Configuration

The S5U13706P00C100 is designed to support as many platforms as possible. The S5U13706P00C100 incorporates a DIP switch and three jumpers which allow both the evaluation board and S1D13706 LCD controller to be configured for a specified evaluation platform.

3.1 Configuration DIP Switches

The S1D13706 has configuration inputs (CNF[7:0]) which are read on the rising edge of RESET#. In order to configure the S1D13706 for multiple Host Bus Interfaces a ten-position DIP switch (S1) is provided. The following figure shows the location of DIP switch SW1 on the S5U13706P00C100.
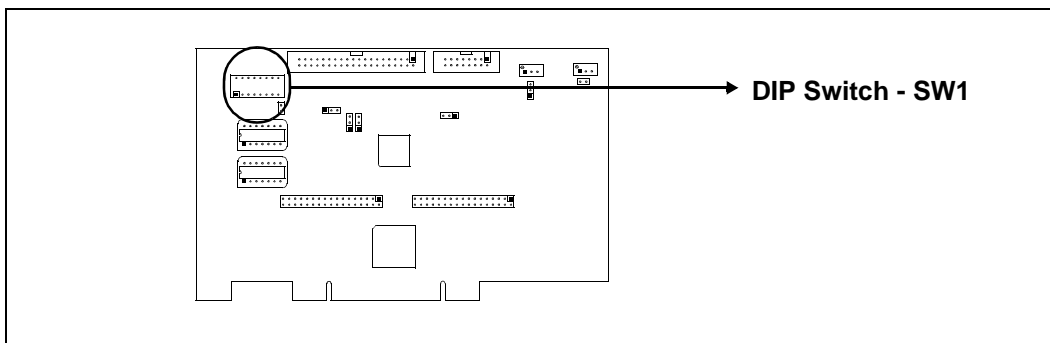

Figure 3-1: Configuration DIP Switch (SW1) Location

The S1D13706 has 8 configuration inputs (CNF[7:0]) which are read on the rising edge of RESET#. All S1D13706 configuration inputs are fully configurable using a ten position DIP switch as described below.

Table 3-1: Configuration DIP Switch Settings

Switch	S1D13706 Signal	Value on this pin at rising edge of RESET# is used to configure:	
		Closed (On/1)	Open (Off/0)
SW1-[3:1]	CNF[2:0]	Select host bus interface as follows: **CNF2 CNF1 CNF0 Host Bus Interface** 0 0 0 SH-4/SH-3 0 0 1 MC68K #1 0 1 0 MC68K #2 0 1 1 Generic #1 1 0 0 Generic #2 1 0 1 RedCap 2 1 1 0 DragonBall 1 1 1 Reserved Note: The host bus interface is 16-bit.	
SW1-4	CNF3	Enable GPIO pins	Enable additional pins for D-TFD/HR-TFT
SW1-5	CNF4	Big Endian bus interface	Little Endian bus interface
SW1-6	CNF5	WAIT# is active high	WAIT# is active low
SW1-[8:7]	CNF[7:6]	CLKI to BClk divide select: **CNF7 CNF6 CLKI to BClk Divide Ratio** 0 0 1 : 1 0 1 2 : 1 1 0 3 : 1 1 1 4 : 1	
SW1-9[1]	-	Hardware Video Invert - invert video data[1]	Hardware Video Invert - normal video data[1]
SW1-10	-	Disable FPGA for non-PCI host	Enable FPGA for PCI host

▢ = Required settings when used with PCI Bridge FPGA

Note

[1] To enable the Hardware Video Invert function the following are required:

- GPIO pins must be enabled (S1-4 closed).

- GPIO0 must be connected to S1-9 (Jumper JP1 set to 1-2).

- GPIO Pin Input Enable (REG[A9h] bit 7) must be set to 1b.

- GPIO0 Pin IO Configuration (REG[A8h] bit 0) must be set to 0b.

- Hardware Video Invert Enable bit (REG[70h] bit 5) must be set to 1b.

3.2 Configuration Jumpers

The S5U13706P00C100 has seven jumper blocks which configure various setting on the evaluation board. The jumper positions for each function are shown below.

Table 3-2: Jumper Summary

Jumper	Function	Position 1-2	Position 2-3	No Jumper
JP1	GPIO0 Connection	GPIO0 connected to SW1-9 for hardware video invert	—	GPIO0 disconnected from SW1-9 for direct HR-TFT/D-TFD or GPIO testing
JP4	GP0 Polarity on H1	Normal (Active High)	Inverted (Active Low)	—
JP6	LCD Panel Voltage	+5V LCDVCC	+3.3V LCDVCC	—

☐ = recommended settings

JP1 - GPIO0 Connection

JP1 selects whether GPIO0 is connected to SW1-9. SW1-9 is used to enable hardware video invert on the S1D13706.
When the jumper is on (position 1-2), SW1-9 controls the hardware video invert feature (default setting).
When the jumper is off, the hardware video invert feature is disabled. This setting must be used for HR-TFT and D-TFD panels as GPIO0 is required for both panels. For details, refer to the *S1D13706 Hardware Functional Specification*, document number X31B-A-001-xx.

Note

When configured for Sharp HR-TFT or Epson D-TFD panels, JP1 must be set to no jumper and JP6 must be set to position 2-3.

Figure 3-2: Configuration Jumper (JP1) Location

JP4 - GPO Polarity on H1

JP4 selects the polarity of the GPO signal available on LCD Connector H1.
Position 1-2 sends the GPO signal directly to H1 (default setting).
Position 2-3 inverts the GPO signal before sending it to H1.

Figure 3-3: Configuration Jumper (JP4) Location

JP6 - LCD Panel Voltage

JP6 selects the voltage level to the LCD panel.
Position 1-2 sets the voltage level to 5.0V.
Position 2-3 sets the voltage level to 3.3V (default setting).

Note

When configured for Sharp HR-TFT or Epson D-TFD panels, JP1 must be set to no jumper and JP6 must be set to position 2-3.

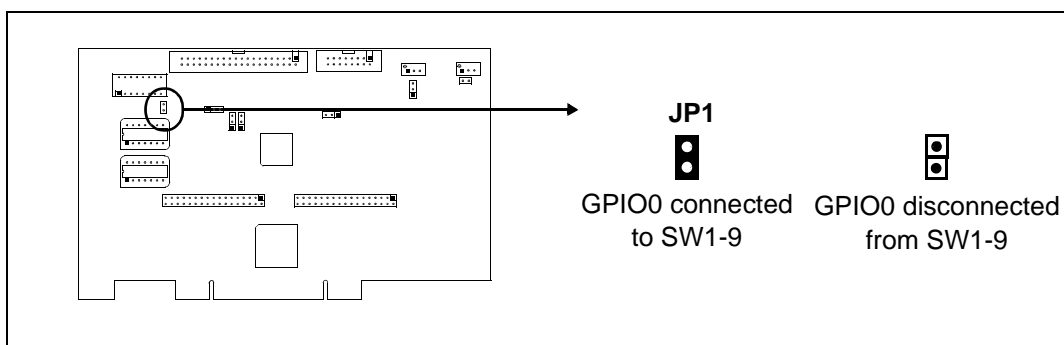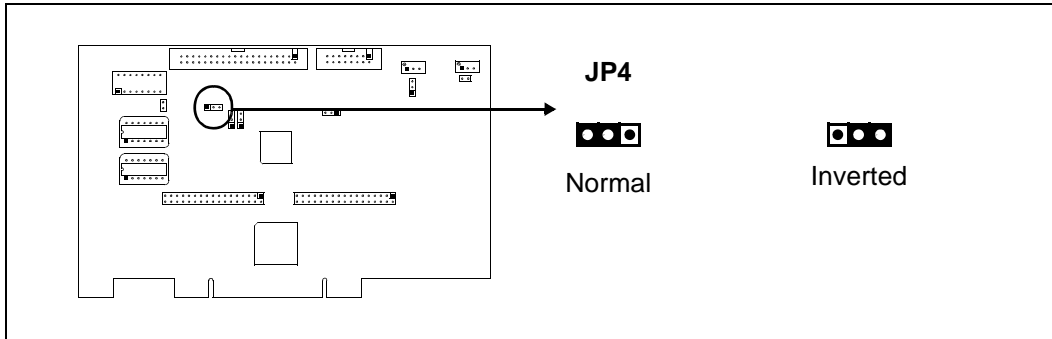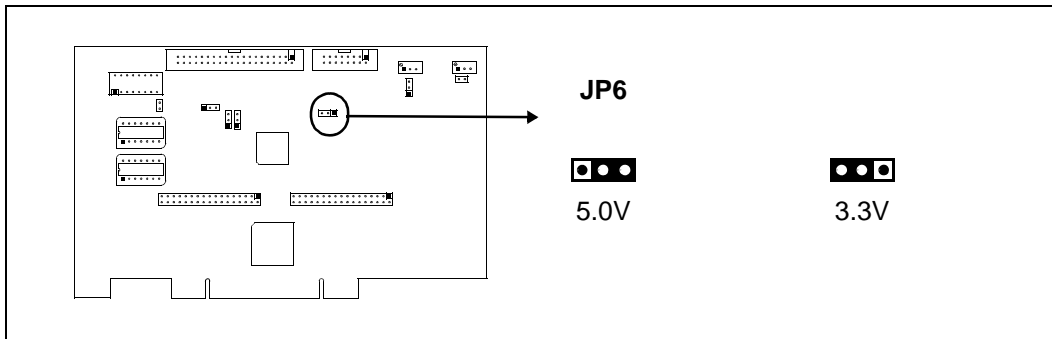*Figure 3-4: Configuration Jumper (JP6) Location*

4 CPU Interface

4.1 CPU Interface Pin Mapping

Table 4-1: CPU Interface Pin Mapping

S1D13706 Pin Name	Generic #1	Generic #2	Hitachi SH-3 /SH-4	Motorola MC68K #1	Motorola MC68K #2	Motorola REDCAP2	Motorola MC68EZ328/ MC68VZ328 DragonBall
AB[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]
AB0	A0[1]	A0	A0[1]	LDS#	A0	A0[1]	A0[1]
DB[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0][2]	D[15:0]	D[15:0]
CS#	External Decode		CSn#	External Decode		CSn#	CSA#
M/R#	External Decode						
CLKI	BUSCLK	BUSCLK	CKIO	CLK	CLK	CLK	CLK
BS#	Connected to V_{DD}[3]		BS#	AS#	AS#	Connected to V_{DD}[3]	
RD/WR#	RD1#	Connected to V_{DD}[3]	RD/WR#	R/W#	R/W#	R/W#	Connected to V_{DD}[3]
RD#	RD0#	RD#	RD#	Connected to V_{DD}[3]	SIZ1	OE#	OE#
WE0#	WE0#	WE#	WE0#	Connected to V_{DD}[3]	SIZ0	EB1#	LWE#
WE1#	WE1#	BHE#	WE1#	UDS#	DS#	EB0#	UWE#
WAIT#	WAIT#	WAIT#	WAIT#/ RDY#	DTACK#	DSACK1#	N/A	DTACK#
RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	RESET#

Note
[1] A0 for these busses is not used internally by the S1D13706.

[2] If the target MC68K bus is 32-bit, then these signals should be connected to D[31:16].

[3] These pins are not used in their corresponding Host Bus Interface mode. Systems are responsible for externally connecting them to the host interface IO V_{DD}.

4.2 CPU Bus Connector Pin Mapping

Table 4-2: CPU Bus Connector (H3) Pinout

Connector Pin No.	Comments
1	Connected to DB0 of the S1D13706
2	Connected to DB1 of the S1D13706
3	Connected to DB2 of the S1D13706
4	Connected to DB3 of the S1D13706
5	Ground
6	Ground
7	Connected to DB4 of the S1D13706
8	Connected to DB5 of the S1D13706
9	Connected to DB6 of the S1D13706
10	Connected to DB7 of the S1D13706
11	Ground
12	Ground
13	Connected to DB8 of the S1D13706
14	Connected to DB9 of the S1D13706
15	Connected to DB10 of the S1D13706
16	Connected to DB11 of the S1D13706
17	Ground
18	Ground
19	Connected to DB12 of the S1D13706
20	Connected to DB13 of the S1D13706
21	Connected to DB14 of the S1D13706
22	Connected to DB15 of the S1D13706
23	Connected to RESET# of the S1D13706
24	Ground
25	Ground
26	Ground
27	+12 volt supply
28	+12 volt supply
29	Connected to WE0# of the S1D13706
30	Connected to WAIT# of the S1D13706
31	Connected to CS# of the S1D13706
32	Connected to MR# of the S1D13706
33	Connected to WE1# of the S1D13706
34	Connected to TXVDD1

Table 4-3: CPU Bus Connector (H4) Pinout

Connector Pin No.	Comments
1	Connected to A0 of the S1D13706
2	Connected to A1 of the S1D13706
3	Connected to A2 of the S1D13706
4	Connected to A3 of the S1D13706
5	Connected to A4 of the S1D13706
6	Connected to A5 of the S1D13706
7	Connected to A6 of the S1D13706
8	Connected to A7 of the S1D13706
9	Ground
10	Ground
11	Connected to A8 of the S1D13706
12	Connected to A9 of the S1D13706
13	Connected to A10 of the S1D13706
14	Connected to A11 of the S1D13706
15	Connected to A12 of the S1D13706
16	Connected to A13 of the S1D13706
17	Ground
18	Ground
19	Connected to A14 of the S1D13706
20	Connected to A15 of the S1D13706
21	Connected to A16 of the S1D13706
22	Not connected
23	Not connected
24	Not connected
25	Ground
26	Ground
27	+5 volt supply
28	+5 volt supply
29	Connected to RD/WR# of the S1D13706
30	Connected to BS# of the S1D13706
31	Connected to BUSCLK of the S1D13706
32	Connected to RD# of the S1D13706
33	Not connected
34	Not connected

5 LCD Interface Pin Mapping

Table 5-1: LCD Signal Connector (H1)

Pin Name	Connector Pin No.	Monochrome Passive Single		Color Passive Panel Single				Color TFT Panel Others			Color TFT Panel Sharp HR-TFT[1]	Color TFT Panel Epson D-TFD[1]
		4-bit	8-bit	4-bit	Format 1 8-bit	Format 2 8-bit	16-Bit	9-bit	12-bit	18-bit	18-bit	18-bit
FPDAT0	1	driven 0	D0	driven 0	D0 (B5)[1]	D0 (G3)[1]	D0 (R6)[1]	R2	R3	R5	R5	R5
FPDAT1	3	driven 0	D1	driven 0	D1 (R5)[1]	D1 (R3)[1]	D1 (G5)[1]	R1	R2	R4	R4	R4
FPDAT2	5	driven 0	D2	driven 0	D2 (G4)[1]	D2 (B2)[1]	D2 (B4)[1]	R0	R1	R3	R3	R3
FPDAT3	7	driven 0	D3	driven 0	D3 (B3)[1]	D3 (G2)[1]	D3 (R4)[1]	G2	G3	G5	G5	G5
FPDAT4	9	D0	D4	D0 (R2)[1]	D4 (R3)[1]	D4 (R2)[1]	D8 (B5)[1]	G1	G2	G4	G4	G4
FPDAT5	11	D1	D5	D1 (B1)[1]	D5 (G2)[1]	D5 (B1)[1]	D9 (R5)[1]	G0	G1	G3	G3	G3
FPDAT6	13	D2	D6	D2 (G1)[1]	D6 (B1)[1]	D6 (G1)[1]	D10 (G4)[1]	B2	B3	B5	B5	B5
FPDAT7	15	D3	D7	D3 (R1)[1]	D7 (R1)[1]	D7 (R1)[1]	D11 (B3)[1]	B1	B2	B4	B4	B4
FPDAT8	17	driven 0	driven 0	driven 0	driven 0	driven 0	D4 (G3)[1]	B0	B1	B3	B3	B3
FPDAT9	19	driven 0	driven 0	driven 0	driven 0	driven 0	D5 (B2)[1]	driven 0	R0	R2	R2	R2
FPDAT10	21	driven 0	driven 0	driven 0	driven 0	driven 0	D6 (R2)[1]	driven 0	driven 0	R1	R1	R1
FPDAT11	23	driven 0	driven 0	driven 0	driven 0	driven 0	D7 (G1)[1]	driven 0	driven 0	R0	R0	R0
FPDAT12	25	driven 0	driven 0	driven 0	driven 0	driven 0	D12 (R3)[1]	driven 0	G0	G2	G2	G2
FPDAT13	27	driven 0	driven 0	driven 0	driven 0	driven 0	D13 (G2)[1]	driven 0	driven 0	G1	G1	G1
FPDAT14	29	driven 0	driven 0	driven 0	driven 0	driven 0	D14 (B1)[1]	driven 0	driven 0	G0	G0	G0
FPDAT15	31	driven 0	driven 0	driven 0	driven 0	driven 0	D15 (R1)[1]	driven 0	B0	B2	B2	B2
FPDAT16	4	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	B1	B1	B1
FPDAT17	6	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	B0	B0	B0
FPSHIFT	33	FPSHIFT									CLK	XSCL
DRDY	35 & 38	MOD		FPSHIFT2	MOD		DRDY				no connect	GCP
FPLINE	37	FPLINE									LP	LP
FPFRAME	39	FPFRAME									SPS	DY
GND	2, 8, 14, 20, 26	GND										
PWMOUT	28	PWMOUT										
NC	30	Not connected										
VCC	32	LCDVCC (3.3V / 5.0V)										
+12V	34	+12V										
NC	36	Not connected										
GPO	40	GPO[2] (for controlling on-board LCD bias power supply on/off)									MOD[3]	GPO[2]

Note

[1]These pin mappings use signal names commonly used for each panel type, however signal names may differ between panel manufacturers. The values shown in brackets represent the color components as mapped to the corresponding FPDATxx signals at the first valid edge of FPSHIFT. For further FPDATxx to LCD interface mapping, see the *S1D13706 Hardware Functional Specification*, document number X31B-A-001-xx.

[2]GPO on H1 can be inverted by setting JP4 to 2-3.

[3]The Sharp HR-TFT MOD signal controls the panel power. This must not be confused with the MOD signal used on many passive panels.

Table 5-2: Extended LCD Signal Connector (H2)

Pin Name	Connector Pin No.	Monochrome Passive Panel		Color Passive Panel				Color TFT Panel				
		Single		Single				Others			HR-TFT[1]	D-TFD[1]
					Format 1	Format 2						
		4-bit	8-bit	4-bit	8-bit	8-bit	16-Bit	9-bit	12-bit	18-bit	18-bit	18-bit
GPIO0	1	GPIO0									PS	XINH
GPIO1	3	GPIO1									CLS	YSCL
GPIO2	5	GPIO2									REV	FR
GPIO3	7	GPIO3									SPL	FRS
GPIO4	9	GPIO4									GPIO4	RES
GPIO5	11	GPIO5									GPIO5	DD_P1
GPIO6	13	GPIO6									GPIO6	YSCLD
CVOUT	15	CVOUT										
GND	2, 4, 6, 8, 10, 12, 14, 16	GND										

Note

[1] When dip switch SW1-4 is open (CNF3 = 0 at RESET#), GPIO[6:0] are at low output states after reset. If REG[10h] bits 1-0 are set for either HR-TFT or D-TFD, some of the pins are used for the HR-TFT or D-TFD interfaces and are not available as GPIO pins.

6 Technical Description

6.1 PCI Bus Support

The S1D13706 **does not** have on-chip PCI bus interface support. The S1D13706P00C100 uses the PCI Bridge FPGA to support the PCI bus.

6.2 Direct Host Bus Interface Support

The S5U13706P00C100 is specifically designed to work using the PCI Bridge FPGA in a standard PCI bus environment. However, the S1D13706 directly supports many other host bus interfaces. Connectors H3 and H4 provide the necessary IO pins to interface to these host buses. For further information on the host bus interfaces supported, see "CPU Interface" on page 11.

Note
> The PCI Bridge FPGA must be disabled using SW1-10 in order for direct host bus interfaces to operate properly.

6.3 S1D13706 Embedded Memory

The S1D13706 has 80K bytes of embedded SRAM. The 80K byte display buffer address space is directly and contiguously available through the 17-bit address bus.

6.4 Software Adjustable LCD Backlight Intensity Support Using PWM

The S1D13706 provides Pulse Width Modulation output on PWMOUT. PWMOUT can be used to control LCD panels which support PWM control of the backlight inverter. The PWMOUT signal is provided on the buffered LCD connector (H1).

6.5 Passive/Active LCD Panel Support

The S1D13706 directly supports:

- 4/8-bit single monochrome passive panels.

- 4/8/16-bit single color passive panels.

- 9/12/18-bit TFT active matrix panels.

- 18-bit Sharp HR-TFT panels.

- 18-bit Epson D-TFD panels.

All the necessary signals are provided on the 40-pin LCD connector, H1, and 16-pin Extended LCD Connector, H2. For connection information, see Section 5, "LCD Interface Pin Mapping" on page 14.

The S5U13706P00C100 does not provide a power supply for the LCD bias voltage needed by passive LCD panels. An external power supply is required to provide the bias LCD voltage to the LCD panel.

6.5.1 Buffered LCD Connector

The buffered LCD connector (H1) provides the same LCD panel signals as those directly from S1D13706, but with voltage-adapting buffers selectable to 3.3V or 5.0V. Pin 32 on this connector provides a voltage level of 3.3V or 5.0V to the LCD panel logic (see "JP6 - LCD Panel Voltage" on page 10 for information on setting the panel voltage).

6.5.2 Extended LCD Connector

The S1D13706 directly supports Sharp 18-bit HR-TFT and Epson 18-bit D-TFD panels. The extended LCD connector (H2) provides the extra signals required to support these panels. The signals on this connector are also buffered from the S1D13706 and adjustable to 3.3V or 5.0V (see "JP6 - LCD Panel Voltage" on page 10 for details on setting the panel voltage).

6.6 External oscillator support for CLKI and CLKI2

The S1D13706 uses CLKI and CLKI2 signals provided by two +5V oscillators. The oscillators are mounted on the evaluation board in 14-pin DIP sockets. The 5V clock signals are shifted to 3.3V which is accepted by the S1D13706.

7 References

7.1 Documents

- Epson Research and Development, Inc., *S1D13706 Hardware Functional Specification*, document number X31B-A-001-xx.

- Epson Research and Development, Inc., *S1D13706 Programming Notes and Examples*, document number X31B-G-003-xx.

7.2 Document Sources

- Epson Research and Development: http://www.erd.epson.com.

8 Parts List

Table 8-1: Parts List

Item	Qty	Reference	Part	Description	Manufacturer / Part No. / Assembly Instructions
1	16	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C13, C16, C17, C18, C19, C20, C21, C25, C27, C29	0.1u	50V X7R +/-5%, 1206 pckg.	Panasonic-ECG ECJ-3VB1H104K. Do not populate C9, C10, C11, C25, C27
2	0	C26, C12	10u 10V	10u 10V	Do not purchase. Do not populate.
3	0	C15, C14	n/p	1206 pckg.	Do not purchase. Do not populate.
4	0	C22, C28	22u 10V	Tantalum C-Size, 10V +/-10%	Do not purchase. Do not populate.
5	9	C23, C38, C39, C40, C41, C42, C43, C44, C45, C46	0.22uF	Ceramic Chip 0.22uF, 50V, X7R +/-5%, 1206 pckg	Kemet C1206C224J5RAC or equivalent capacitor
6	0	C24, C32	10u 63V	Electrolytic, Radial Lead 63V +/-20%	Do not purchase. Do not populate.
7	4	C30, C34, C35, C37	68u 10V	Tantalum D-Size, 68uF,10V, +/-10%	Kemet T491D686K010AS (altern -Panasonic ECST1AD686R (Digikey).
8	0	C31	1n	50V X7R +/-5%, 1206 pckg	Do not purchase. Do not populate.
9	2	C36, C33	33u 20V	Tantalum D-Size, 33uF,20V, +/-10%	Kemet T491D336K020AS (altern -Panasonic ECST1AD336R (Digikey)
10	0	D2, D1	1N5819	Schottky Barrier Rectifier, MELF pckg.	Do not purchase. Do not populate.
11	1	H1	HEADER 20X2	20x2, shrouded header, keyed, straight	Samtec TST-120-01-G-D
12	1	H2	HEADER 8X2	8x2, shrouded header, keyed, straight	Samtec TST-108-01-G-D
13	2	H4, H3	HEADER 17X2	17x2, 0.1" pitch, .025" sq. unshrouded header	Samtec TSW-117-05-G-D
14	1	JP7, JP1	HEADER 2	2x1 .1" pitch unshrouded header	Do not populate JP7
15	2	JP2, JP3, JP4, JP5, JP6	HEADER 3	3x1 .1" pitch unshrouded header	Do not populate JP2, JP3, JP5
16	0	L2, L1	47uH	Shielded SMT power inductor, +/-20%, 1.17A, 0.18 ohm	Do not purchase. Do not populate.
17	0	Q1	MMBT3906	PNP Transistor / SOT-23	Do not purchase. Do not populate.

Table 8-1: Parts List

Item	Qty	Reference	Part	Description	Manufacturer / Part No. / Assembly Instructions
18	0	Q2	MMFT3055VL	N-channel FET, SOT-223 pckg.	Do not purchase. Do not populate.
19	0	Q3	FZT792A	High gain transistor, SOT-223 pckg.	Do not purchase. Do not populate.
20	0	Q4, Q5	MMBT2222A	NPN transistor, SOT-23 pckg.	Do not purchase. Do not populate.
21	14	R1-R9, R33, R36, R37, R38, R39	15K	1206 / 5%	
22	9	R10, R11, R12, R13, R14, R15, R16, R17, R18	330K	1206 / 5%	
23	0	R19	12.4K 1%	1206 / 1%, E-96 series	Do not purchase. Do not populate.
24	0	R20, R21	80K	1206 / 5%	Do not purchase. Do not populate.
25	0	R22	402 1%	1206 / 1%, E-96 series	Do not purchase. Do not populate.
26	0	R23	301 1%	1206 / 1%, E-96 series	Do not purchase. Do not populate.
27	0	R24	200 POT	Trim POT	Do not purchase. Do not populate.
28	0	R25	0.22 1/4W	1210 / 5% / 1/4W	Do not purchase. Do not populate.
29	0	R26	470	1206 / 5%	Do not purchase. Do not populate.
30	0	R27	22K	1206 / 5%	Do not purchase. Do not populate.
31	1	R28, R29, R32	100K	1206 / 5%	Do not populate R28, R29
32	0	R30	1.2M	1206 / 5%	Do not purchase. Do not populate.
33	0	R31	500K POT	Trim POT	Do not purchase. Do not populate.
34	3	R34, R35, R40, R41	1K	1206 / 5%	Do not populate R41
35	1	SW1	SW DIP-10	Dip Switch 10-Position	Grayhill 76SB10ST (Digikey GH1117-ND)
36	0	S1	SW DIP-4	DIP switch, 4-position	Do not purchase. Do not populate.
37	1	U1	S1D13706F00A	100-pin TQFP15 surface mount package	
38	0	U2	LT1117CST-5	5V fixed voltage regulator, SOT-223	Do not purchase. Do not populate.
39	1	U3	74AHC04	SO-14 package	TI 74AHC04, SO-14 package
40	0	U4	ICD2061A	Wide SO-16 package	Do not purchase. Do not populate.

Table 8-1: Parts List

| Item	Qty	Reference	Part	Description	Manufacturer / Part No. / Assembly Instructions
41	2	U6, U5	Test Socket	14 pin narrow DIP, screw machine socket	
42	4	U7, U8, U9, U10	74HCT244	Buffer, SO-20 package	TI74HCT244 or equivalent
43	0	U11	MAX754	16 pin narrow SO pckg.	Do not purchase. Do not populate.
44	1	U12	LT1117CM-3.3	3.3V fixed voltage regulator, 3 Lead Plastic DD	Linear Technology LT1117CM-3.3
45	0	U13	MAX749	8 pin SO pckg.	Do not purchase. Do not populate.
46	1	U14	EPF6016TC144-2	144-pin QFP	Altera EPF6016TC144-2
47	1	U15	8-pin DIP socket	8-pin DIP socket	Machined socket, 8-pin
48	1	(U15)	EPC1PI8N	8-pin DIP pckg	Altera EPC1PI8N, programmed, socketed
49	0	Y1	14.31818MHz	Vertical-mount HC-49	Do not purchase. Do not populate.
50	3	(JP1), (JP4), (JP6)	Micro Shunt		
51	1		Bracket	Computer Bracket, Blank - PCI	Keystone - Cat. No. 9203
52	2		Screw	Pan head, #4-40 x 1/4"	Screw, pan head, #4-40 x 1/4"-please assemble bracket onto board
53	2	Resistor SMD 0805 0ohm	0	0805 Resistor, 0 ohm	please mount on solder side to short pins 2-3 of JP2 and JP3
54	1	(U6)	50MHz	Oscillator DIP14, 50MHz	Epson SG8002DB, 50MHz, socketed
55	1	(U5)	6.5MHz	Oscillator DIP14, 6.5MHz	Epson SG8002DB, 6.5MHz, socketed

9 Schematics
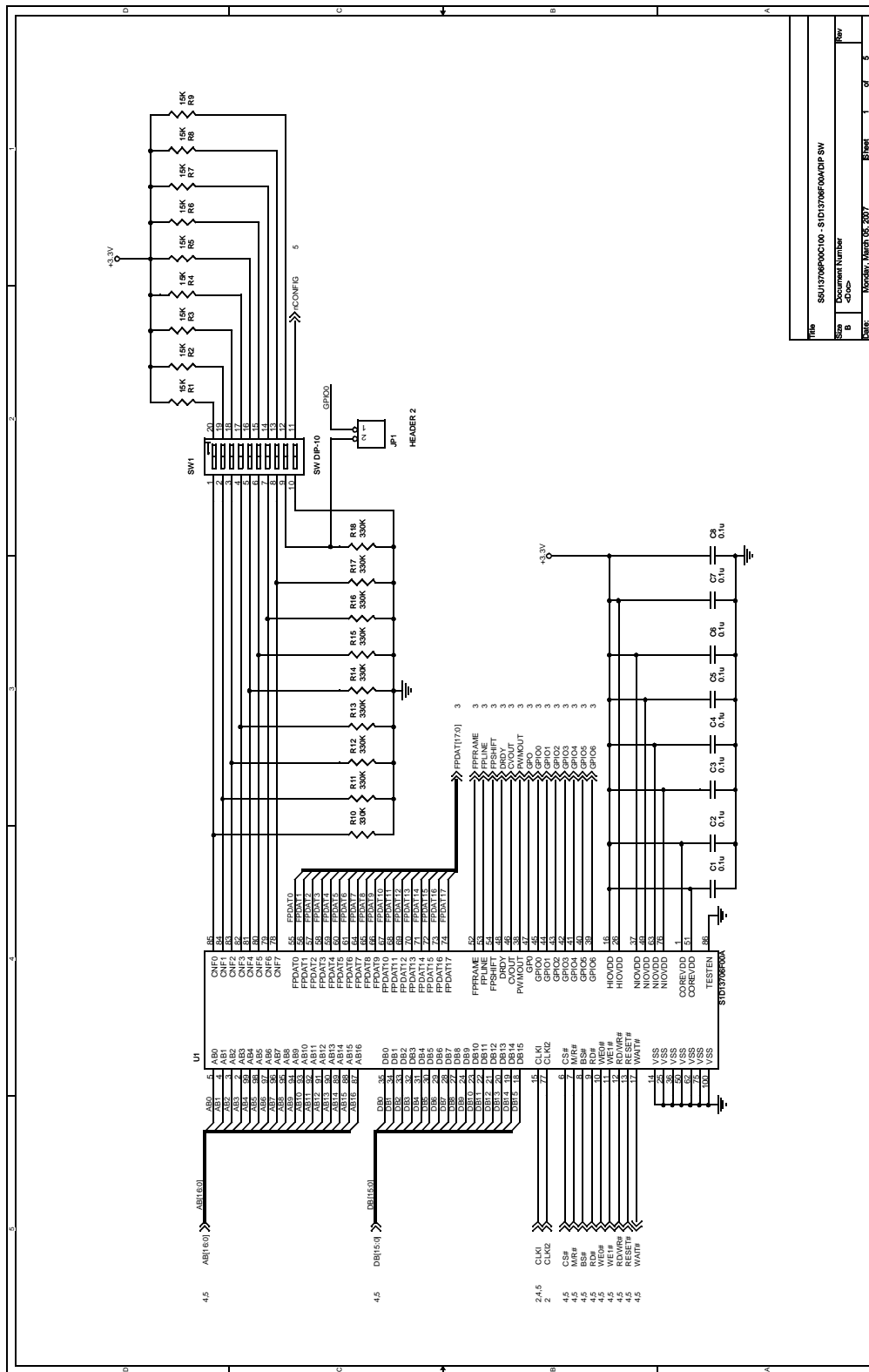
Figure 9-1: S5U13706P00C100 Schematics (1 of 5)
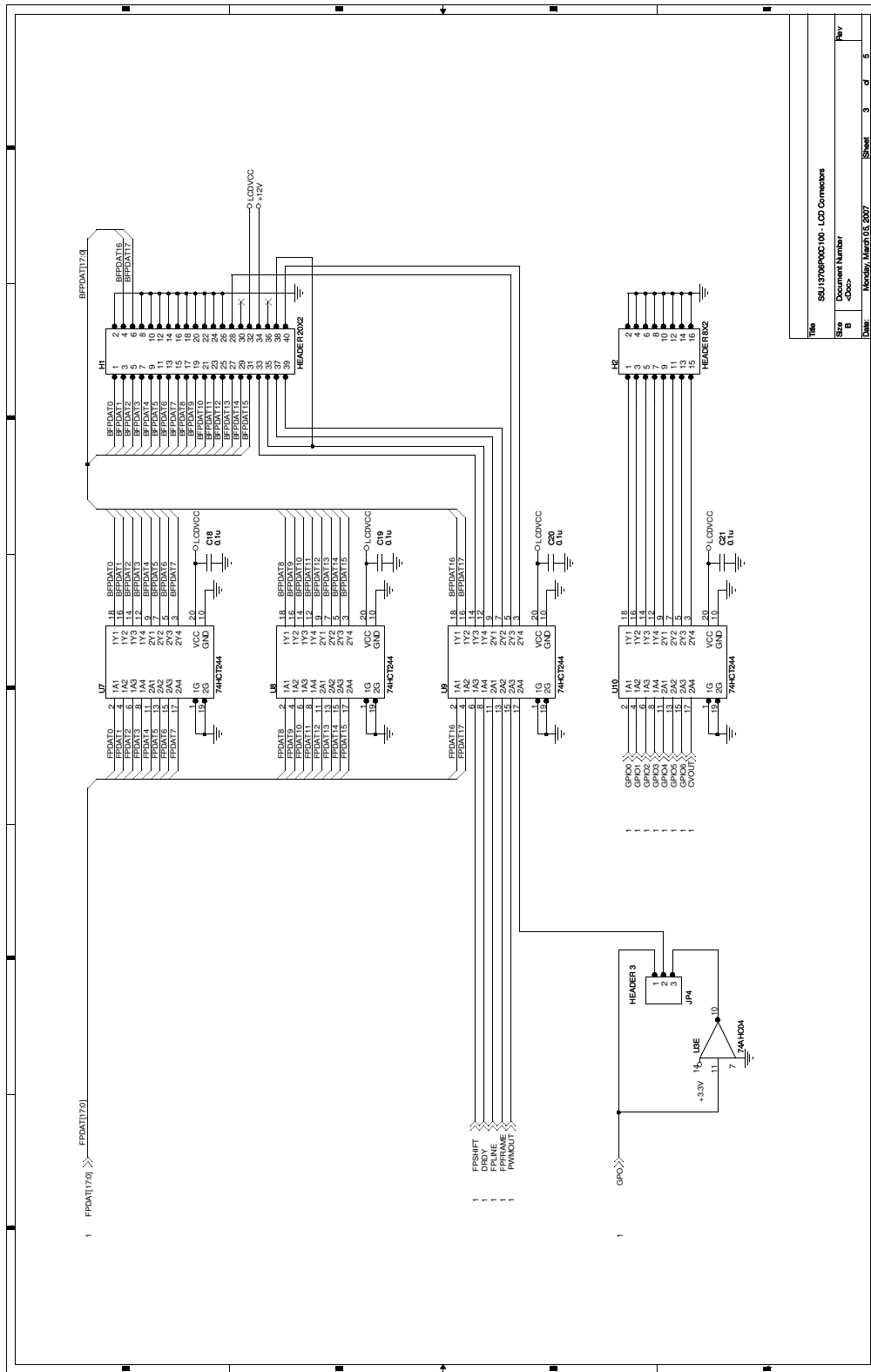
Figure 9-2: S5U13706P00C100 Schematics (2 of 5)

Figure 9-3: S5U13706P00C100 Schematics (3 of 5)
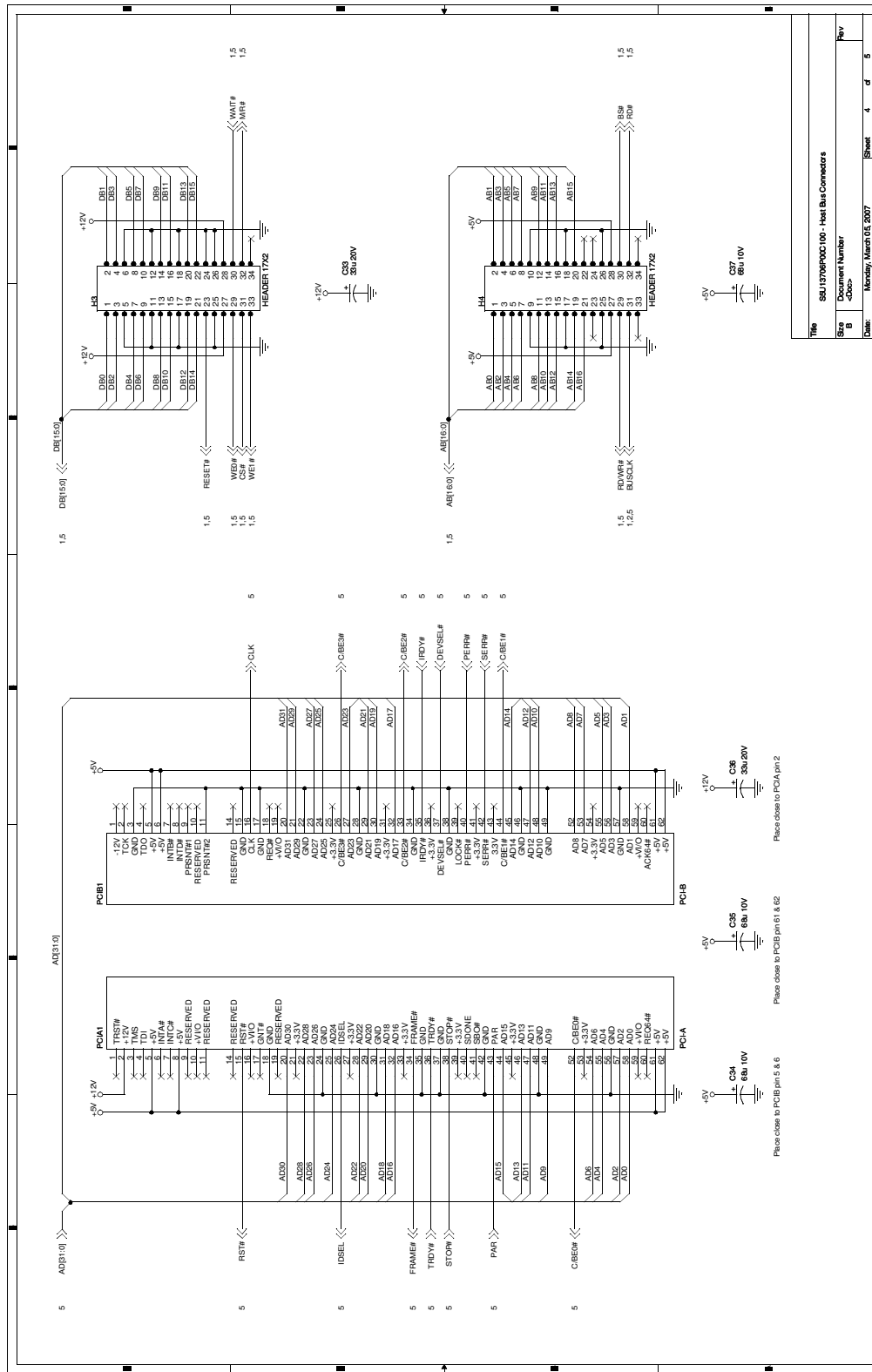
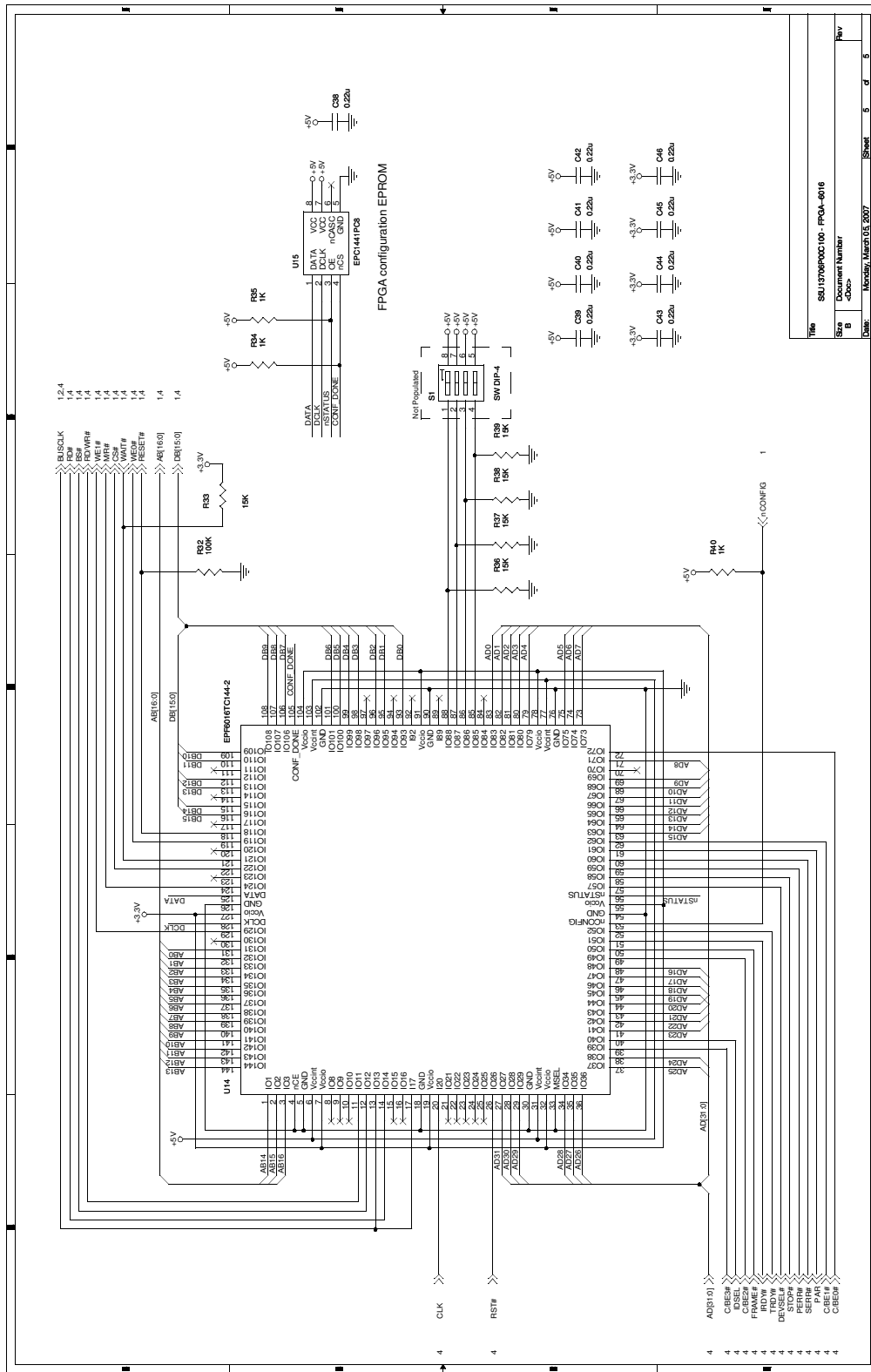*Figure 9-4: S5U13706P00C100 Schematics (4 of 5)*

Figure 9-5: S5U13706P00C100 Schematics (5 of 5)
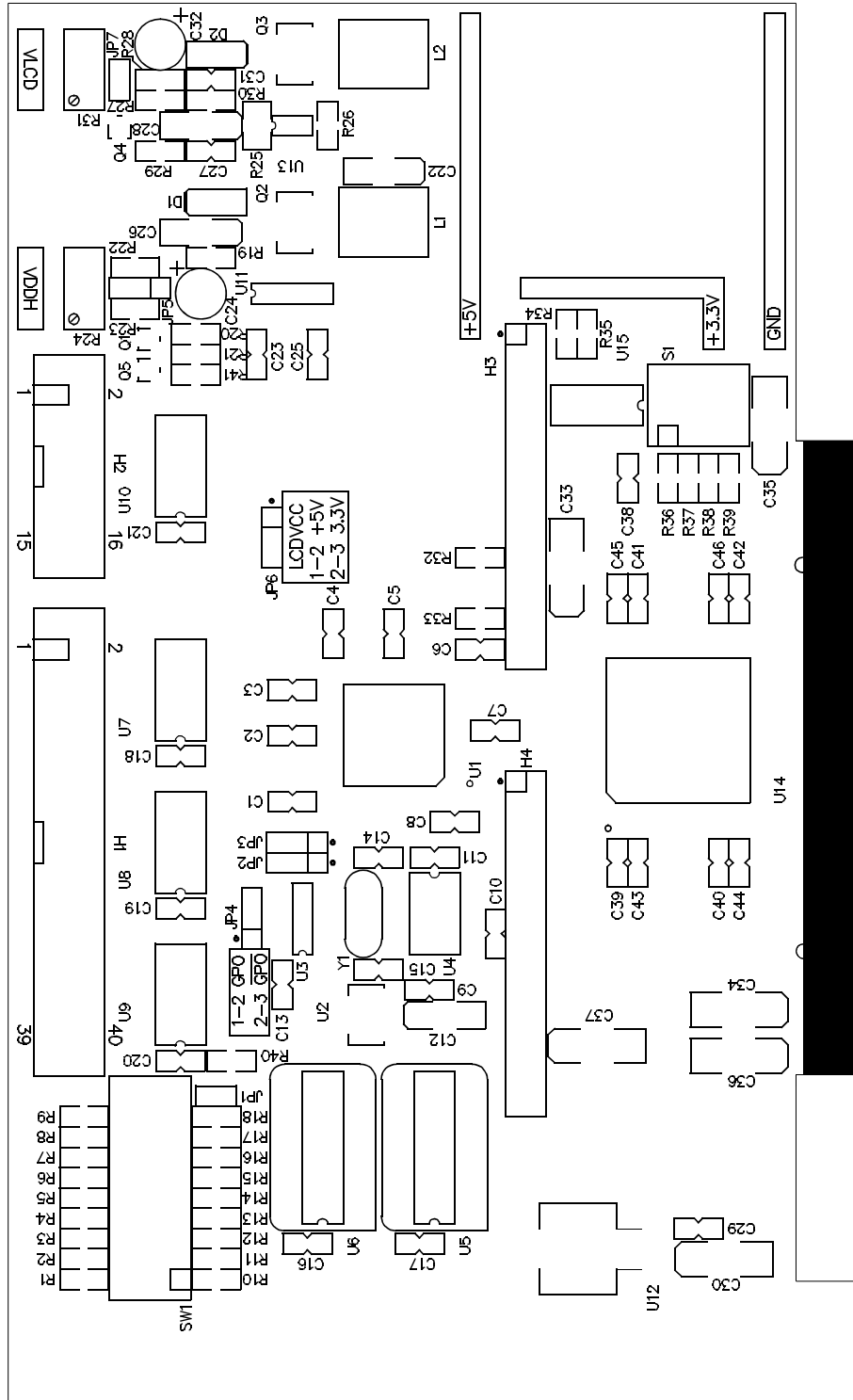
10 Board Layout

Figure 10-1: S5U13706P00C100 Board Layout

11 Technical Support

11.1 EPSON LCD Controllers (S1D13706)

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Change Record

X31B-G-021-01   Revision 1.1 - Issued: March 03, 2009

- section 11 - update sales office addresses

X31B-G-021-01   Revision 1.0 - Issued: March 19, 2007

- initial draft
- minor edits
- added parts list
- added schematics
- updated tech support contact information