- **Fully Supports Provisions of IEEE 1394-1995 Standard for High Performance Serial Bus**
- **Fully Interoperable with FireWire™ and i.LINK™ Implementation of IEEE 1394-1995**
- **Provides Three Fully Compliant Cable Ports at 100/200 Megabits per Second (Mbits/s)**
- **Cable Ports Monitor Line Conditions for Active Connection to Remote Node**
- **Device Power-Down Feature to Conserve Energy in Battery-Powered Applications**
- **Inactive Ports Disabled to Save Power**
- **Logic Performs System Initialization and Arbitration Functions**
- **Encode and Decode Functions Included for Data-Strobe Bit-Level Encoding**
- **Incoming Data Resynchronized to Local Clock**
- **Single 3.3-V Supply Operation**
- **Interface to Link-Layer Controller Supports Low Cost TI™ Bus-Holder Isolation**
- **Data Interface to Link-Layer Controller Provided Through 2/4 Parallel Lines at 49.152 MHz**
- **Low Cost 24.576-MHz Crystal Oscillator and PLL Provide Transmit/Receive Data at 100/200 Mbits/s, and Link-Layer Controller Clock at 49.152 MHz**
- **Interoperable with 1394 Link-Layer Controllers Using 5-V Supplies**
- **Interoperable Across 1394 Cable with 1394 Physical Layers (Phy) Using 5-V Supplies**
- **Node Power-Class Information Signaling for System Power Management**
- **Cable Power Presence Monitoring**
- **Separate Cable Bias and Driver Termination Voltage Supply for Each Port**
- **High Performance 64-Pin TQFP (PM) Package and 68-Pin CFP (HV) Package**

description

The TSB21LV03C provides the analog and digital physical layer functions needed to implement a three-port node in a cable-based IEEE 1394-1995 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The TSB21LV03C is designed to interface with a link-layer controller (LLC), such as the TSB12LV21, TSB12LV31, TSB12C01, TSB12LV22, TSB12LV41, or TSB12LV01.

The TSB21LV03C requires either an external 24.576-MHz crystal or crystal oscillator. The internal oscillator drives an internal phase-locked loop (PLL), which generates the required 196.608-MHz reference signal. The 196.608-MHz reference signal is internally divided to provide the 49.152/98.304-MHz clock signals that control transmission of the outbound encoded strobe and data information. The 49.152-MHz clock signal is also supplied to the associated LLC for synchronization of the two chips and is used for resynchronization of the received data. For the TSB21LV03C, the 49.152 MHz clock output is active when $\overline{\text{RESET}}$ is asserted low. The power-down function, when enabled by taking the PD terminal high, stops operation of the PLL and disables all circuitry except the cable-not-active signal circuitry.

The TSB21LV03C supports an optional isolation barrier between itself and its LLC. When $\overline{\text{ISO}}$ is tied high, the link interface outputs behave normally. Also, when $\overline{\text{ISO}}$ is tied high, the internal bus hold function is enabled for use with the TI Bus Holder isolation. TI bus holder isolation is implemented when $\overline{\text{ISO}}$ is tied high.

FireWire is a trademark of Apple Computer, Incorporated.
i.LINK is a trademark of SONY.
TI is a trademark of Texas Instruments Incorporated.

description (continued)

Data bits to be transmitted through the cable ports are received from the LLC on two or four data lines (D0 – D3), and are latched internally in the TSB21LV03C in synchronization with the 49.152-MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304 or 196.608 Mbits/s as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the TPB cable pair(s), and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

During packet reception the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded Strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are split into two or four parallel streams, resynchronized to the local system clock, and sent to the associated LLC. The received data is also transmitted (repeated) out of the other active (connected) cable ports.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common mode voltage is used during arbitration to set the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage for the presence of the remotely supplied twisted-pair bias voltage. The presence or absence of this common-mode voltage is used as an indication of cable connection status. The cable connection status signal is internally debounced in the TSB21LV03C on a cable disconnect-to-connect. The debounced cable connection status signal initiates a bus reset. On a cable disconnect-to-connect a debounce delay is incorporated. There is no delay on a cable disconnect.

The TSB21LV03C provides a 1.86-V nominal bias voltage for driver load termination. This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. The value of this bias voltage has been chosen to allow interoperability between transceiver chips operating from either 5-V or 3-V nominal supplies. This bias voltage source should be stabilized by using an external filter capacitor of approximately 1.0 μF.

The transmitter circuitry is disabled under the following conditions: power down, cable not active, reset, or transmitter disable. The receiver circuitry is disabled under the following conditions: power down, cable not active, or receiver disable. The twisted-pair bias voltage circuitry is disabled under the following conditions: power down or reset. The power-down condition occurs when the PD input is high. The cable-not-active (CNA) condition occurs when the cable connection status indicates that no cable is connected. The reset condition occurs when the $\overline{\text{RESET}}$ input terminal is low. The transmitter disable and receiver disable conditions are determined from the internal logic.

The line drivers in the TSB21LV03C operate in a high-impedance current mode and are designed to work with external 110-Ω line-termination resistor networks. One network is provided at each end of each twisted-pair cable. Each network is composed of a pair of series-connected 55-Ω resistors. The midpoint of the pair of resistors that is directly connected to the twisted-pair A (TPA) package terminals is connected to the TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the twisted-pair B (TPB) package terminals is coupled to ground through a parallel RC network with recommended resistor and capacitor values of 5 kΩ and 220 pF respectively. The values of the external resistors are designed to meet the draft standard specifications when connected in parallel with the internal receiver circuits and are shown in Figure 3.

The driver output current, along with other internal operating currents, is set by an external resistor. This resistor is connected between the R0 and R1 terminals and has a value of 6.3 kΩ, ±0.5%. This might be accomplished by placing a 6.34 kΩ, ±0,5% resistor in parallel with a 1-MΩ resistor.

description (continued)

Four package terminals are used as inputs to set four configuration status bits in the self-identification (Self-ID) packet. These terminals are hardwired high or low as a function of the equipment design. PC0 – PC2 are the three terminals that indicate either the need for power from the cable or the ability to supply power to the cable. The fourth terminal, C/LKON, indicates whether a node is a contender for bus manager. When the C/LKON terminal is asserted, it means the node can be a contender for bus manager. When the terminal is not asserted, it means that the node is not a contender. The C bit corresponds to bit 20 in the Self-ID packet, PC0 corresponds to bit 21, PC1 corresponds to bit 22, and PC2 corresponds to bit 23 (see Table 4–29 of the IEEE 1394–1995 standard for additional details).

A power-down terminal, PD, is provided to allow a power-down mode where most of the TSB21LV03C circuits are powered down to conserve energy in battery-powered applications. A cable status terminal, CNA, provides a high output when all twisted-pair cable ports are disconnected. This output is not debounced. The CNA output can be used to determine when to power the TSB21LV03C down or up. In the power-down mode all circuitry is disabled except the CNA circuitry. It should be noted that when the device is powered-down it does not act in a repeater mode. When the TSB21LV03C is powered down using the PD terminal, the twisted-pair transmitter and receiver circuitry has been designed to present a high impedance to the cable to prevent loading the TPBias terminal voltage on the other end of the cable.

NOTE:

Reference suspend/resume section in the current 1394a specification for interoperability with PD implementation of power down.

If the TSB21LV03C is being used with one or more of the ports not being brought out to a connector, the TPB terminals must be terminated for reliable operation. For each unused port, the TPB+ and TPB– terminals must be connected to GND. This is done in the normal termination network. When a port does not have a cable connected, the normal termination network pulls TPB+ and TPB– to ground through a 5-kΩ resistor, thus disabling the port.

NOTE:

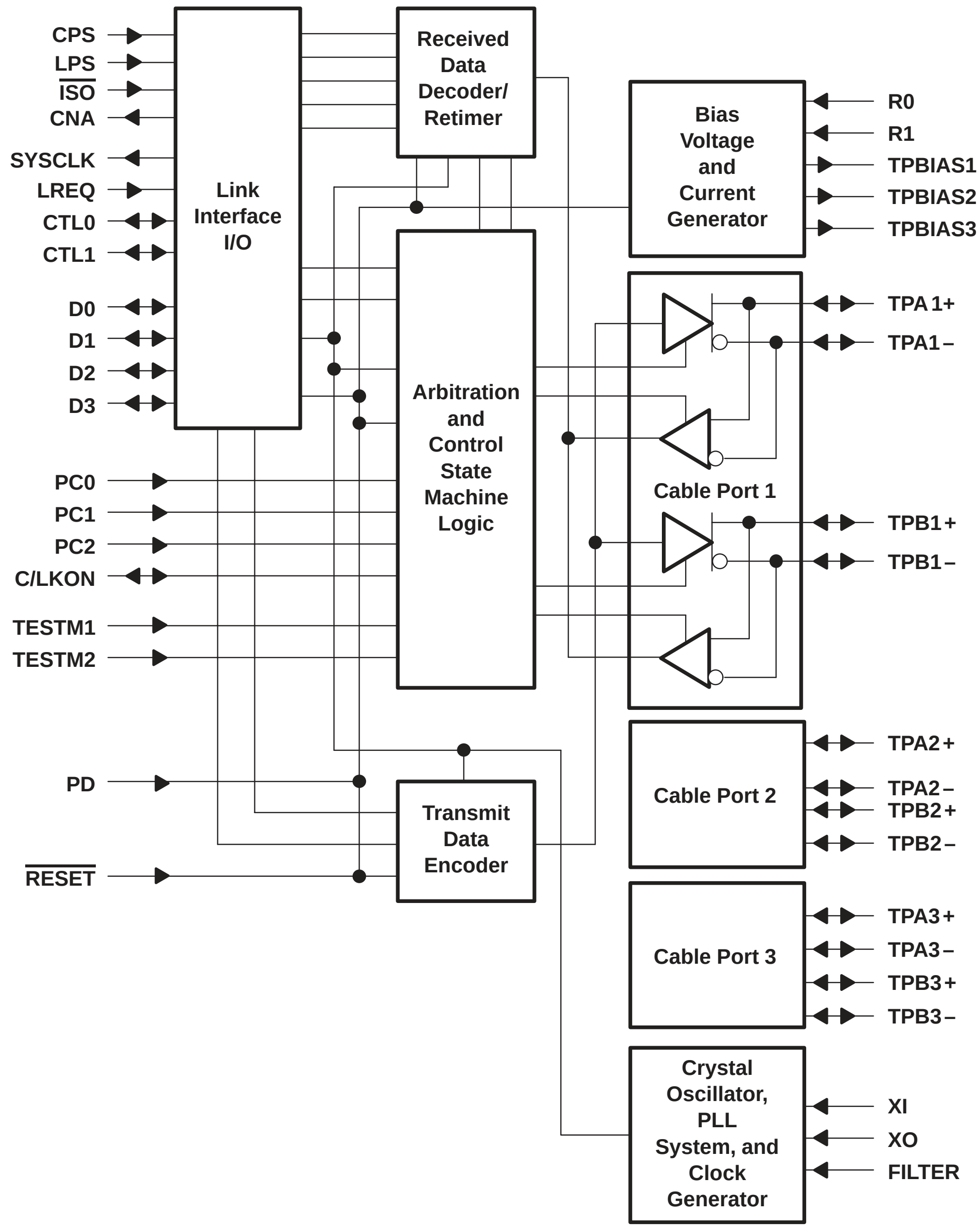
All gap counts on all nodes of a 1394 bus must be identical. This may only be accomplished by using phy configuration packets (see section 4.3.4.3 of IEEE 1394-1995 Standard) or by using two bus resets, which resets the gap counts to the maximum level (3 Fh).

The link power status (LPS) terminal works with the C/LKON terminal to manage the LLC power usage of the node. The LPS terminal indicates that the LLC of the node is powered down and powers down the phy-LLC interface to save power. If the phy then receives a link-on packet, the C/LKON terminal is activated to output a 6.114 MHz signal, which can be used by the LLC to power itself up. Once the LLC is powered up, the LPS signal communicates this to the TSB21LV03C and the C/LKON signal is turned off and the phy-link interface is enabled.

Two of the package terminals are used to set up various test conditions used in manufacturing. These terminals, TESTM1 and TESTM2, should be connected to V_{DD} for normal operation.

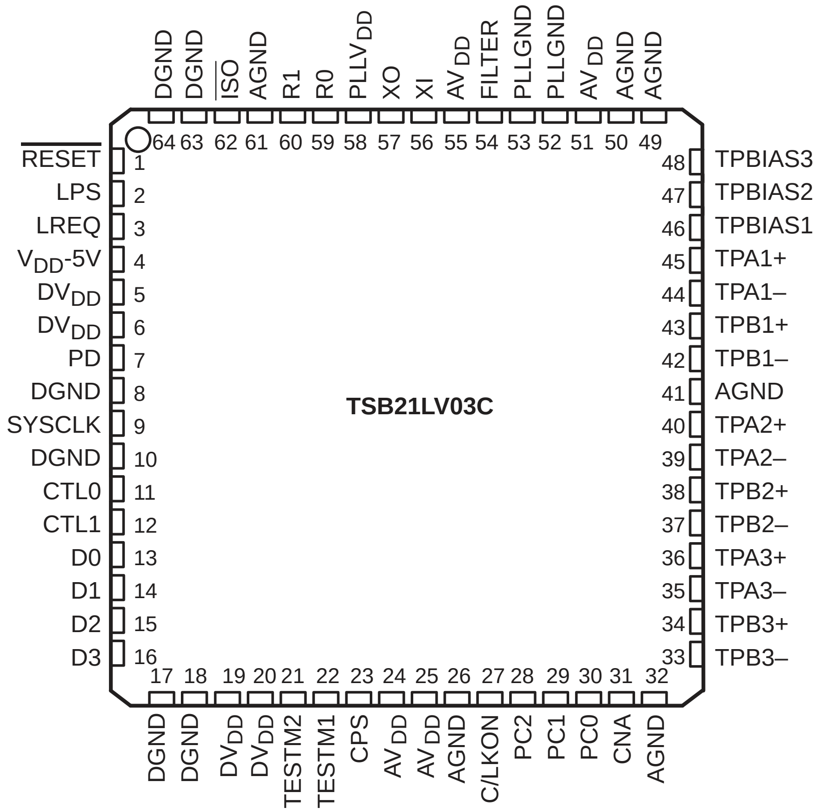
The TSB21LV03C is characterized for operation from 0°C to 70°C. The TSB21LV03CI is characterized for operation from –40°C to 85°C. The TSB21LV03CM is characterized for operation over the full military temperature range of –55°C to 125°C.

functional block diagram

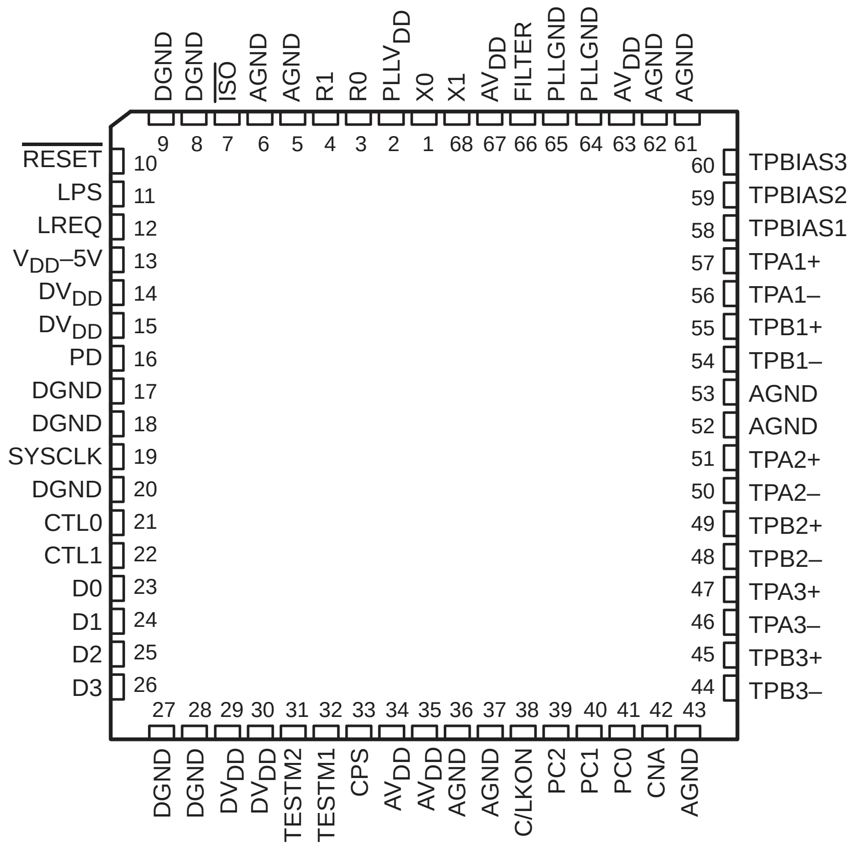


package outline

PLASTIC QUAD FLATPACK (PM)
(TOP VIEW)



CERAMIC QUAD FLATPACK (HV)
(TOP VIEW)



AVAILABLE OPTIONS

T_A	PACKAGE	
	PLASTIC QUAD FLAT PACK (PM)	CERAMIC QUAD FLAT PACK (HV)
0°C to 70°C	TSB21LV03CPM	—
–40°C to 85°C	TSB21LV03CIPM	—
–55°C to 125°C	—	TSB21LV03CMHVB

Terminal Functions

TERMINAL			TYPE	I/O	DESCRIPTION
NAME	NO.				
	HV	PM			
AGND	5, 6, 36, 37, 43, 52, 53, 61, 62	26, 32, 41, 49, 50, 61	Supply	—	Analog circuit ground. All AGND terminals should be tied together to the low-impedance circuit-board ground plane. External to the device, AGND should be tied to DGND and PLLGND.
AV_{DD}	34, 35, 63, 67	24, 25, 51, 55	Supply	—	Analog circuit power. A combination of high frequency decoupling capacitors near each AV_{DD} terminal is suggested, such as 0.1-μF and 0.001-μF capacitors. Lower frequency 10-μF filtering capacitors are also recommended. AV_{DD} terminals are separated from DV_{DD} terminals internally from the other supply terminals to provide noise isolation. They should be tied together to a power plane on the circuit board. Each supply source should be individually filtered.
C/LKON	38	27	CMOS	I/O	Bus manager capable (input). When set as an input, C/LKON specifies in the Self-ID packet that the node is bus manager capable. The bit value programming is done by tying the terminal through a 10-kΩ resistor to V_{DD} (high, bus manager capable) or to GND (low, not bus manager capable). Using either the pullup or pulldown resistor allows the LINK ON output to override the input bit value when necessary.
					Link-on (output). When set as an output, C/LKON indicates the reception of a link-on message by asserting a 6.114-MHz signal.
CNA	42	31	CMOS	O	Cable-not-active output. CNA is asserted high when none of the TSB21LV03C ports are connected to another active port. This circuit remains active during the power-down mode.
CPS	33	23	CMOS	I	Cable power status. CPS is normally connected to the cable power through a 400-kΩ resistor. This circuit drives an internal comparator that detects the presence of cable power. This information is maintained in two internal registers and is available to the LLC by way of a register read (see the Phy-Link Interface Annex in the IEEE 1394-1995 standard).
CTL0 CTL1	21 22	11 12	CMOS	I/O	Control I/O. The CTLn terminals are bidirectional communications control signals between the TSB21LV03C and the LLC. These signals control the passage of information between the two devices. Control I/O terminals are 5-V tolerant. The CTLn terminals have an internal bus-holder function built-in.
D0 – D3	23, 24, 25, 26	13, 14, 15, 16	CMOS	I/O	Data I/O. The D terminals are bidirectional and pass data between the TSB21LV03C and the LLC. Data I/O terminals are 5-V tolerant. The D terminals have an internal bus-holder function built-in.
DGND	8, 9, 17, 18, 20, 27, 28	8, 10, 17, 18, 63, 64	Supply	—	Digital circuit ground. The DGND terminals should be tied to the low-impedance circuit-board ground plane. External to the device, AGND should be tied to DGND and PLLGND.
DV_{DD}	14, 15, 29, 30	5, 6, 19, 20	Supply	—	Digital circuit power. DV_{DD} supplies power to the digital portion of the device. It is recommended that a combination of high-frequency decoupling capacitors be connected to DV_{DD} (i.e., paralleled 0.1 μF and 0.001 μF). Lower frequency 10-μF filtering capacitors can also be used. These supply terminals are separated from AV_{DD} internally in the device to provide noise isolation. These terminals should also be tied together to a power plane on the circuit board. Individual filtering networks for each is desired.
FILTER	66	54	CMOS	I/O	PLL filter. FILTER is connected to a 0.1-μF capacitor and then to PLLGND to complete the internal lag-lead filter. This filter is required for stable operation of the frequency multiplier PLL running off of the crystal oscillator.

Terminal Functions (Continued)

TERMINAL			TYPE	I/O	DESCRIPTION
NAME	NO.				
	HV	PM			
$\overline{\text{ISO}}$	7	62	CMOS	I	Link interface isolation input. $\overline{\text{ISO}}$ is normally tied high both to implement TI bus-holder isolation or no isolation. The TSB21LV03C does not support Annex J isolation.
LPS	11	2	CMOS	I	Link power status. LPS is connected to either the V_{DD} supplying the LLC through a 1–k Ω resistor or directly to a pulsed output that is active when the LLC is powered for the purpose of monitoring the LLC power status. The pulsed signal must be between 220 kHz and 5.5 MHz to be sensed as active. If LPS is inactive, the phy-LLC interface is disabled, and the TSB21LV03C performs only the basic repeater functions required for network initialization and operation. LPS is 5-V tolerant and has an internal bus-holder function built-in. If this terminal is tied through a resistor to a fixed state, the resistor must be 1 kΩ or less.
LREQ	12	3	CMOS	I	Link request. LREQ is an input from the LLC that requests the TSB21LV03C to perform some service. LREQ is 5-V tolerant and has an internal bus-holder function built-in. If this terminal is tied through a resistor to a fixed state, the resistor must be 1 kΩ or less.
PC2 – PC0	39, 40, 41	28, 29, 30	CMOS	I	Power class indicators. The PC signals set the bit values of the three power-class bits in the Self-ID packet (bits 21, 22, and 23). These bits can be programmed by tying the terminals to V_{DD} (high) or to GND (low).
PD	16	7	CMOS	I	Power down. When asserted high, PD turns off all internal circuitry except the CNA monitor circuits that drive the CNA terminal. PD is 5-V tolerant. The PD terminal may be tied directly to V_{DD} or to DGND. If this terminal is tied through a resistor to a fixed state, the resistor must be 1 kΩ or less. The PD terminal has an internal bus-holder function built in to it.
PLLGND	64, 65	52, 53	Supply	—	PLL circuit ground. The PLLGND terminals should be tied to the low-impedance circuit-board ground plane. External to the device, AGND should be tied to DGND and PLLGND.
$PLLV_{DD}$	2	58	Supply	—	PLL circuit power. $PLLV_{DD}$ supplies power to the PLL portion of the device. It is recommended that a combination of high-frequency decoupling capacitors be connected to $PLLV_{DD}$ (i.e., paralleled 0.1 µF and 0.001 µF). Lower frequency 10-µF filtering capacitors can also be used. The $PLLV_{DD}$ supply terminals are separated from AV_{DD} and DV_{DD} internally in the device to provide noise isolation. The $PLLV_{DD}$, AV_{DD}, and DV_{DD} terminals should also be tied together to a power plane on the circuit board. Individual filtering networks for each is recommended.
R0 R1	3 4	59 60	—	—	Current setting resistor. An internal reference voltage is applied to a resistor connected between R0 and R1 to set the operating current and the cable driver output current. A resistance of 6.3 kΩ ±0.5% should be used to meet the IEEE 1394-1995 standard requirements for output voltage limits.
$\overline{\text{RESET}}$	10	1	CMOS	I	Reset. When $\overline{\text{RESET}}$ is asserted low (active), a bus reset condition is set on the active cable ports and the the internal logic is reset to the reset start state. An internal pullup resistor, which is connected to V_{DD}, is provided so only an external delay capacitor is required. This input is a standard logic buffer and can also be driven by an open-drain logic output buffer. The minimum hold time for RESET is listed in the recommended operating characteristics table.
SYSCLK	19	9	CMOS	O	System clock. SYSCLK provides a 49.152-MHz clock signal, which is synchronized with the data transfers to the LLC.
TESTM1 TESTM2	32 31	22 21	CMOS	I	Test mode control. TESTM1 and TESTM2 are used during the manufacturing test and should be tied to V_{DD}.

Terminal Functions (Continued)

TERMINAL			TYPE	I/O	DESCRIPTION
NAME	NO.				
	HV	PM			
TPA1+ TPA2+ TPA3+	57 51 47	45 40 36	Cable	O	Portn, port cable pair A. TPAn is the port A connection to the twisted-pair cable. Board traces from these terminals should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPA1– TPA2– TPA3–	56 50 46	44 39 35			
TPB1+ TPB2+ TPB3+	55 49 45	43 38 34	Cable	O	Portn, port cable pair B. TPBn is the port B connection to the twisted-pair cable. Board traces from these terminals should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPB1– TPB2– TPB3–	54 48 44	42 37 33			
TPBIAS1 TPBIAS2 TPBIAS3	58 59 60	46 47 48	Cable	O	Portn, twisted-pair bias. TPBIASn provides the 1.86-V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers and for sending a valid cable connection signal to the remote nodes.
V_{DD}–5V	13	4	Supply	—	5-V V_{DD} supply. V_{DD}–5V should be connected to the LLC V_{DD} supply when a 5-V LLC is connected to the phy, and it should be connected to the phy DV_{DD} when a 3-V LLC is used.
XI XO	68 1	56 57	—	—	Crystal oscillator. XO and XI connect to a 24.576-MHz parallel resonant fundamental mode crystal. Although, when a 24.576-MHz crystal oscillator is used, it can be connected to XI with XO left unconnected. The optimum values for the external shunt capacitors are dependent on the specifications of the crystal used. See application note on crystal oscillator.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . –0.3 V to 4 V
Input voltage range, V_I . . . . . –0.5 V to V_{DD}+0.5 V
Output voltage range at any output, V_O . . . . . –0.5 V to V_{DD}+0.5V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A, TSB21LV03C . . . . . 0°C to 70°C
TSB21LV03CI . . . . . –40°C to 85°C
TSB21LV03CM . . . . . –55°C to 125°C
Junction temperature, T_J, PM package . . . . . 150°C
HV package . . . . . 165°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 220°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
PM	1866 mW	14.9 mW/°C	1194 mW	972 mW	—
HV	2943 mW	21.02 mW/°C	1997 mW	1681 mW	841 mW

‡ This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$) and uses a board-mounted 67°C/W for PM package and 47.57°C/W for HV package.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	Source power node		3	3.3	3.6	V
	Nonsource power node§		2.7	3	3.6	
High-level input voltage, V_{IH}	CMOS inputs	Commercial	$0.7 V_{DD}$			V
		Industrial, Military	$0.85 V_{DD}$			
Low-level input voltage, V_{IL}	CMOS inputs				$0.2 V_{DD}$	V
Differential input voltage, V_{ID}	Cable inputs, 100-Mbit operation		142		260	mV
	Cable inputs, 200-Mbit operation		132		260	
	Cable inputs, during arbitration		171		262	
Common-mode input voltage, V_{IC}	TPB cable inputs, 100-Mbit or speed signaling off, Source power node		1.165		2.515	V
	TPB cable inputs, 100-Mbit or speed signaling off, Nonsource power node§		1.165		2.015	
	TPB cable inputs, 200-Mbit speed signaling, Source power node		0.935		2.515	
	TPB cable inputs, 200-Mbit speed signaling, Nonsource power node§		0.935		2.015	
Receive input jitter	TPA, TPB cable inputs, 100-Mbit operation				*±1.08	ns
	TPA, TPB cable inputs, 200-Mbit operation				*±0.5	
Receive input slew	Between TPA and TPB cable inputs, 100-Mbit operation				*±0.8	ns
	Between TPA and TPB cable inputs, 200-Mbit operation				*±0.55	
Output current, I_{OL}/I_{OH}	Control, Data, CNA and C/LKON outputs, SYSCLK		–12		12	mA
Output current, I_O	TPBIAS outputs		–3		1.3	mA
Hold time, power-up reset ($\overline{RESET}$)			*2			ms

§ For a node that does not source power (see Section 4.2.2.2 in IEEE 1394–1995 Standard).
* These parameters are not production tested for the HV package.

electrical characteristics over recommended operating conditions (unless otherwise noted)

driver

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OD}	Differential output voltage	55-Ω load	172		265	mV
$V_{(OFF)}$	Off-state differential output voltage	Drivers disabled			20	mV
$I_{O(diff)}$	Differential current (TPA+, TPA–, TPB+, TPB–)	Driver enabled, Speed signaling off	–1.05†		1.05†	mA
$I_{(SP)}$	Common-mode speed signaling current (TPB+, TPB–)	200-Mbit speed signaling enabled	–2.53‡		–4.84‡	mA

† Limits are defined as the algebraic sum of TPA+ and TPA– driver currents. Limits also apply to TPB+ and TPB– as the algebraic sum of driver currents.
‡ Limits are defined as the absolute limit of each of TPB+ and TPB– driver currents.

electrical characteristics over recommended operating conditions (unless otherwise noted) (continued)

receiver

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IT}	Input threshold voltage		–30		30	mV
V_{IT}	Cable bias-detect input threshold voltage, TPBn cable inputs	Driver disabled	0.6		1	V
I_{IC}	Common-mode input current	Driver disabled	–40		40	µA
Z_{ID}	Differential input impedance	Driver disabled	15			kΩ
					*6	pF
Z_{IC}	Common-mode impedance	Driver disabled	20			kΩ
					*24	pF

* These parameters are not production tested for the HV package.

device

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Supply current		V_{DD} = 3.3 V	Node transmitting or repeating		114		mA
				Node receiving		140		mA
			V_{DD} = 3.6 V				*175	mA
			V_{DD} = 3.6 V,	Power-down mode		20		
V_{IT}	Power status input threshold voltage (CPS)		R_L = 400 kΩ		4.7		7.5	V
V_{OH}	High-level output voltage		V_{DD} = min,	I_{OH} max	V_{DD}– 0.55			V
V_{OL}	Low-level output voltage		V_{DD} = max,	I_{OL} min			0.5	V
I_I	Input current (TESTM1, TESTM2, PC0, PC1, PC2)		$V_I = V_{DD}$ or 0				±1	µA
I_{off}	Off-state output current (CTL0, CTL1, D0, D1, D2, D3, C/LKON)		$V_O = V_{DD}$ or 0				±5	µA
	Pullup current (RESET)		V_I = 0 or 1.5 V	Commercial	–90	–45	–10	µA
				Industrial, Military	–110	–45	–10	
V_{TH+}	Positive arbitration comparator-input threshold voltage				89		168	mV
V_{TH-}	Negative arbitration comparator-input threshold voltage				–168		–89	mV
V_{IT}	Speed-signal input threshold voltage		TPBIAS –TPA common-mode voltage		49		131	mV
V_O	Output voltage (TPBIAS1, TPBIAS2, TPBIAS3)		At rated I_O current		1.665		2.015	V
	Bus holding current (LPS, LREQ, CTLn, Dn, PD)		$V_I = 1/2\,(V_{DD})$			725		µA

* These parameters are not production tested for the HV package.

thermal characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	PM package	EIA/JESD51-3, No air flow		67		°C/W
		HV package			47.57		
$R_{\theta JC}$	Junction-to-case thermal resistance	PM package			10.4		°C/W
		HV package			3		

switching characteristics

PARAMETER		MEASURED	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Jitter, transmit	TPA, TPB				±0.25	ns
	Skew rate, transmit	Between TPA and TPB				*±0.15	ns
t_r	Rise time, transmit	10% to 90%	R_L = 55 Ω, C_L = 10 pF			*2.2	ns
t_f	Fall time, transmit	90% to 10%	R_L = 55 Ω, C_L = 10 pF			*2.2	ns
t_{su}	Setup time, Dn, CTLn, LREQ↑↓ to SYSCLK↑	50% to 50%	See Figure 1	*5			ns
t_h	Hold time, Dn, CTLn, LREQ↑↓ before SYSCLK↑	50% to 50%	See Figure 1	*2			ns
t_d	Delay time, SYSCLK↑ to Dn, CTLn↑↓	50% to 50%	See Figure 2	2		11	ns

* These parameters are not production tested for the HV package.

PARAMETER MEASUREMENT INFORMATION

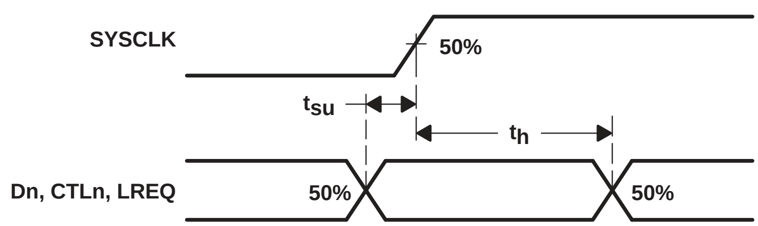


Figure 1. Dn, CTLn, LREQ Input Setup and Hold Timing Waveforms

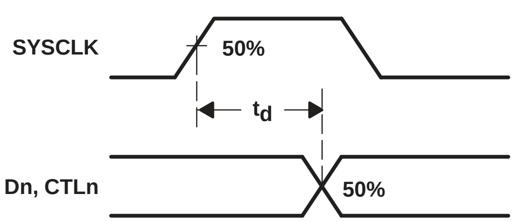


Figure 2. Dn and CTLn Output-Delay Timing Waveforms

APPLICATION INFORMATION

internal register configuration

The accessible internal registers of this device are listed in Table 1.

Table 1. Internal Register Configuration

Address	0	1	2	3	4	5	6	7
0000	Physical ID						R	CPS
0001	RHB	IBR	GC					
0010	SPD		Rev		NP			
0011	AStat1		BStat1		Ch1	Con1	Reserved	
0100	AStat2		BStat2		Ch2	Con2	Reserved	
0101	AStat3		BStat3		Ch3	Con3	Reserved	
0110	LoopInt	CPSInt	CPS	IR	Reserved			C
0111	Reserved							
1000	Reserved							

Table 2. Internal Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
AStat(n)	2	Read only	AStat contains the line state of TPAn. The status is indicated by the following: 11 = high-impedance state 01 = 1 10 = 0 00 = Invalid data state. Power-up reset initializes to this line state. This line state is also output during transmit and receive operations, including date-end signaling. The line state outputs are generally valid during arbitration and idle conditions on the bus.
BStat(n)	2	Read only	BStat contains the line state of TPBn. The status is indicated by the following: 11 = high-impedance state 01 = 1 10 = 0 00 = Invalid data state. Power-up reset initializes to this line state. This line state is also output during transmit and receive operations. The line state outputs are generally valid during arbitration and idle conditions on the bus.
C	1	R	Bus manager capable. C indicates the state of the Bus Manager Capable input. When set, this bit is used by the TSB21LV03C to specify in the Self-ID packet that the node is Bus Manager Capable.
Ch(n)	1	Read only	When Ch = 1, the port is a child, otherwise it is a parent. This bit is invalid after a hardware reset or a bus reset until tree-ID processing is completed.
Con(n)	1	Read only	Con indicates the connection status of the port. When Con = 1, the port is connected, otherwise it is disconnected. This bit is set to 1 by a hardware reset and is updated to reflect the actual cable connection status of the port during bus reset. The TSB21LV03C contains connection debounce circuitry that prevents a new cable connection on a port from initiating a bus reset until the connection status has been stable for at least 335 ms. A cable disconnect initiates a bus reset immediately. After a hardware reset, the TSB21LV03C sets the connection status of all ports to 0. The TSB21LV03C proceeds with the bus reset, tree-ID, and Self-ID, but with all ports considered to be disconnected child ports. The TSB21LV03C can not transmit any signals on the serial bus ports during this time. The TSB21LV03C does report itself as root with a physical address of 00h at the completion of Self-ID. If any port is actually connected, after the debounce delay, the TSB21LV03C initiates another bus reset, which proceeds normally with interaction between the TSB21LV03C and its peer nodes.

APPLICATION INFORMATION

Table 2. Internal Register Field Descriptions (continued)

FIELD	SIZE	TYPE	DESCRIPTION
CPS	1	Read only	Cable power status (CPS) contains the status of the CPS input terminal. When cable power voltage has dropped too low for reliable operation, CPS is reset (0). CPS is included twice in the internal registers to expedite handling of the CPSInt.
CPSInt	1	Read/ Write	CPSint indicates that a cable power status interrupt has occurred. This interrupt occurs whenever the CPS input goes low. The interrupt indicates that the cable power voltage has dropped too low to ensure reliable operation. This bit is cleared (0) by a hardware reset or by writing a 0 to this register. However, if the CPS input is still low, another cable-power status interrupt immediately occurs.
GC	6	Read/ Write	The gap count (GC) register sets the fair and arb-reset gap times. The gap count may be set to a particular value to optimize bus performance. Typically, the gap count should be set to 2 times the maximum number of hops on the bus and **must** be set to the same value for all nodes on the bus. The gap count can be set by either a write to this register or by reception or transmission of a PHY_CONFIG packet. The gap count is reset to 3Fh after a hardware reset or after two consecutive bus resets without an intervening write to the gap count register (either a write to the gap count register by the LLC or a PHY_CONFIG packet).
IBR	1	Read/ Write	When set, initiate bus reset (IBR) causes the current node to immediately initiate a bus reset. IBR is cleared (0) after a hardware reset or a bus reset.
IR	1	Read/ Write	IR indicates that the last bus reset was initiated in this TSB21LV03C phy. This bit is also included in the self-ID packet.
LoopInt	1	Read/ Write	LoopInt indicates that a configuration loop timeout has occurred. This interrupt occurs when the arbitration controller waits for too long a period of time during tree-ID. This interrupt can indicate that the bus is configured in a loop. This bit is cleared (0) by a hardware reset or by writing a 0 to this register bit.
NP	4	Read only	NP contains the number of ports implemented in the core logic (not the number of ports actually on the device). For the TSB21LV03C, NP is set to 0011b.
Physical ID	6	Read only	Physical ID contains the physical address of the local node. The physical ID in valid after a hardware reset or a bus reset until the Self-ID process has been completed. A complete Self-ID is indicated by an unsolicited status transfer of the register 0 contents to the LLC.
R	1	Read only	R indicates whether the current node is the root node or not. This bit is cleared (0) on a hardware reset or a bus reset. This bit is set during tree-ID when the current node is root.
Rev	2	Read only	The revision (Rev) bits indicate the design revision of the core logic. For the TSB21LV03C, Rev is set to 00.
RHB	1	Read/ Write	When set, the root hold-off bit (RHB) instructs the local node to try to become the root node during the next bus reset. RHB is reset (0) during a hardware reset and is not affected by a bus reset.
SPD	2	Read only	The speed (SPD) bits indicates the top signaling speed of the local port and for the TSB21LV03C is set to 01b.

APPLICATION INFORMATION

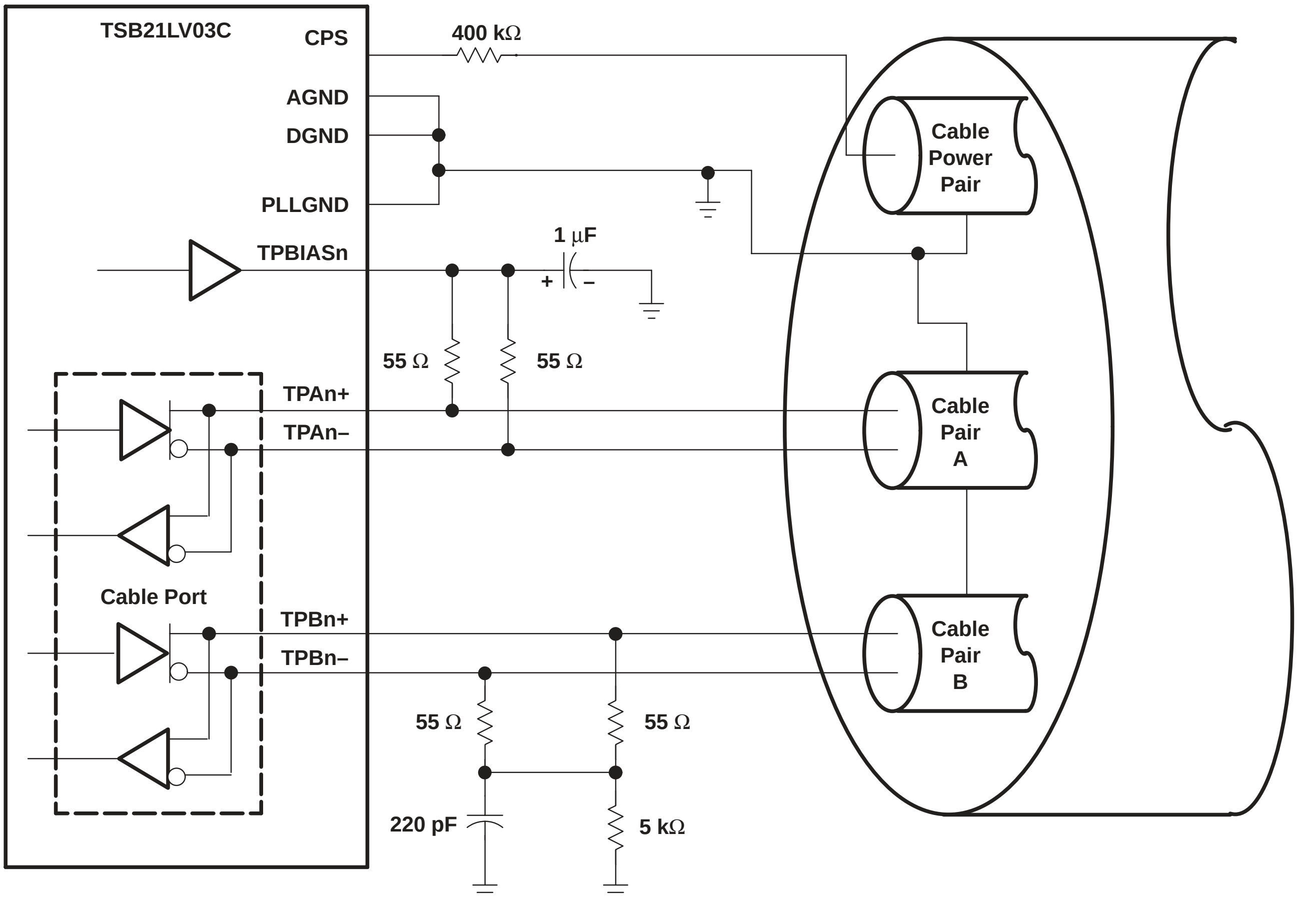


Figure 3. Twisted-Pair Cable Interface Connections

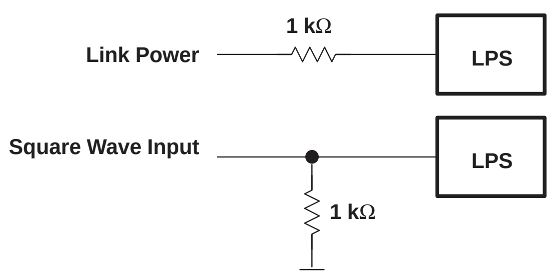


Figure 4. Nonisolated Connection Variations for LPS

APPLICATION INFORMATION

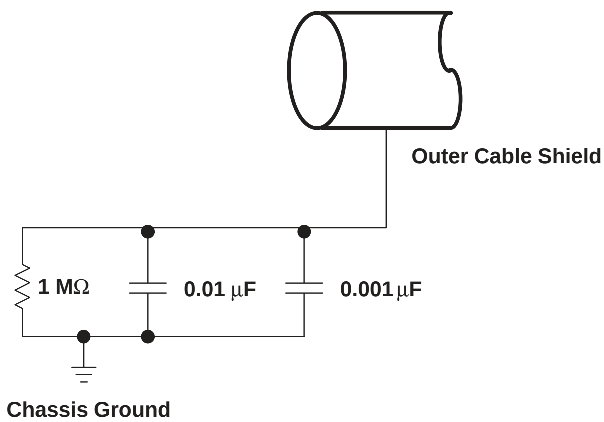


Figure 5. Compliant DC Isolated Outer Shield Termination

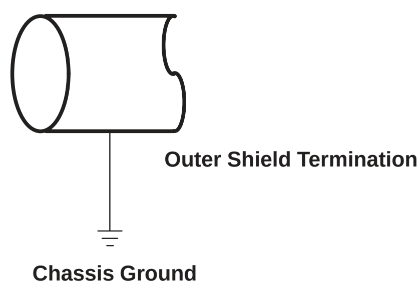
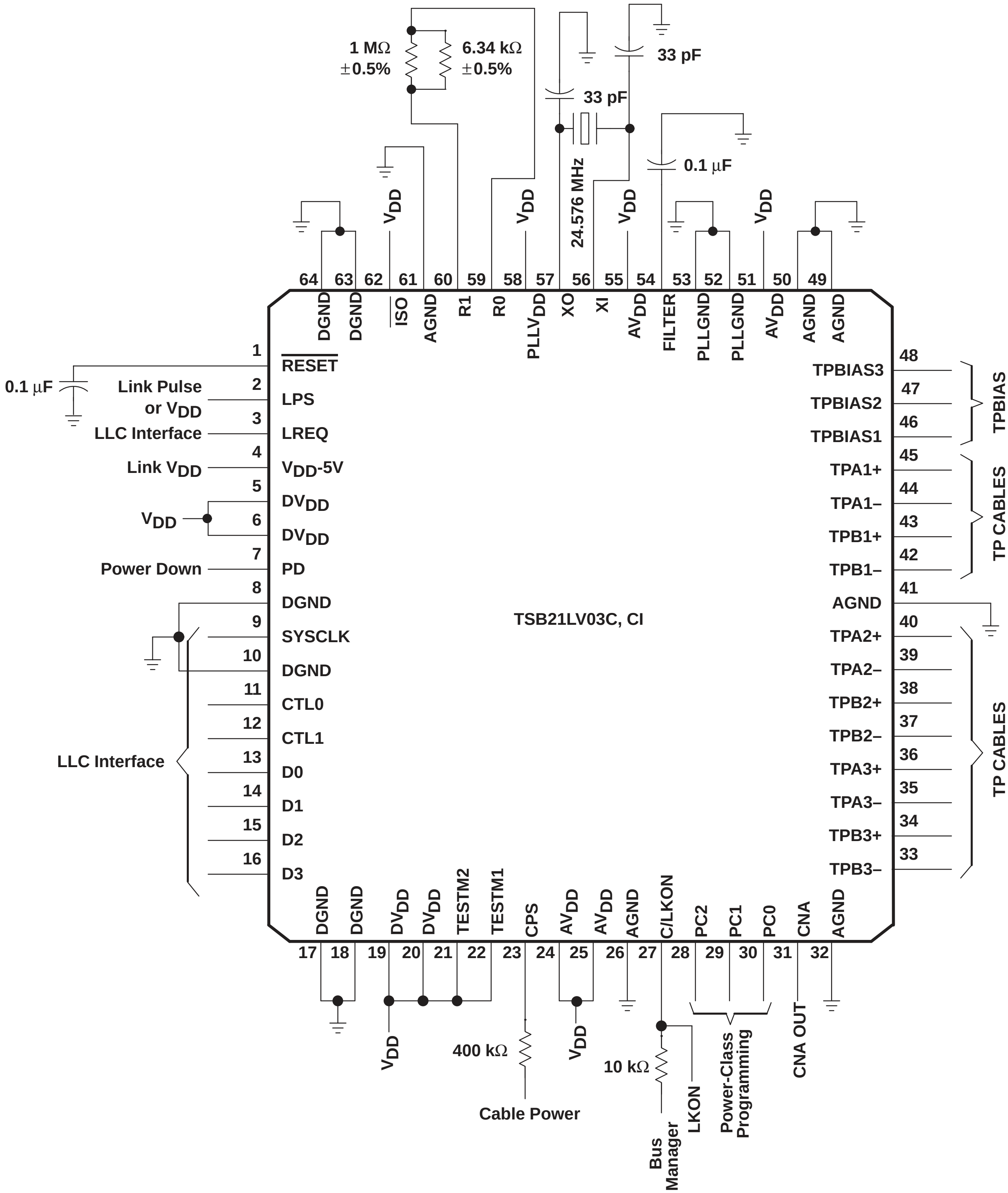


Figure 6. Nonisolated Outer Shield Termination

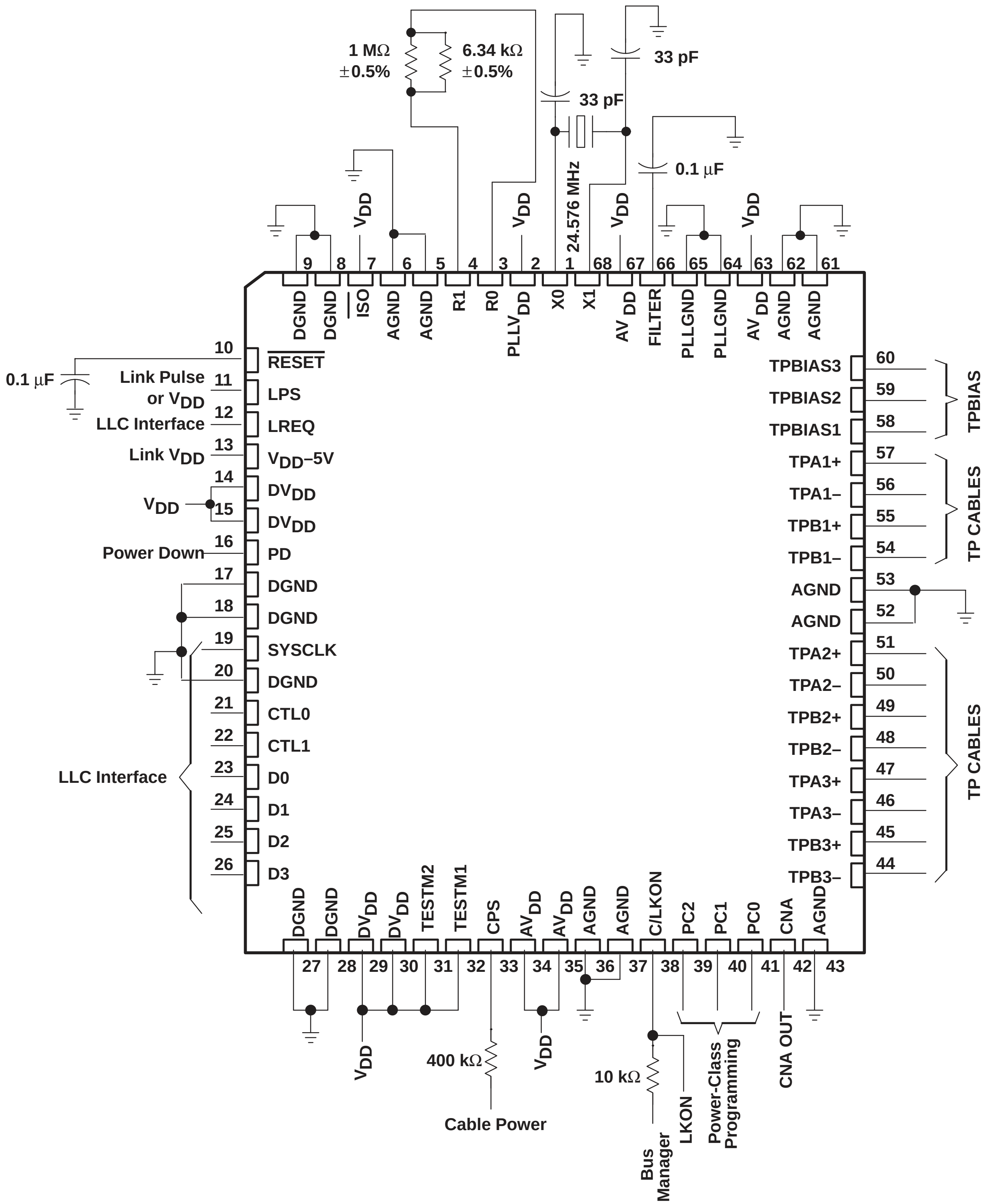
APPLICATION INFORMATION (PM PACKAGE)



NOTE A: For more information see the application note.

Figure 7. External Component Connections

APPLICATION INFORMATION (HV PACKAGE)



NOTE A: For more information see the application note.

Figure 8. External Component Connections

APPLICATION INFORMATION

crystal selection

TI PHYs may use an external 24.576 MHz crystal connected between the XI and XO pins on the PHY to provide the PHY clock. The following are some typical specifications for the crystals used with the Physical Layers from TI. The clock resulting from the input from the crystal must be within the tolerance of ±100 parts per million for the PHYs to function correctly. This is required by the 1394 standard. This frequency tolerance for the PHY clocks on each node must be maintained over the variation introduced over production runs of boards and environment the machines operate in. Every board must have an SYSCLK (clock generated by the PHY) within ±100 ppm of 49.152 MHz to be compliant to the 1394 standard. If adjacent nodes are more than 200 ppm away from one another then long packets sent across the 1394 bus may be corrupted, with the final bits of the packet being lost. TI PHYs are designed with a maximum of margin, but the limits imposed by 1394 must still be adhered to.

1. Crystal Mode of operation:
   Fundamental
2. Frequency Tolerance at 25°C:
   Total variation specification for the complete circuit is 100ppm. The crystal is specified at less than 100 ppm.
3. Frequency stability (over temperature):
   Total variation specification for the complete circuit is 100 ppm. The crystal is specified at less than 100 ppm.

NOTE:
The total variation must be kept below 100 ppm with some allowance for variation introduced by variations in board builds and device tolerances. So the sum of the frequency tolerance and the frequency stability must be less than 100 ppm. This can be traded off between the two, for example the frequency tolerance may be specified at 50 ppm and the temperature may be specified at 30 ppm to give a total of 80 ppm possible variation just due to the crystal.

4. Load capacitance: [Parallel (pF)]
   Parallel mode crystal circuits should be used for optimum precision. Load capacitance will be a function of your board layout and circuit. The total load capacitance (C_L) will affect the frequency of oscillation. Consult with the crystal vendor on design to get an SYSCLK supplied by the PHY to less than 100 ppm from 49.152 MHz . A tolerance of ±5% is recommend for load capacitors. For TI's TSBKOHCI403 Designer Kit with a crystal specified for 20-pF loading, a value of 33 pF for each load capacitor (C9 = C10 below) is appropriate with the layout used for the board. The load specified for the crystal includes the load capacitors (C9, C10), the loading of the PHY pins (C_{PHY}), and the loading of the board itself (C_{BD}). To summarize: $C_L = [(C9 \times C10) / (C9+C10)] + C_{PHY} + C_{BD}$. Representative values for C_{PHY} are ~1 pF and for C_{BD} are about 0.8 pF per centimeter of board etch, a typical board can have from 3 pF to 6 pF or more. The capacitance of load capacitors C9 and C10 combine as capacitors in series.

APPLICATION INFORMATION

crystal selection (continued)

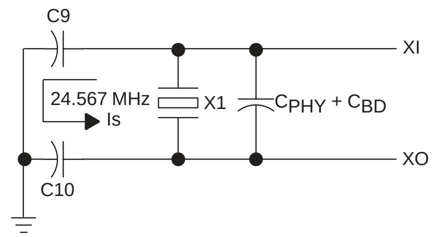


Figure 9. Load Capacitance for the TSB21LV03C PHY

NOTE:

The layout of the crystal portion of the PHY circuit is important for getting the correct frequency from the crystal, minimizing the noise introduced into the PHY Phase Lock Loop, and minimizing any emissions from the circuit. The crystal and the two load capacitors should be considered a unit during layout. The crystal and the load capacitors should be placed as close as possible to one another while minimizing the loop area created by the combination of the three components. Varying the size of the capacitors may help in this. Minimizing the loop area minimizes the effect of the resonant current (Is) that flows in this resonant circuit. This layout unit (crystal and load capacitors) should then be placed as close as possible to the PHY XI and XO pins to minimize etch lengths.

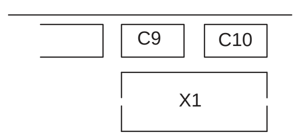


Figure 10. Recommended Crystal and Capacitor Layout for the TSB21LV03C PHY

Part of the verification process for the design should be to measuring the frequency of the SYSCLK output of the PHY. This should be done with a frequency counter with an accuracy of 6 digits or better. If the SYSCLK is more than the crystal tolerance away from 49.152 MHz, the load capacitance of the crystal may be varied to reduce total variation to below 100 ppm. Changes should be done to both load capacitors (C9 and C10 above) at the same time to the same value. Consult crystal vender for detailed understanding of requirements. In order for a 1394 bus to operate correctly each SYSCLK on each node on the bus must be within 200 ppm of the adjacent SYSCLK on the bus. The 1394 standard requires this by specifying a center frequency of 49.152 MHz and a ±100 ppm tolerance around 49.152 MHz.

PRINCIPLES OF OPERATION

The TSB21LV03C is designed to operate with a LLC such as the TI TSB12LV22, TSB12LV41, TSB12LV01, TSB12LV21, TSB12LV31, and TSB12C01. Details of how the LLC devices operate are described in the LLC data sheets. The following paragraphs describe the operation of the phy-LLC interface.

The TSB21LV03C supports 100-/200-Mbit/s data transfer and has four bidirectional data lines, D0 – D3, crossing the interface. In 100-Mbit/s operation only D0 and D1 terminals are used. In 200 Mbit/s operation, all Dn terminals are used for data transfer. The unused Dn terminals are driven low. In addition, there are two bidirectional control lines CTL0 and CTL1, the 49.152-MHz SYSCLK line from the phy to the LLC, and the LLC request terminal LREQ from the LLC to the phy. The TSB21LV03C has control of all bidirectional terminals. The LLC is allowed to drive these terminals only after it has been given permission by the phy. The dedicated LREQ request terminal is used by the LLC for any activity that it wishes to initiate.

There are four operations that may occur in the phy-LLC interface: request, status, transmit, and receive. With the exception of the request operation, all actions are initiated by the phy.

When the phy has control of the bus the CTL0 and CTL1 lines are encoded as shown in Table 3.

Table 3. CTLn Status When Phy Has Control of the Bus

CTL0	CTL1	STATUS NAME	DESCRIPTION
0	0	Idle	No activity is occurring (this is the default mode).
0	1	Status	Status information is being sent from the phy to the LLC.
1	0	Receive	An incoming packet is being sent from the phy to the LLC.
1	1	Transmit	The LLC has been given control of the bus to send an outgoing packet.

When the LLC has control of the bus (phy permission) the CTL0 and CTL1 terminals are encoded as shown in Table 4.

Table 4. CTLn Status When LLC Has Control of the Bus

CTL0	CTL1	STATUS NAME	DESCRIPTION
0	0	Idle	The LLC releases the bus (transmission has been completed).
0	1	Hold	The LLC is holding the bus while data is being prepared for transmission or is sending another packet without arbitrating.
1	0	Transmit	An outgoing packet is being sent from the LLC to the phy.
1	1	Reserved	None

request

When the LLC requests the bus or accesses a register that is located in the TSB21LV03C, a serial stream of information is sent across the LREQ line. The length of the stream varies depending on whether the transfer is a bus request, a read command, or a write command. Regardless of the type of transfer, a start bit of 1 is required at the beginning of the stream, and a stop bit of 0 is required at the end of the stream. Bit 0 is the most significant bit, and is transmitted first. The LREQ terminal is required to idle low (logic level 0).

PRINCIPLES OF OPERATION

Table 5. LLC Bus-Request or Register-Access-Request Bit Length

REQUEST TYPE	NUMBER OF BITS
Bus request	7
Read register request	9
Write register request	17

For a Bus Request the length of the LREQ data stream is 7 bits as shown in Table 6.

Table 6. LLC Bus Request

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1).
1–3	Request Type	Indicates the type of bus request (see Table 9 for the encoding of this field).
4–5	Request Speed	Should be 00 for TSB21LV03C 100-Mbit/s speed and 01 for 200-Mbit/s speed.
6	Stop Bit	Indicates the end of the transfer (always 0).

For a Read Register Request the length of the LREQ data stream is 9 bits as shown in Table 7.

Table 7. LLC Read Register Access

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1).
1–3	Request Type	Always a 100 indicating that this is a read register request.
4–7	Address	Identifies the address of the phy register to be read.
8	Stop Bit	Indicates the end of the transfer (always 0).

For a Write Register Request the Length of the LREQ data stream is 17 bits as shown in Table 8.

Table 8. LLC Write Register Access

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1).
1–3	Request Type	Always a 101 indicating that this is a write register request.
4–7	Address	Identifies the address of the phy register to be written to.
8–15	Data	Gives the data that is to be written to the specified register address.
16	Stop Bit	Indicates the end of the transfer (always 0).

The 3-bit Request Type field has the values shown in Table 9.

Table 9. LLC Bus Request Type

LREQ1	LREQ2	LREQ3	NAME	DESCRIPTION
0	0	0	ImmReq	Immediate request. Upon detection of an idle, the LLC takes control of the bus immediately (no arbitration).
0	0	1	IsoReq	Isochronous request: the LLC arbitrates for the bus, no gaps.
0	1	0	PriReq	Priority request: the LLC arbitrates after a subaction gap, ignores fair protocol.
0	1	1	FairReq	Fair request: the LLC arbitrates after a subaction gap, follows fair protocol.
1	0	0	RdReg	The LLC returns the specified register contents through a status transfer.
1	0	1	WrReg	The LLC writes to the specified register.
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

PRINCIPLES OF OPERATION

LREQ timing (each cell represents one clock sample time):

NOTE B: Each cell represents one clock sample time.

Figure 11. LREQ Timing

For fair or priority access, the LLC requests control of the bus at least one clock after the phy-LLC interface becomes idle. If the LLC senses that the CTLn terminals are in a receive state (CTL0 = 1, CTL1 = 0), this indicates that its request has been lost. This is true anytime during or after the LLC sends the bus request transfer. Additionally, the phy ignores any fair or priority requests if it asserts the receive state while the LLC is requesting the bus. The LLC then reissues the request one clock after the next interface idle.

The cycle master uses a normal priority request to send a cycle-start message. After receiving a cycle-start message, the LLC can issue an isochronous bus request. When arbitration is won, the LLC proceeds with the isochronous transfer of data. The isochronous request register is cleared in the phy once the LLC sends another type of request or when the isochronous transfer has been completed. The isochronous request must be issued during a packet reception. Generally this request would be during reception of a cycle-start packet.

The ImmReq request is issued when the LLC needs to send an acknowledgment after reception of a packet addressed to it. This request must be issued during packet reception. This is done to minimize the delays that a phy would have to wait between the end of a packet and the transmittal of an acknowledgment. As soon as the packet ends, the phy immediately grants access of the bus to the LLC. The LLC sends an acknowledgment to the sender unless the header CRC of the packet turns out to be bad. In this case, the LLC releases the bus immediately; it is not allowed to send another type of packet on this grant. To guarantee this, the LLC is forced to wait 160 ns after the end of the packet is received. The phy then gains control of the bus and the acknowledgement with the CRC error is sent. Then the bus is released and allowed to proceed with another requests.

Although highly improbable, it is conceivable that two separate nodes can believe that an incoming packet is intended for them. The nodes then issue a ImmReq request before checking the CRC of the packet. Since both phys seize control of the bus at the same time, a temporary, localized collision of the bus occurs somewhere between the competing nodes. This collision would be interpreted by the other nodes on the network as being a high-impedance line state, not a bus reset. As soon as the two nodes check the CRC, the mistaken node drops its request and the false line state is removed. The only side effect would be the loss of the intended acknowledgment packet (this is handled by the higher-layer protocol).

read/write requests

When the LLC requests to read the specified register contents, the phy sends the contents of the register to the LLC through a status transfer. When an incoming packet is received while the phy is transferring status information to the LLC, the phy continues to attempt to transfer the contents of the register until it is successful.

For write requests, the phy loads the data field into the appropriately addressed register as soon as the transfer has been completed. The LLC is allowed to request read or write operations at any time.

PRINCIPLES OF OPERATION

status

A status transfer is initiated by the phy when it has status information to transfer to the LLC. The phy waits until the interface is idle before starting the transfer. The transfer is initiated by asserting the following on the control terminals: CTL0 – CTL1 = 01 along with the first two bits of status information on the D0 – D3 terminals. The phy maintains CTL0 – CTL1 = 01 for the duration of status transfer. The phy may prematurely end a status transfer by asserting something else other than CTL0 – CTL1 = 01 on the control terminals. This could be caused by an incoming packet from another node. The phy continues to attempt to complete the transfer until the information has been successfully transmitted. There must be at least one idle cycle in between consecutive status transfers.

The phy normally sends just the first 4 bits of status to the LLC. These bits are status flags that are needed by the LLC state machines. The phy sends an entire status packet to the LLC after a request transfer that contains a read request, or when the phy has pertinent information to send to the LLC or transaction layers. The only defined condition where the phy automatically sends a register to the LLC is after self-ID, when it sends the physical-ID register, which contains the new node address. After a power-on reset, the TSB21LV03C sends two self-ID status transfers. The first transfer is invalid (a status of not connected); later, during the same bus reset, a second, correct root, node number, and connection status self-ID is transferred. During all other bus resets, only one Self-ID status is transmitted.

The definition of the bits in the status transfer are shown in Table 10 and the timing is shown in Figure 7.

Table 10. 16-Bit Stream Status Request

BIT(S)	NAME	DESCRIPTION
0	Arbitration Reset Gap	Bit 0 indicates that the phy has detected that the bus has been idle for an arbitration reset gap time (this time is defined in the IEEE 1394–1995 standard). Bit 0 is used by the LLC in its busy/retry state machine.
1	Subaction Gap	Bit 1 indicates that the phy has detected that the bus has been idle for a subaction gap time (this time is defined in the IEEE 1394–1995 standard). Bit 1 is used by the LLC to detect the completion of an isochronous cycle.
2	Bus Reset	Bit 2 indicates that the phy has entered the bus reset state.
3	State Timeout or CPS	Bit 3 indicates that the phy stayed in a particular state for too long a period, which is usually the effect of a loop in the cable topology, or that the cable power has dropped below the threshold for reliable operation.
4–7	Address	Bits 4 – 7 hold the address of the phy register whose contents are transferred to the LLC.
8–15	Data	Bits 8 – 15 contain the data that is to be sent to the LLC.

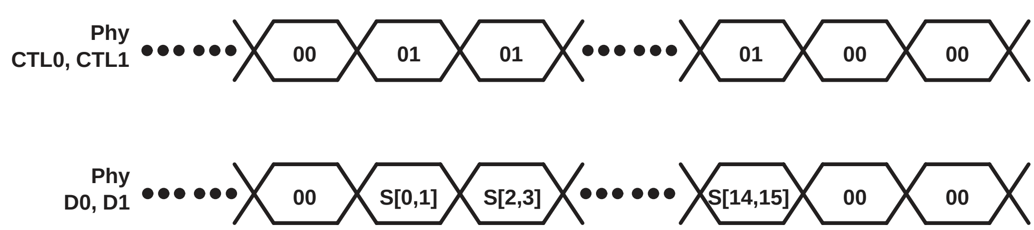


Figure 12. Status Transfer Timing

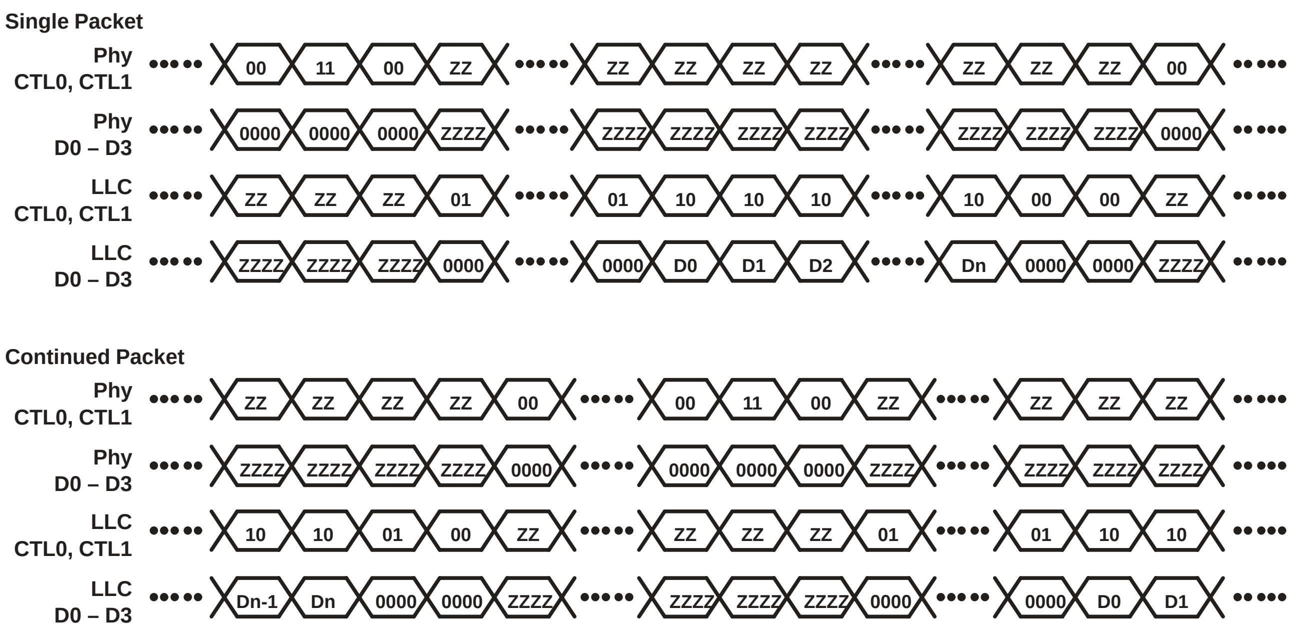
PRINCIPLES OF OPERATION

transmit

When the LLC wants to transmit information, it first requests access to the bus through the LREQ terminal. Once the phy receives this request, it arbitrates to gain control of the bus. When the phy wins ownership of the serial bus, it grants the bus to the LLC by asserting the transmit state on the CTLn terminals for at least one SYSCLK cycle, followed by idle for one clock cycle. The LLC takes control of the bus by asserting either hold or transmit on the CTLn terminals. Hold is used by the LLC to keep control of the bus when it needs some time to prepare the data for transmission. The phy keeps control of the bus for the LLC by asserting a data-on state on the bus. It is not necessary for the LLC to use hold when it is ready to transmit as soon as bus ownership is granted.

When the LLC is prepared to send data, it asserts the transmit state on the CTLn terminals as well as sending the first bits of the packet on the D0 – D3 lines (assuming 200 Mbits/s). The transmit state is held on the CTLn terminals until the last bits of data have been sent. The LLC then asserts an idle state on the CTLn terminals for one clock cycle after which it releases control of the interface.

However, there are times when the LLC needs to send another packet without releasing the bus. For example, the LLC may want to send consecutive isochronous packets or it may want to attach a response to an acknowledgment. To do this, the LLC asserts a hold state instead of an idle state when the first packet of data has been completely transmitted. In this case, hold informs the phy that the LLC needs to send another packet without releasing control of the bus. The phy then waits a set amount of time before asserting a transmit state. The LLC can then proceed with the transmittal of the second packet. After all data has been transmitted and the LLC has asserted an idle state on the CTLn terminals, the phy asserts its own idle state on the CTLn terminals. When sending multiple packets in this fashion, it is required that all data be transmitted at the same speed. This is required because the transmission speed is set during arbitration and since the arbitration step is skipped, there is no way of informing the network of a change in speed.



NOTE A: ZZ = High-impedance state
D0 => Dn = Packet data

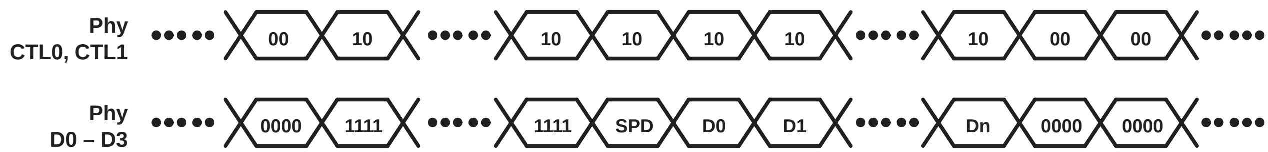
Figure 13. Transmit Timing Waveforms

PRINCIPLES OF OPERATION

receive

When data is received by the phy from the serial bus, the phy transfers the data to the LLC for further processing. The phy asserts a receive state on the CTLn terminals and asserts a 1 on each Dn terminal. The phy indicates the start of the packet by placing the speed code on the data bus. The phy then proceeds with the transmittal of the packet to the LLC on the Dn terminals while still keeping the receive status on the CTLn terminals. Once the packet has been completely transferred, the phy asserts an idle state on the CTLn terminals, which completes the receive operation.

NOTE:
The speed is a phy-LLC protocol and not included in the CRC.



NOTE A: SPD = Speed Code
D0 => Dn = Packet data

Figure 14. Receive Timing Waveforms

Table 11. Speed Code for the Receiver

D0 – D3	Data Rate
00YY†	100 Mbit/s
0100	200 Mbit/s

† Y = Transmitted as 0, ignored on receive.

power class bits in self-ID packet

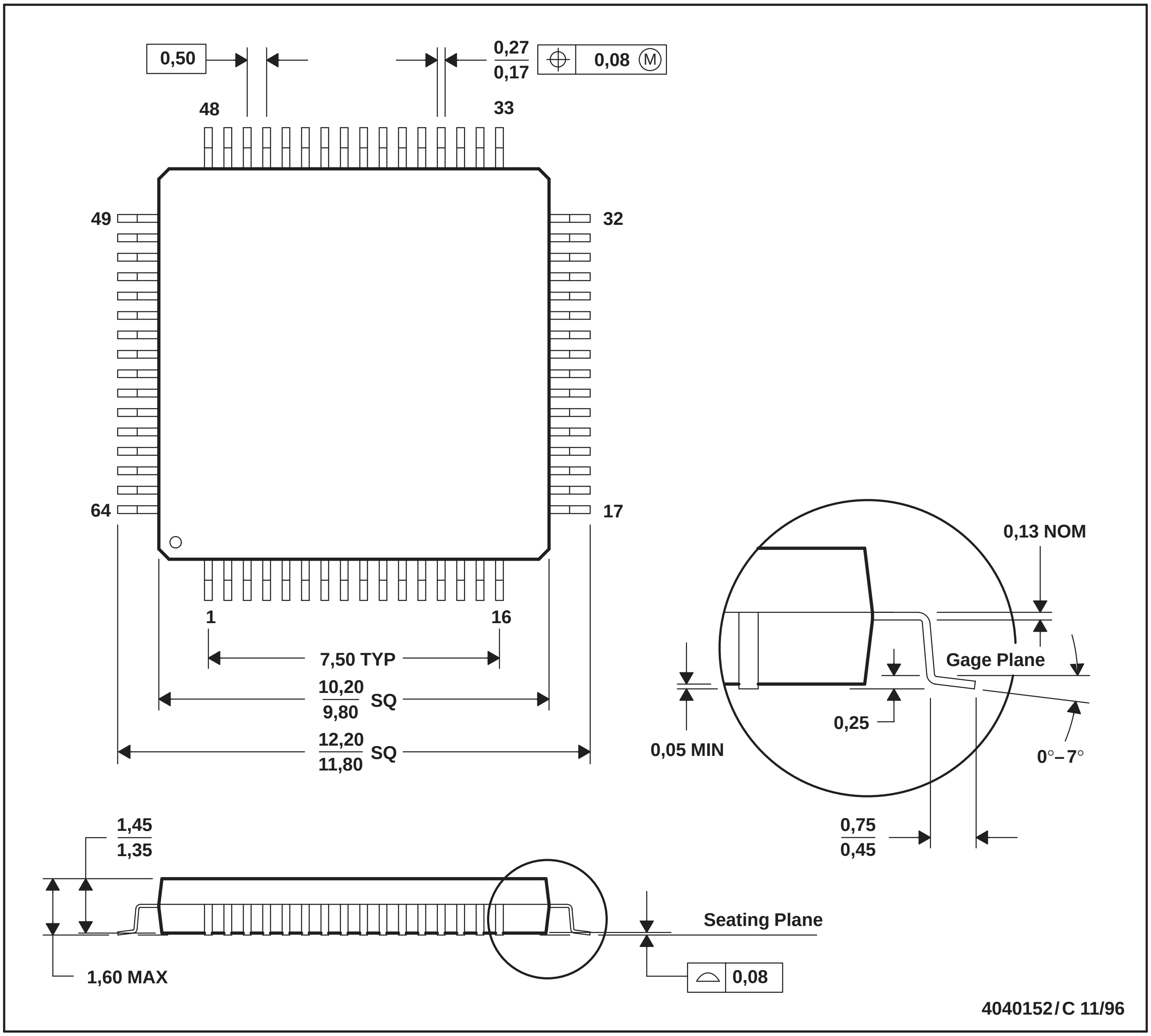
Table 12 describes the meaning of the power-class bits in the pwr field of the Self-ID packet. Bit 21 is transmitted first, followed by bit 22 and then bit 23. This power-field bit description complies with the IEEE 1394-1995 standard.

Table 12. Self-ID Packet Pwr-Field Bit Description

PC0–PC2	DESCRIPTION
000	Node does not need power and does not repeat power.
001	Node is self powered, and provides a minimum of 15 W to the bus.
010	Node is self powered, and provides a minimum of 30 W to the bus.
011	Node is self powered, and provides a minimum of 45 W to the bus.
100	Node may be powered from the bus, and is using up to 1 W.
101	Node may be powered from the bus, and is using up to 1 W. An additional 2 W is needed to enable the LLC and higher layers.
110	Node may be powered from the bus, and is using up to 1 W. An additional 5 W is needed to enable the LLC and higher layers.
111	Node may be powered from the bus, and is using up to 1 W. An additional 9 W is needed to enable the LLC and higher layers.

MECHANICAL INFORMATION

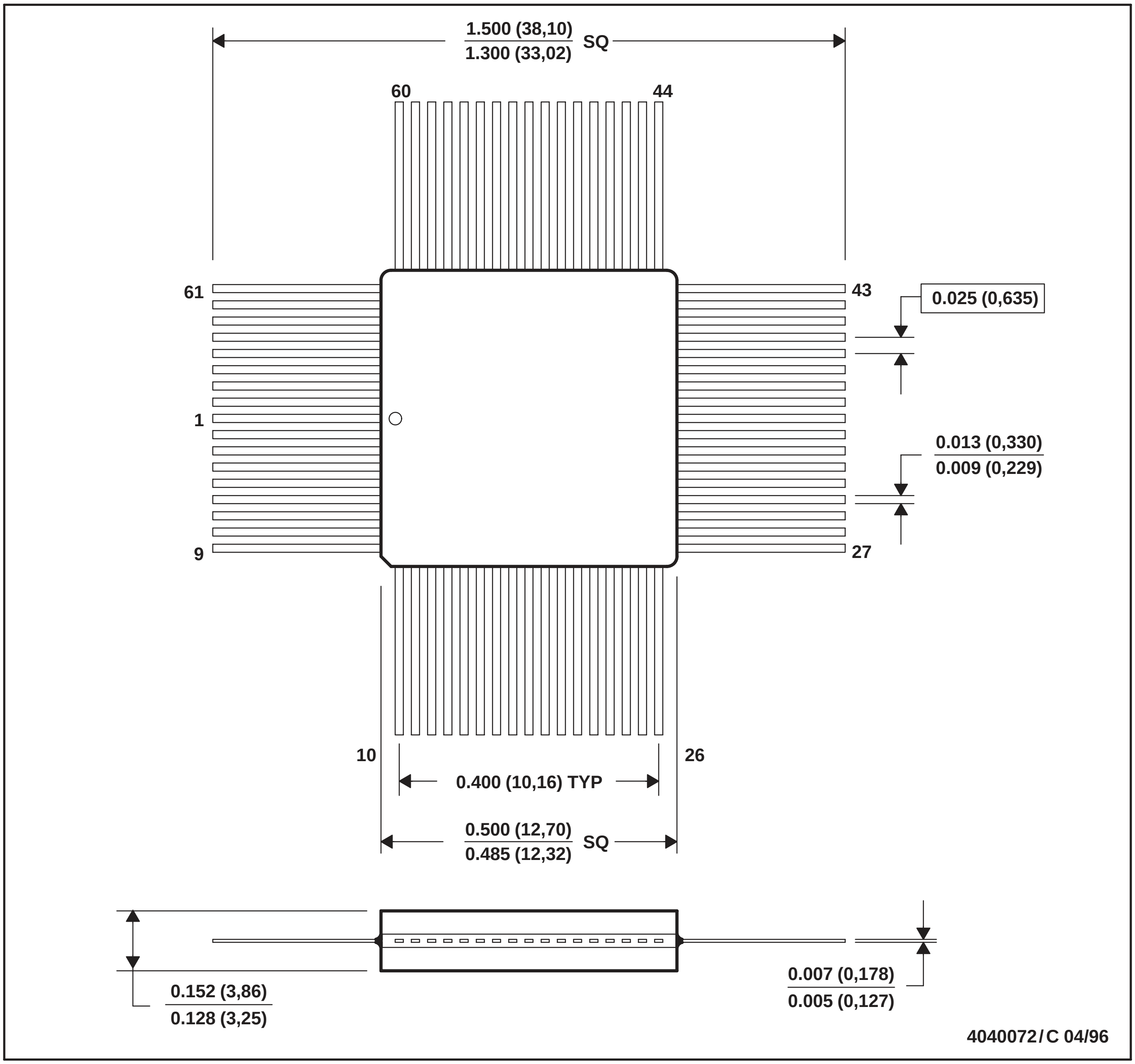
PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

MECHANICAL INFORMATION

HV (S-GQFP-F68) **CERAMIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.

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TSB21LV03C, IEEE 1394-1995, 3.3V, 3-Port, 100/200Mbps Physical Layer Controller

Device Status: Active

> Description
> Features
> Datasheets
> Pricing/Samples/Availability
> Application Notes
> Related Documents
> Applications

Parameter Name	TSB21LV03C
Supply Voltage(s) (V)	3.3
Speed (max) (Mbps)	200
Ports	3

Description

The TSB21LV03C provides the analog and digital physical layer functions needed to implement a three-port node in a cable-based IEEE 1394-1995 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The TSB21LV03C is designed to interface with a link-layer controller (LLC), such as the TSB12LV21, TSB12LV31, TSB12C01, TSB12LV22, TSB12LV41, or TSB12LV01.

The TSB21LV03C requires either an external 24.576-MHz crystal or crystal oscillator. The internal oscillator drives an internal phase-locked loop (PLL), which generates the required 196.608-MHz reference signal. The 196.608-MHz reference signal is internally divided to provide the 49.152/98.304-MHz clock signals that control transmission of the outbound encoded strobe and data information. The 49.152-MHz clock signal is also supplied to the associated LLC for synchronization of the two chips and is used for resynchronization of the received data. For the TSB21LV03C, the 49.152 MHz clock output is active when RESET\ is asserted low. The power-down function, when enabled by taking the PD terminal high, stops operation of the PLL and disables all circuitry except the cable-not-active signal circuitry.

The TSB21LV03C supports an optional isolation barrier between itself and its LLC. When ISO\ is tied high, the link interface outputs behave normally. Also, when ISO\ is tied high, the internal bus hold function is enabled for use with the TI Bus Holder isolation. TI bus holder isolation is implemented when ISO\ is tied high.

Data bits to be transmitted through the cable ports are received from the LLC on two or four data lines (D0 - D3), and are latched internally in the TSB21LV03C in synchronization with the 49.152-MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304 or 196.608 Mbits/s as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the TPB cable pair(s), and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

During packet reception the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded Strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are split into two or four parallel streams, resynchronized to the local system clock, and sent to the associated LLC. The received data is also transmitted (repeated) out of the other active (connected) cable ports.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common mode voltage is used during arbitration to set the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage for the presence of the remotely supplied twisted-pair bias voltage. The presence or absence of this common-mode voltage is used as an indication of cable connection status. The cable connection status signal is internally debounced in the TSB21LV03C on a cable disconnect-to-connect. The debounced cable connection status signal initiates a bus reset. On a cable disconnect-to-connect a debounce delay is incorporated. There is no delay on a cable disconnect.

The TSB21LV03C provides a 1.86-V nominal bias voltage for driver load termination. This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. The value of this bias voltage has been chosen to allow interoperability between transceiver chips operating from either 5-V or 3-V nominal supplies. This bias voltage source should be stabilized by using an external filter capacitor of approximately 1.0

uF.

The transmitter circuitry is disabled under the following conditions: power down, cable not active, reset, or transmitter disable. The receiver circuitry is disabled under the following conditions: power down, cable not active, or receiver disable. The twisted-pair bias voltage circuitry is disabled under the following conditions: power down or reset. The power-down condition occurs when the PD input is high. The cable-not-active (CNA) condition occurs when the cable connection status indicates that no cable is connected. The reset condition occurs when the RESET\ input terminal is low. The transmitter disable and receiver disable conditions are determined from the internal logic.

The line drivers in the TSB21LV03C operate in a high-impedance current mode and are designed to work with external 110- Ω line-termination resistor networks. One network is provided at each end of each twisted-pair cable. Each network is composed of a pair of series-connected 55- Ω resistors. The midpoint of the pair of resistors that is directly connected to the twisted-pair A (TPA) package terminals is connected to the TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the twisted-pair B (TPB) package terminals is coupled to ground through a parallel RC network with recommended resistor and capacitor values of 5 k Ω and 220 pF respectively. The values of the external resistors are designed to meet the draft standard specifications when connected in parallel with the internal receiver circuits and are shown in
Figure 3.

The driver output current, along with other internal operating currents, is set by an external resistor. This resistor is connected between the R0 and R1 terminals and has a value of 6.3 k Ω, ±0.5%. This might be accomplished by placing a 6.34 k Ω, ±0,5% resistor in parallel with a 1-M Ω resistor.

Four package terminals are used as inputs to set four configuration status bits in the self-identification (Self-ID) packet. These terminals are hardwired high or low as a function of the equipment design. PC0 - PC2 are the three terminals that indicate either the need for power from the cable or the ability to supply power to the cable. The fourth terminal, C/LKON, indicates whether a node is a contender for bus manager. When the C/LKON terminal is asserted, it means the node can be a contender for bus manager. When the terminal is not asserted, it means that the node is not a contender. The C bit corresponds to bit 20 in the Self-ID packet, PC0 corresponds to bit 21, PC1 corresponds to bit 22, and PC2 corresponds to bit 23 (see Table 4-29 of the IEEE 1394-1995 standard for additional details).

A power-down terminal, PD, is provided to allow a power-down mode where most of the TSB21LV03C circuits are powered down to conserve energy in battery-powered applications. A cable status terminal, CNA, provides a high output when all twisted-pair cable ports are disconnected. This output is not debounced. The CNA output can be used to determine when to power the TSB21LV03C down or up. In the power-down mode all circuitry is disabled except the CNA circuitry. It should be noted that when the device is powered-down it does not act in a repeater mode. When the TSB21LV03C is powered down using the PD terminal, the twisted-pair transmitter and receiver circuitry has been designed to present a high impedance to the cable to prevent loading the TPBias terminal voltage on the other end of the cable.

NOTE:
Reference suspend/resume section in the current 1394a specification for interoperability with PD implementation of power down.

If the TSB21LV03C is being used with one or more of the ports not being brought out to a connector, the TPB terminals must be terminated for reliable operation. For each unused port, the TPB+ and TPB- terminals must be connected to GND. This is done in the normal termination network. When a port does not have a cable connected, the normal termination network pulls TPB+ and TPB- to ground through a 5-k Ω resistor, thus disabling the port.

NOTE:
All gap counts on all nodes of a 1394 bus must be identical. This may only be accomplished by using phy configuration packets (see section 4.3.4.3 of IEEE 1394-1995 Standard) or by using two bus resets, which resets the gap counts to the maximum level (3 Fh).

The link power status (LPS) terminal works with the C/LKON terminal to manage the LLC power usage of the node. The LPS terminal indicates that the LLC of the node is powered down and powers down the phy-LLC interface to save power. If the phy then receives a link-on packet, the C/LKON terminal is activated to output a 6.114 MHz signal, which can be used by the LLC to power itself up. Once the LLC is powered up, the LPS signal communicates this to the TSB21LV03C and the C/LKON signal is turned off and the phy-link interface is enabled.

Two of the package terminals are used to set up various test conditions used in manufacturing. These terminals, TESTM1 and TESTM2, should be connected to V_{DD} for normal operation.

The TSB21LV03C is characterized for operation from 0°C to 70°C. The TSB21LV03CI is characterized for operation from -40°C to 85°C. The TSB21LV03CM is characterized for operation over the full military temperature range of -55°C to 125°C.

Features

- Fully Supports Provisions of IEEE 1394-1995 Standard for High Performance Serial Bus
- Fully Interoperable with FireWire™ and i.LINK™ Implementation of IEEE 1394-1995
- Provides Three Fully Compliant Cable Ports at 100/200 Megabits per Second (Mbits/s)
- Cable Ports Monitor Line Conditions for Active Connection to Remote Node
- Device Power-Down Feature to Conserve Energy in Battery-Powered Applications
- Inactive Ports Disabled to Save Power
- Logic Performs System Initialization and Arbitration Functions
- Encode and Decode Functions Included for Data-Strobe Bit-Level Encoding
- Incoming Data Resynchronized to Local Clock
- Single 3.3-V Supply Operation
- Interface to Link-Layer Controller Supports Low Cost TI™ Bus-Holder Isolation
- Data Interface to Link-Layer Controller Provided Through 2/4 Parallel Lines at 49.152 MHz
- Low Cost 24.576-MHz Crystal Oscillator and PLL Provide Transmit/Receive Data at 100/200 Mbits/s, and Link-Layer Controller Clock at 49.152 MHz
- Interoperable with 1394 Link-Layer Controllers Using 5-V Supplies
- Interoperable Across 1394 Cable with 1394 Physical Layers (Phy) Using 5-V Supplies
- Node Power-Class Information Signaling for System Power Management
- Cable Power Presence Monitoring
- Separate Cable Bias and Driver Termination Voltage Supply for Each Port
- High Performance 64-Pin TQFP (PM) Package and 68-Pin CFP (HV) Package

To view the following documents, Acrobat Reader 3.x is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

Datasheets

Full datasheet in Acrobat PDF: slls331a.pdf (393 KB)
Full datasheet in Zipped PostScript: slls331a.psz (363 KB)

Pricing/Samples/Availability

Orderable Device	Package	Pins	Temp (ºC)	Status	Price/unit USD (100-999)	Pack Qty	DSCC Number	Availability / Samples
TSB21LV03CIPM	PM	64		ACTIVE	11.56	160		Check stock or order
TSB21LV03CMHV	HV	68	-55 TO 125	ACTIVE	111.00	1		Check stock or order
TSB21LV03CMHVB	HV	68	-55 TO 125	ACTIVE	116.46	1	5962-9677101QXA	Check stock or order
TSB21LV03CPM	PM	64		ACTIVE	9.92	160		Check stock or order

Application Reports

- Capturing 1394 Events On The Twisted-Pair Lines (SLLA056 - Updated: 09/30/1999)
- Comparing Bus Solutions (SLLA067 - Updated: 03/02/2000)
- Galvanic Isolation of the IEEE1394-1995 Serial Bus (SLLA011 - Updated: 10/09/1997)
- Jitter Analysis (SLLA075 - Updated: 03/30/2000)
- Recommendations For Phy Layout (SLLA020A - Updated: 02/05/1999)
- TI IEEE 1394A Cable Transceiver/Arbiter FAQ (SLLA087 - Updated: 08/24/2000)

Related Documents

- TSB41LV03 to TSB41LV03A Transition Document (SLLA055A, 21 KB - Updated: 03/01/2000)

Table Data Updated on: 9/7/2000