

Ultralow capacitance ESD protection for antenna

Features

- ultralow diode capacitance 0.6 pF
- Single line, protected against 15 kV ESD
- breakdown voltage $V_{BR} = 6.0 \text{ V min.}$
- Flip Chip 400 μm pitch, lead-free
- very low leakage current
- very small PCB area
- RoHS compliant

Benefits

- minimized impact on rise and fall times for maximum data integrity
- low PCB space occupation
- higher reliability through monolithic integration

Complies with the following standards

- IEC 61000-4-2 level 4:
 - 15 kV (air discharge)
 - 8 kV (contact discharge)
- MIL STD 883G - Method 3015.7:
 - 25 kV (human body model)

Applications

- antenna protection
- DVB - H
- GPS

Description

The ESDARF03-1BF3 is a monolithic, application specific discrete device dedicated to ESD protection of antennas.

Its ultralow line capacitance secures a high level of signal integrity without compromising the protection of sensitive chips against the most stringently characterized ESD strikes.

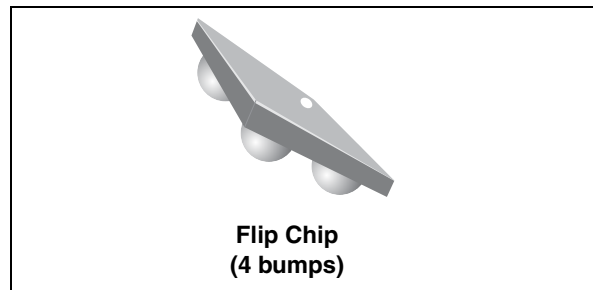


Figure 1. Pin layout (bump side)

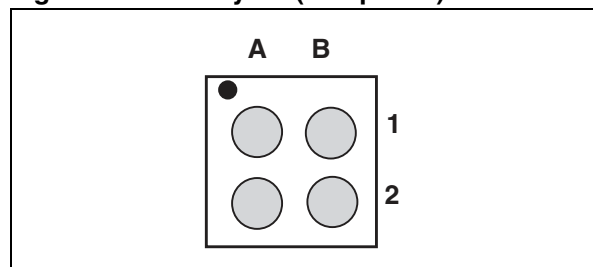
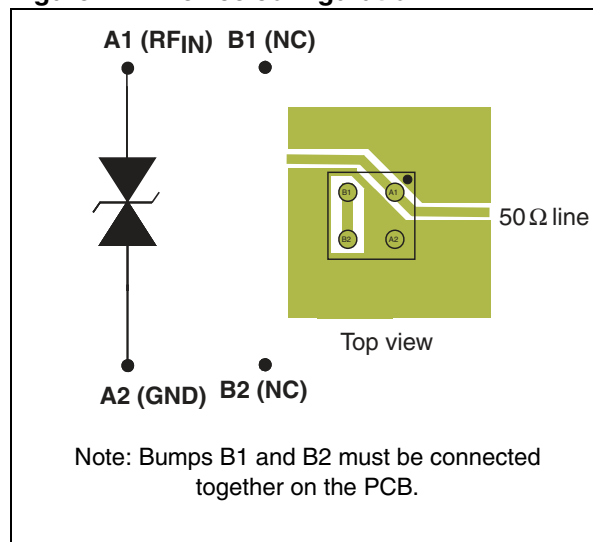


Figure 2. Device configuration



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1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2, air discharge	15	kV
	ESD discharge IEC 61000-4-2, contact discharge	8	
P_{PP}	Peak pulse power dissipation (8/20 μs)	60	W
T_j	Maximum junction temperature	125	$^{\circ}\text{C}$
T_{op}	Operating temperature range	-30 to + 85	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-55 to +150	$^{\circ}\text{C}$

Figure 3. Electrical characteristics (definitions)

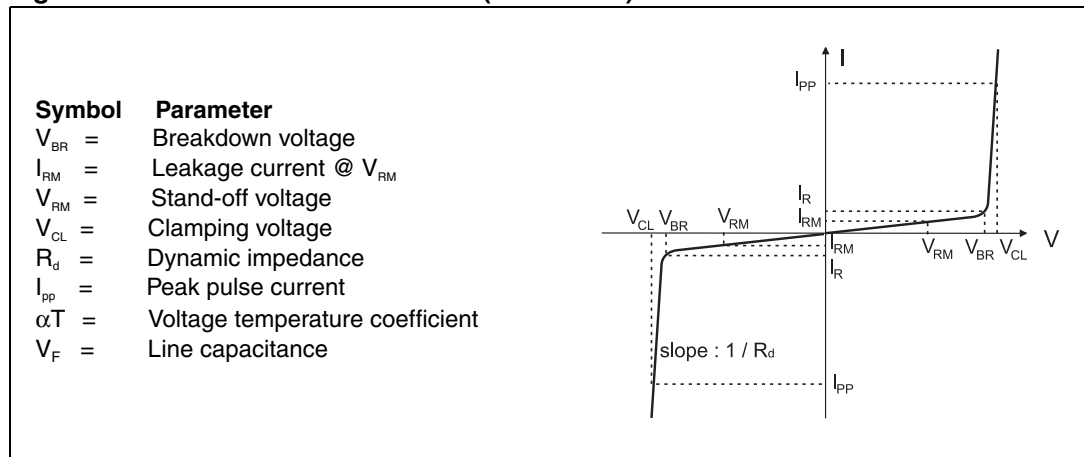


Table 2. Electrical characteristics ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1\text{ mA}$	6	9		V
I_{RM}	$V_{RM} = 3\text{ V}$			100	nA
R_d	Exponential wave form 8/20 μs , $I_{pp} = 1\text{ to }5\text{ A}$		2.6		Ω
αT	$I_R = 1\text{ mA}$			5	$10^{-4}/^{\circ}\text{C}$
C_{line}	$V_{LINE} = 0\text{ V}$, $V_{OSC} = 30\text{ mV}$, $F = 1\text{ MHz}$		0.6	0.8	pF

Figure 4. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

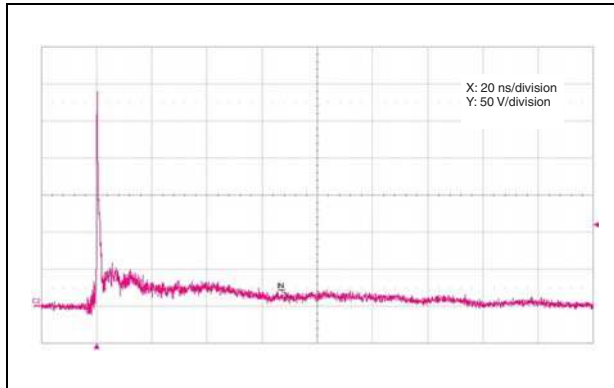


Figure 5. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

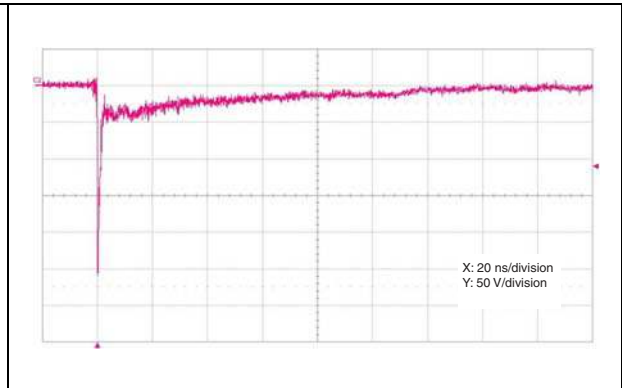


Figure 6. Junction capacitance versus frequency (typical values)

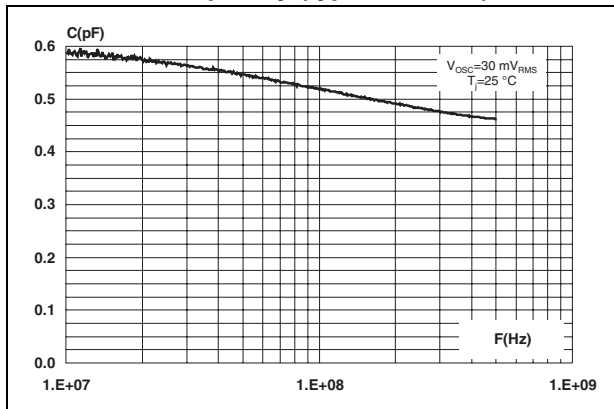


Figure 7. S21 attenuation measurement

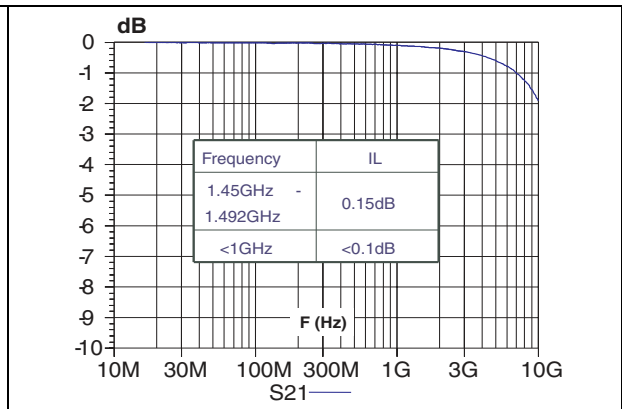
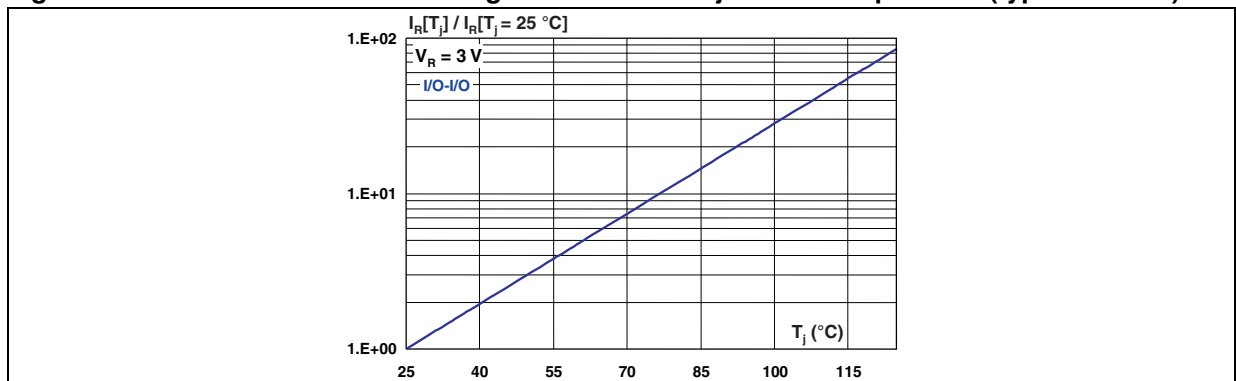
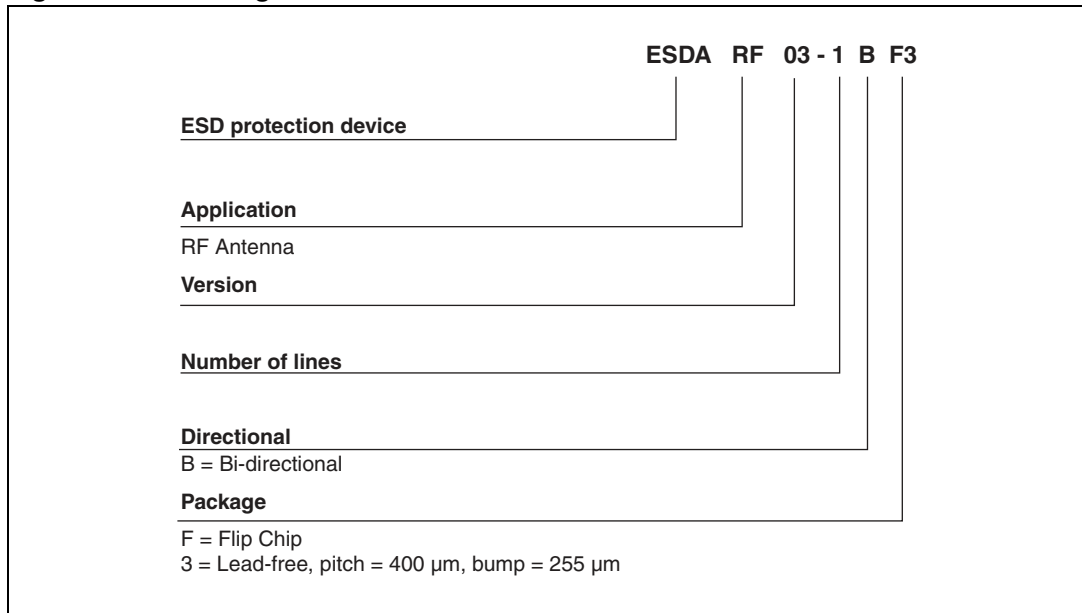


Figure 8. Relative variation of leakage current versus junction temperature (typical values)



2 Ordering information scheme

Figure 9. Ordering information scheme



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 10. Package dimensions

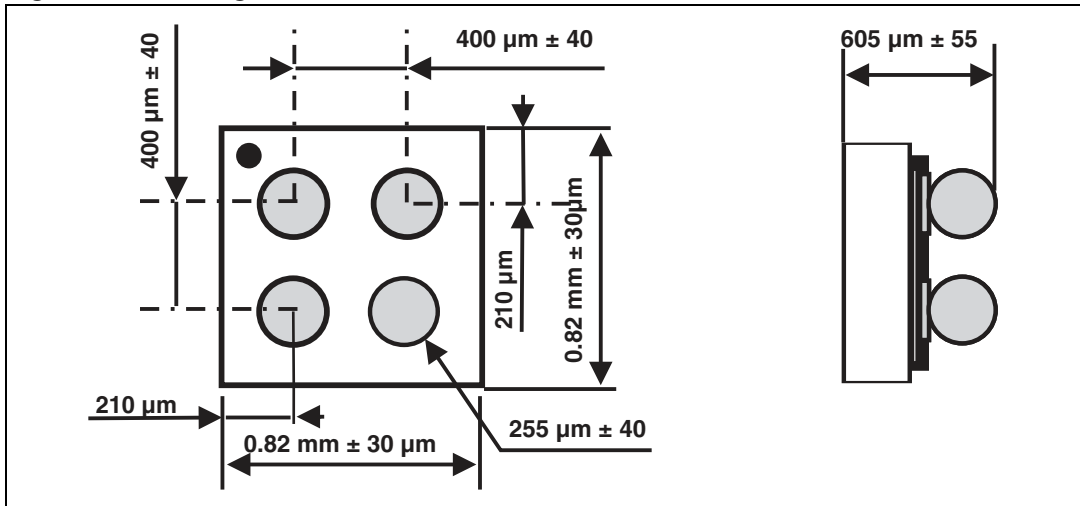


Figure 11. Footprint recommendations **Figure 12. Marking**

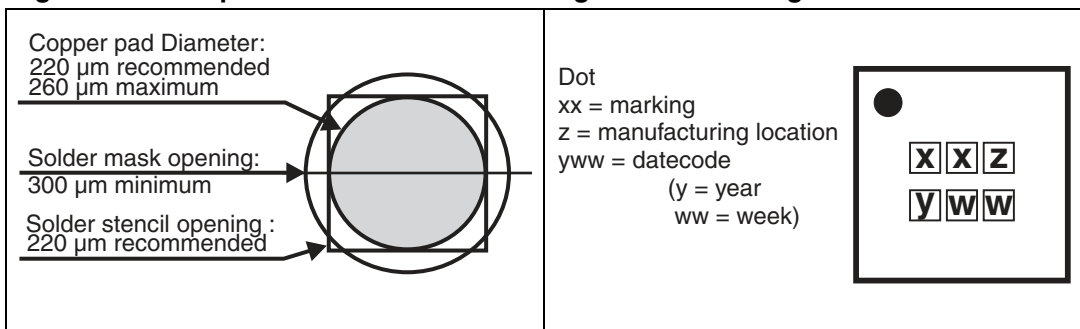
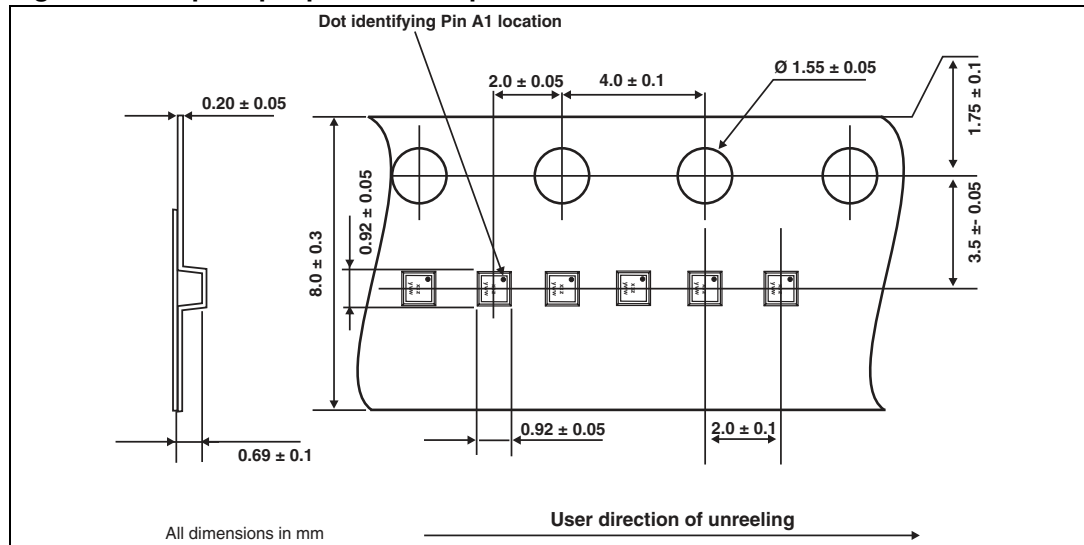


Figure 13. Flip Chip tape and reel specifications



Note: More information is available in the application notes:
 AN2348: “400 μm Flip Chip: Package description and recommendations for use”
 AN1751: “EMI Filters: Recommendations and measurements”

4 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ESDARF03-1BF3	R3	Flip Chip	0.91 mg	5000	Tape and reel (7")

5 Revision history

Table 4. Document revision history

Date	Revision	Changes
15-Nov-2010	1	Initial release.

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