PLL AUDIO CLOCK SYNTHESIZER

MK2703

Description

The MK2703 is a low-cost, low-jitter, high-performance PLL clock synthesizer designed to replace oscillators and PLL circuits in set-top box and multimedia systems. Using IDT's patented analog Phase Locked Loop (PLL) techniques, the device uses a 27 MHz crystal or clock input to produce a buffered reference clock and a selectable audio clock.

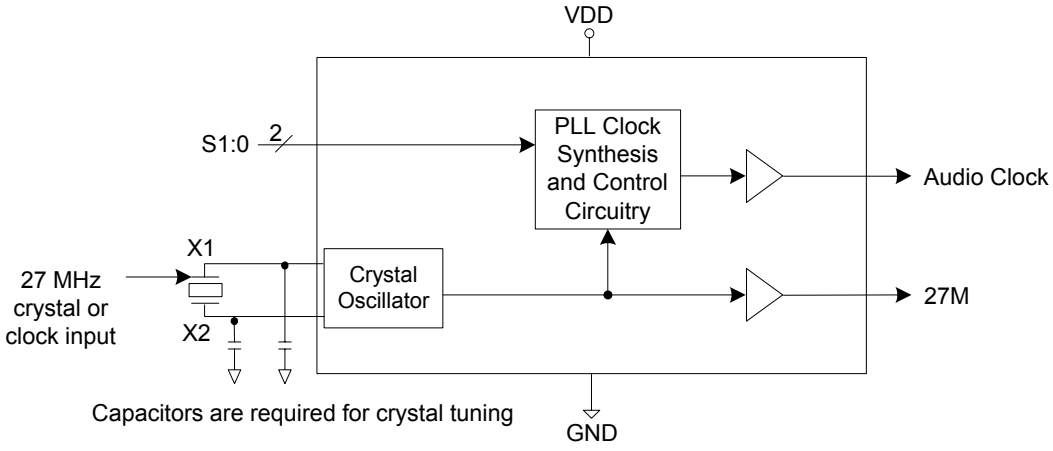
IDT manufactures the largest variety of Set-Top Box and multimedia clock synthesizers for all applications. Consult IDT to eliminate VCXOs, crystals and oscillators from your board.

Features

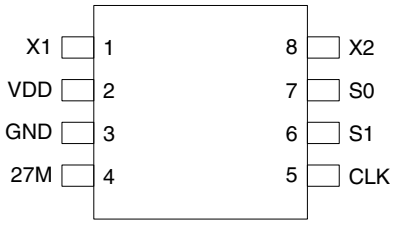
- Packaged in 8-pin SOIC
- Available in Pb (lead) free package
- Uses an inexpensive, fundamental mode crystal or clock
- Supports MPEG sampling rates of 32 kHz, 44.1 kHz, 48 kHz, and 96 kHz
- Patented zero ppm synthesis error in all clocks
- All frequencies are frequency locked
- Advanced, low power, sub-micron CMOS process
- Operating voltage of 3.3 V or 5 V
- Industrial temperature version available
- ***The MK2703B is recommended for new designs***

NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

Block Diagram



Pin Assignment



8-pin (150 mil) SOIC

AUDIO CLOCK OUTPUT SELECT TABLE

S1	S0	CLK (MHz)
0	0	8.192
0	1	11.2896
1	0	12.288
1	1	24.576

Key: 0 = Connect pin directly to ground

1 = Connect pin directly to VDD

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1	XI	Crystal Connection. Connect to a 27 MHz fundamental crystal or clock.
2	VDD	Power	Connect to +3.3 V or +5 V.
3	GND	Power	Connect to ground.
4	27M	Output	27 MHz buffered reference clock output.
5	CLK	Output	Audio clock output per table above.
6	S1	Input	Audio clock frequency select input #1. Determines CLK output per table above. Internal pull-up resistor.
7	S0	Input	Audio clock frequency select input #0. Determines CLK output per table above. Internal pull-up resistor.
8	X2	XO	Crystal connection to a 27 MHz crystal, or leave unconnected for clock output.

External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the MK2703 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between VDD and GND on pins 2 and 3. It must be connected close to the MK2703 to minimize lead inductance. No external power supply filtering is required for the MK2703.

Series Termination Resistor

A 33Ω terminating resistor can be used next to the clock outputs for trace lengths over one inch.

Crystal Load Capacitors

The total on-chip capacitance is approximately 16 pF. A parallel resonant, fundamental mode, AT cut 27 MHz crystal should be used. The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the

stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors, if needed, must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal (C_L -16 pF)*2. In this equation, C_L= crystal load capacitance in pF. Example: For a crystal with an 18 pF load capacitance, each crystal capacitor would be 4 pF [(18-16) x 2] = 4.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK2703. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	-0.5 V to 7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature, MK2703S (commercial)	0 to +70° C
Ambient Operating Temperature, MK2703SI (industrial)	-40 to +85° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	° C
Power Supply Voltage (measured in respect to GND)	+3.13		+5.50	V

DC Electrical Characteristics

VDD=3.3 V ±5% , Ambient temperature -40 to +85° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.13		5.50	V
Input High Voltage	V_{IH}	X1 pin only Note 1	(VDD/2)+1	VDD/2		V
Input Low Voltage	V_{IL}	X1 pin only Note 1		VDD/2	(VDD/2)-1	V
Input High Voltage	V_{IH}	S0, S1 pins	2.0			V
Input Low Voltage	V_{IL}	S0, S1 pins			0.8	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Output High Voltage, CMOS level	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Operating Supply Current	IDD	No load VDD = 3.3 V		25		mA
Short Circuit Current		CLK output		±50		mA
Input Capacitance	C_{IN}	S0, S1 pins		5		pF
Nominal Output Impedance				20		Ω
Frequency Synthesis Error		All Clocks			0	ppm
Internal Pull-up Resistor	R_{PUP}	S1, S0 pins		500		kΩ

Note 1: CMOS level input. Nominal trigger point is VDD/2 for 3.3 V or 5 V operation.

AC Electrical Characteristics

VDD = 3.3 V ±5%, Ambient Temperature -40 to +85° C, unless stated otherwise

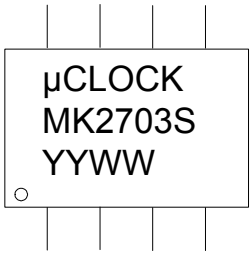
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Crystal or Clock Frequency	F_{IN}			27		MHz
Output Clock Rise Time	t_{OR}	0.8 to 2.0 V, Note 1			1.5	ns
Output Clock Fall Time	t_{OF}	2.0 to 8.0 V, Note 1			1.5	ns
Clock Stabilization Time after Power-up					10	ms
Changing Frequency Setting					10	ms
Output Clock Duty Cycle		at VDD/2, Note 1	40		60	%
Maximum Absolute Jitter, short term	t_{ja}	Deviation from mean		±190		ps

Note 1: Measured with 15 pF load.

Thermal Characteristics

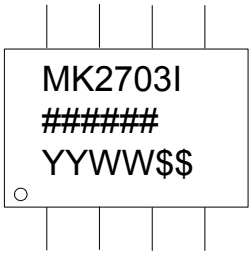
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Marking Diagram - MK2703S



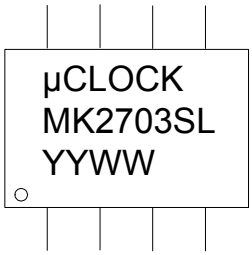
Bottom Marking:
Line 1: ######
Line 2 & 3: Origin

Marking Diagram - MK2703SI



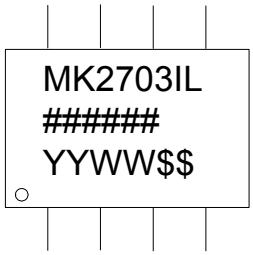
Bottom Marking:
Origin

Marking Diagram - MK2703SLF



Bottom Marking:
Line 1: ######
Line 2 & 3: Origin

Marking Diagram - MK2703SILF



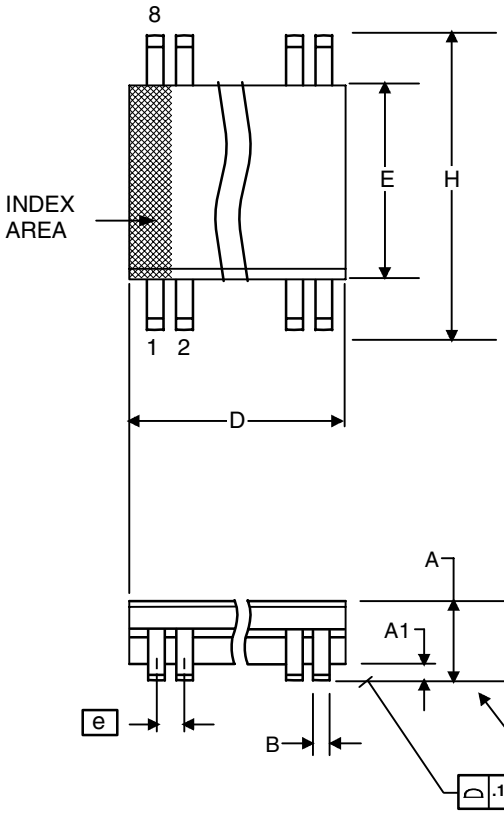
Bottom Marking:
Origin

Notes:

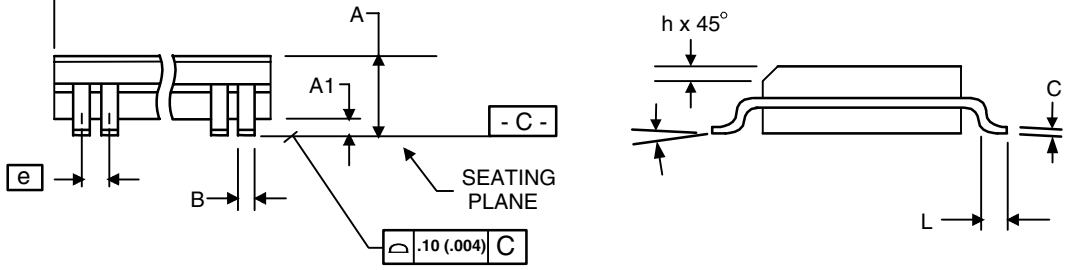
1. ###### is the lot number.
2. YYWW is the last two digits of the year and the week number that the part was assembled.
3. Bottom mark denotes country of origin.

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK2703S*	see page 5	Tubes	8-pin SOIC	0 to +70° C
MK2703STR*		Tape and Reel	8-pin SOIC	0 to +70° C
MK2703SLF	see page 5	Tubes	8-pin SOIC	0 to +70° C
MK2703SLFTR		Tape and Reel	8-pin SOIC	0 to +70° C
MK2703SI*	see page 5	Tubes	8-pin SOIC	-40 to +85° C
MK2703SITR*		Tape and Reel	8-pin SOIC	-40 to +85° C
MK2703SILF	see page 5	Tubes	8-pin SOIC	-40 to +85° C
MK2703SILFTR		Tape and Reel	8-pin SOIC	-40 to +85° C

***NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01**

"LF" denotes Pb (lead) free package.

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