TRIPLE 3-INPUT "AND" GATE
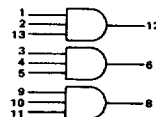
MC3106F · MC3006F
MC3106L · MC3006L,P
(54H11J)   (74H11J,N)

This device consists of three 3-input AND gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.
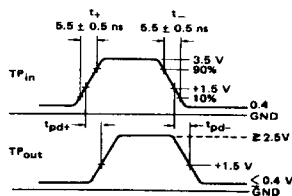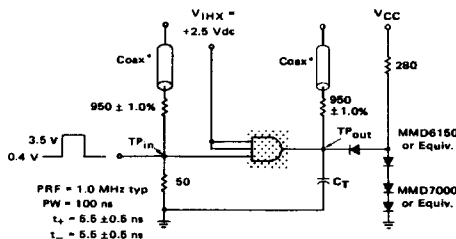
1/3 OF CIRCUIT SHOWN

Positive Logic: 12 = 1 · 2 · 13
Negative Logic: 12 = 1 + 2 + 13

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 84 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT

PRF = 1.0 MHz typ
PW = 100 ns
t_+ = 5.5 ±0.5 ns
t_- = 5.5 ±0.5 ns

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

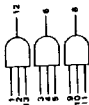C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.
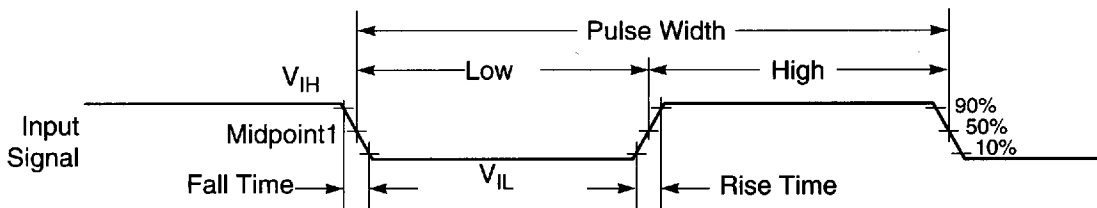
Characteristic	Symbol	Pin Under Test	MC3106 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3006 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	@ Test Temperature	Unit
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	MC3106 {-55°C / +25°C / +125°C / MC3006 {0°C / +25°C / +75°C	mAdc
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50		µAdc
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-		Vdc
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-		Vdc
Output Output Voltage	V_{OL}	12	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4		Vdc
	V_{OH}	12	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-		Vdc
Short-Circuit Current	I_{SC}	12	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100		mAdc
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	26	-	26	-	-	-	26	-	15		mAdc
Power Supply Drain	I_{PDH}	14	-	18	-	18	-	18	-	18	-	18	-	12		mAdc
	I_{PDL}	14	-	36	-	36	-	36	-	36	-	36	-	36		mAdc
Switching Parameters Turn-On Delay	t_{pd+}	1,12	-	-	-	-	-	15	-	-	-	-	-	-		ns
Turn-Off Delay	t_{pd-}	1,12	-	-	-	-	-	12	-	-	-	-	-	-		ns

TEST CURRENT/VOLTAGE VALUES

Symbol	mA I_{OL}	I_{OH}	I_{in}	I_D	Volts V_IL	V_{IH}	V_F	V_R	V_{BH}	V_{min}	V_{CC}	V_{CCL}	V_{CCH}	V_{out}	Gnd
I_F	20	-2.0			1.1	2.0	0.4	2.4	4.0		5.0	4.5	5.5	- 2.5	7
I_R	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5		2,7,13
BV_{in}	20	-2.0			0.8	1.8	0.4	2.4	4.0		5.0	4.5	5.5		2,7,13
V_D	20	-2.0	1		1.1	2.0	0.4	2.5	4.0		5.0	4.75	5.25		7
V_{OL}	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5	7
V_{OH}	20	-2.0			0.9	1.8	0.4	2.5	4.0		5.0	4.75	5.25		7

TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:

Symbol	I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{BH}	V_{min}	V_{CC}	V_{CCL}	V_{CCH}	V_{out}	Gnd
V_{OL}	12			1					2,13*						7
V_{OH}		12				1			2,13*						7
I_{SC}									1,2,13*		14				7,12
I_{max}									1,2,3,4,5, 9,10,11,13	14					7
I_{PDH}									1,2,3,4,5, 9,10,11,13		14				7
I_{PDL}									1,2,3,4,5,7, 9,10,11,13		14				1,2,3,4,5,7, 9,10,11,13
t_{pd+}	Pulse In 1	Pulse Out 12							*		14			2.13	7
t_{pd-}	1	12							*		14			2.13	7

*Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{RH}.

AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, $\overline{RESET}$, MODA, MODB, and MODC. These pins are tested using the input levels set forth in the DC Electrical Characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56002 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.

Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

AA0179

Figure 2-1 Signal Measurement Reference