AS1504, AS1505

DataSheet

Octal 8-Bit Programmable Low-Power DACs with Shutdown and Mid-Scale Reset

1 General Description

The AS1504/AS1505 are low-power (5µA @ 5V) individually programmable 8-channel, 8-bit resolution digital-to-analog converters. All eight DACs share a common reference-voltage input making them ideal for applications where adjustments start at a nominal voltage.

Table 1. Standard Products

Model	Functionality
AS1504	Mid-Scale Reset Pin
AS1505	Separate VREFL Range Settings

The devices feature a low-power shutdown reference input current (5µA) that enables the devices to maintain individual DAC latch settings during shutdown until normal operation is resumed.

The devices are controlled via a standard 3-wire serial interface. Data is shifted into the DACs via the internal serial-to-parallel shift register.

The AS1504/AS1505 are available in a 16-pin SOIC-150 package.

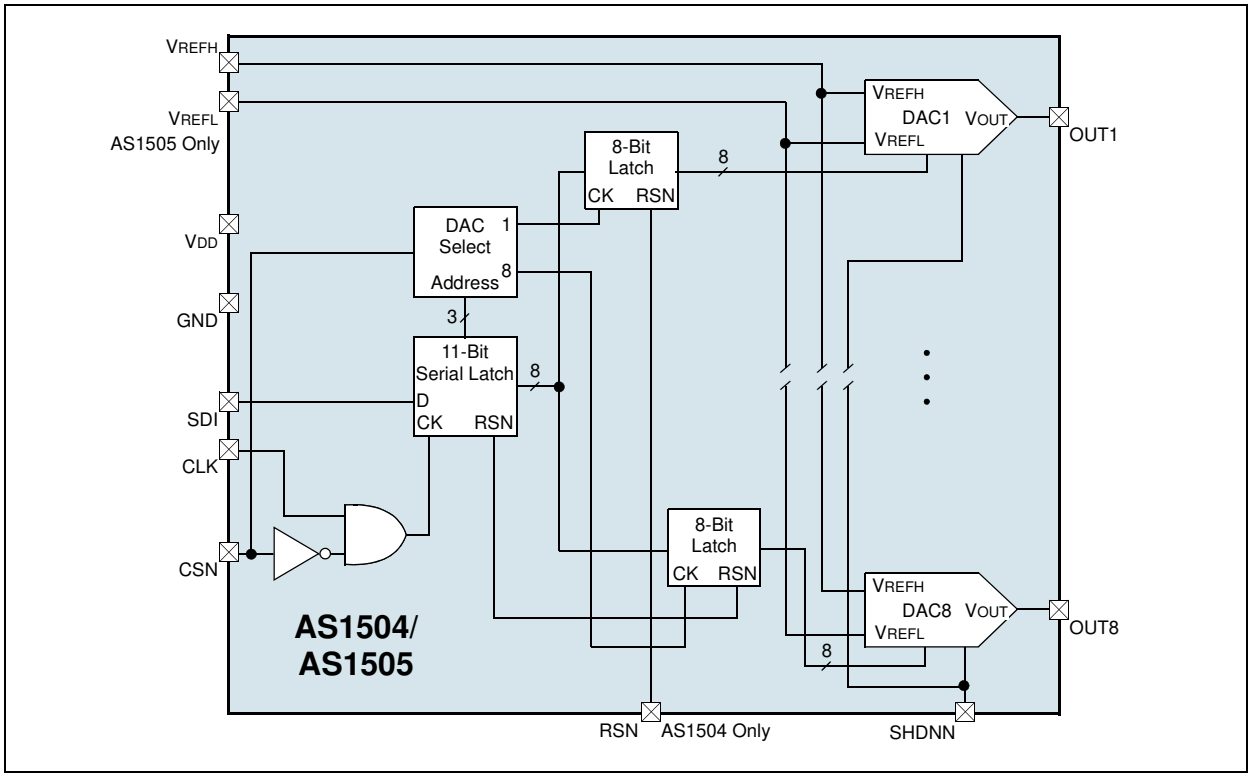
2 Key Features

- 8 Individually-Controlled DACs
- Replaces 8 Potentiometers
- Standard 3-Wire Serial Interface
- Single-Supply Operation: +3 to +5V
- Mid-Scale Reset Pin (AS1504)
- Separate VREFL Range Setting (AS1505)
- Shutdown Mode: ≤25µW (IDD and IREF)
- Power-On Reset
- 16-pin SOIC-150 Package

3 Applications

The devices are ideal for video amplifier gain control, video equipment voltage-controlled frequencies and bandwidths, CRT display geometric corrections and automatic adjustments, or any other space-limited DAC application with low power-consumption requirements.

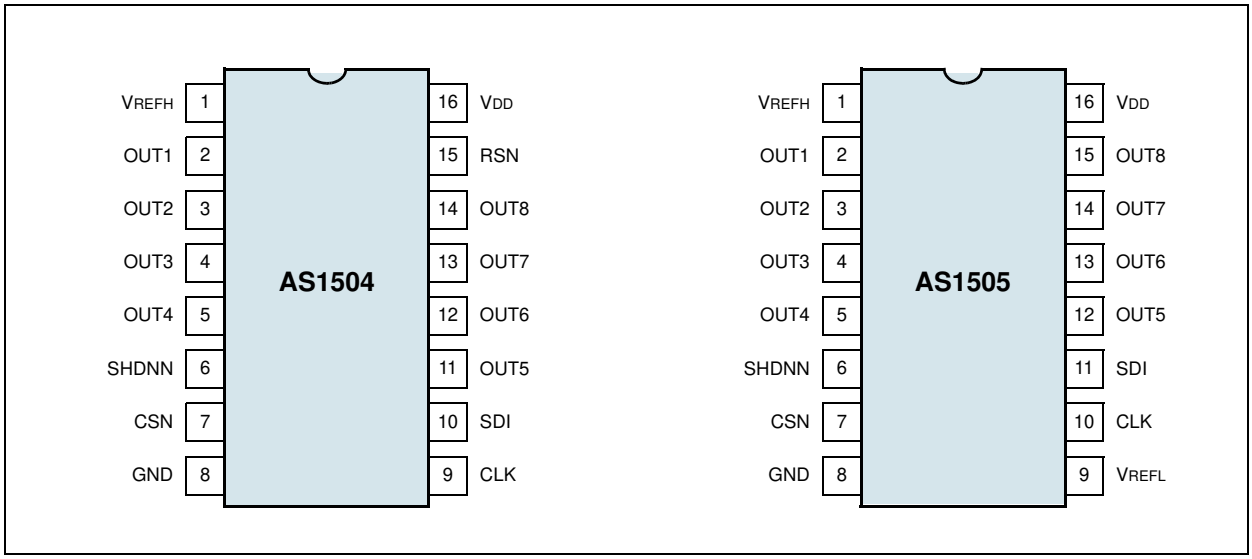
Figure 1. Block Diagram



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 2. Pin Descriptions

Pin Number	Pin Name	Description
(see Figure 2)	CLK	**Serial Clock Input**. Positive-edge triggered.
	CSN	**Chip Select**. When this active-low pin goes high, the serial input register data is decoded based on the address bits and loaded into the target DAC register.
	GND	**Ground**
	OUT1	**DAC 1 Output**. DAC 1 address = 000_2.
	OUT2	**DAC 2 Output**. DAC 1 address = 001_2.
	OUT3	**DAC 3 Output**. DAC 1 address = 010_2.
	OUT4	**DAC 4 Output**. DAC 1 address = 011_2.
	OUT5	**DAC 5 Output**. DAC 1 address = 100_2.
	OUT6	**DAC 6 Output**. DAC 1 address = 101_2.
	OUT7	**DAC 7 Output**. DAC 1 address = 110_2.
	OUT8	**DAC 8 Output**. DAC 1 address = 111_2.
	RSN	**Reset** (AS1504 Only). Active-low asynchronous reset to mid-scale output setting. Loads all DAC latches with 80_h.
	SDI	**Serial Data Input**
	SHDNN	**Shutdown**. Active-low reference input open-circuit. All DAC outputs open-circuit. **Note:** DAC latch settings are maintained during shutdown.
	VDD	**Positive Supply Voltage**. +3 to +5V.
	VREFH	**Common High-Side DAC Reference Input**
	VREFL	**Common Low-Side DAC Reference Input** (AS1505 Only).

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
V_{DD} to GND	-0.3	+7	V	
V_{REFH} and V_{REFH} to GND	0	V_{DD}	V	
OUT*x* to GND	0	V_{DD}	V	
Digital Input Voltage to GND	0	V_{DD}	V	
Package Power Dissipation				T_J Max - T_{AMB}/θ_{JA}
Operating Temperature Range	-40	+85	ºC	
Storage Temperature Range	-65	+150	ºC	
Maximum Junction Temperature (T_J Max)		+150	ºC	
Thermal Resistance (θ_{JA})		60	ºC/W	
Electro-Static Discharge		<1	kV	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in compliance with *IPC/JEDEC J-STD-020C "Moisture/ Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"*.

6 Electrical Characteristics

V_{DD} = +3.0V ±10% or +5.0V ±10%, V_{REFH} = V_{DD}, V_{REFL} = 0V, -40ºC ≤ T_{AMB} ≤ +85ºC (unless otherwise specified).

Table 4. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
Static Accuracy (specifications apply to all DACs)						
N	Resolution		8			Bit
INL	Integral Non-Linearity Error		-0.75	±0.15	+0.75	LSB
DNL	Differential Non-Linearity	Guaranteed Monotonic	-0.5	±0.1	+0.5	LSB
G_{FSE}	Full-Scale Error		-1	±0.2	+1	LSB
V_{ZSE}	Zero-Code Error		-0.5	±0.1	+0.5	LSB
R_{OUT}	DAC Output Resistance		3	5	8	kΩ
ΔR/R_{OUT}	Output Resistance Match			1		%
Reference Input						
V_{REFH}	High Voltage Input Range [2]		0		V_{DD}	V
V_{REFL}	Low Voltage Input Range (AS1505 Only) [3]		0		V_{DD}	V
R_{IN}	Input Resistance [4]	Digital Inputs = 55h, V_{REFH} ≈ V_{DD}		625		Ω
C_{REFH}	High Reference Input Capacitance [5]	Digital Inputs = All 0s		60		pF
C_{REFL}	Low Reference Input Capacitance [5]	Digital Inputs = All 1s		60		pF
Digital Inputs						
V_{IH}	Logic High	V_{DD} = +5V	2.4			V
		V_{DD} = +3V	2.1			
V_{IL}	Logic Low	V_{DD} = +5V			0.8	V
		V_{DD} = +3V			0.6	
I_{IL}	Input Current	V_{IN} = 0 or +5V			±1	µA
C_{IL}	Input Capacitance [5]			5		pF
Power Supplies [6]						
$V_{DDRANGE}$	Power Supply Range		2.7		5.5	V
I_{DD}	Supply Current (CMOS)	V_{IH} = V_{DD} or V_{IL} = 0V		0.01	5	µA
	Supply Current (TTL)	V_{IH} = 2.4V or V_{IL} = 0.8V, V_{DD} = +5.5V		1	4	mA
I_{REFH}	Shutdown Current	SHDNN = 0V		0.01	5	µA
P_{DISS}	Power Dissipation	V_{IH} = V_{DD} or V_{IL} = 0V, V_{DD} = +5.5V			27.5	µW
PSRR	Power Supply Rejection Ratio	V_{DD} = +5V ±10%, V_{REFH} = +4.5V		0.001	0.002	%/%
		V_{DD} = +3V ±10%, V_{REFH} = +2.7V		0.01		
Dynamic Performance [5]						
tS	Positive or Negative V_{OUT} Settling Time	±0.5 LSB Error Band		0.5		µs
CT	Crosstalk [7]			90		dB

Table 4. Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
Switching Characteristics [5, 8]						
t_{CH}	Input Clock Pulse Width	High Clock Level	15			ns
t_{CL}		Low Clock Level	15			ns
t_{DS}	Data Setup Time		5			ns
t_{DH}	Data Hold Time		5			ns
t_{CSS}	CSN Setup Time		10			ns
t_{CSW}	CSN High Pulse Width		10			ns
t_{RS}	Reset Pulse Width		60			ns
t_{CSH}	CLK-Rise to CSN-Rise Hold Time		15			ns
t_{CS1}	CSN-Rise to Next Rising Clock Time		10			ns

1. Typ values are average readings at +25ºC.
2. V_{REFH} can be any value between V_{DD} and GND.
3. V_{REFL} can be any value between V_{DD} and GND.
4. With all DACs set to code 0x55h. Typical input resistance per DAC is 5kOhm with code 0x55h.
5. Guaranteed by design; not subject to production test.
6. V_{IN} = 0V or V_{DD} (CMOS); DAC outputs unloaded. P_{DISS} is calculated as I_{DD} x V_{DD}.
7. Measured at an OUT*x* pin where an adjacent OUT*x* pin is making a full-scale voltage change.
8. See Figure 13 on page 9 for location of measured values. All input control voltages are specified with t_R = t_F = 2ns.

7 Typical Operating Characteristics

Figure 3. Differential Non-Linearity; V_{DD} = 2.7V, V_{REFH} = 2.7V, V_{REFL}= 0V, T_{AMB} = -40, +25, and +85ºC

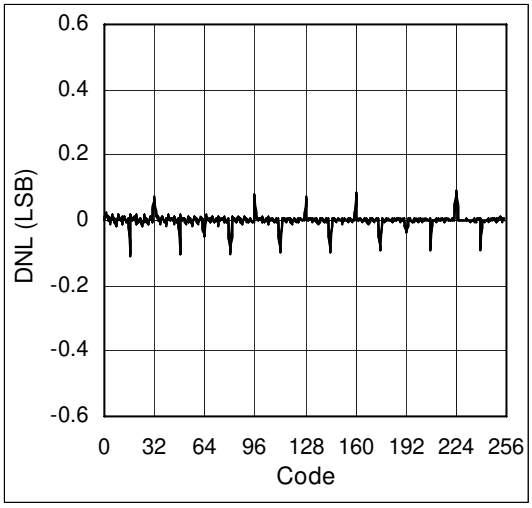


Figure 4. Integral Non-Linearity; V_{DD} = 2.7V, V_{REFH} = 2.7V, V_{REFL}= 0V, T_{AMB} = -40, +25, and +85ºC

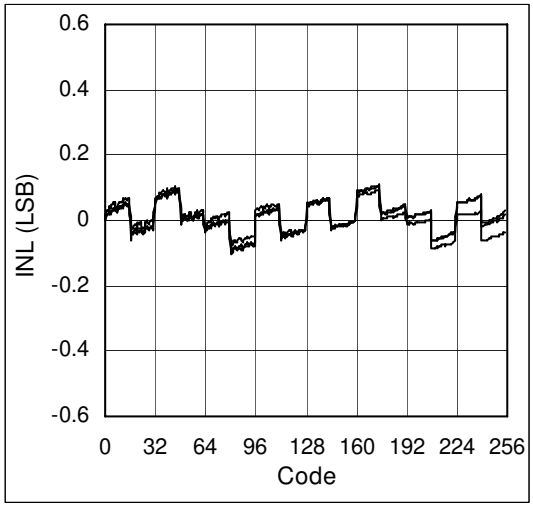


Figure 5. Reference Current vs. Code; V_{DD} = 2.7V, V_{REFH} = 2.7V, V_{REFL}= 0V

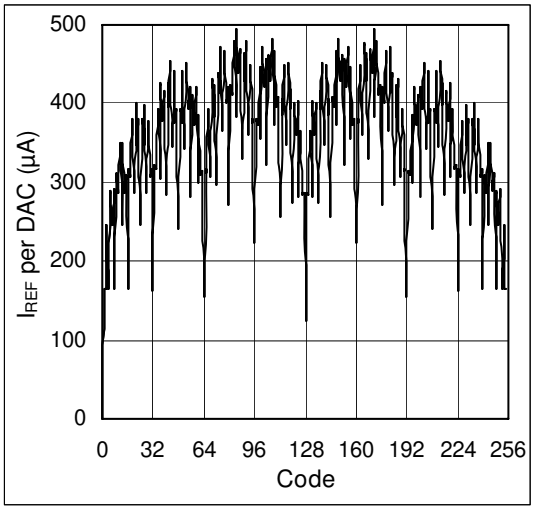


Figure 6. Reference Current vs. Code; V_{DD} = 5.5V, V_{REFH} = 5.5V, V_{REFL}= 0VReference C.

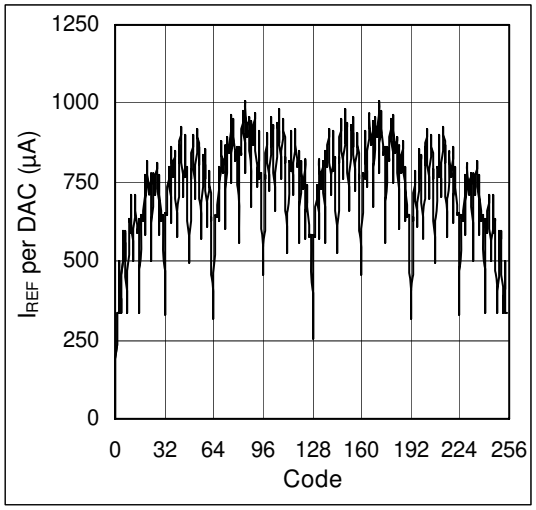


Figure 7. DNL vs. Channel; V_{DD} = 2.7V, T = 25ºC

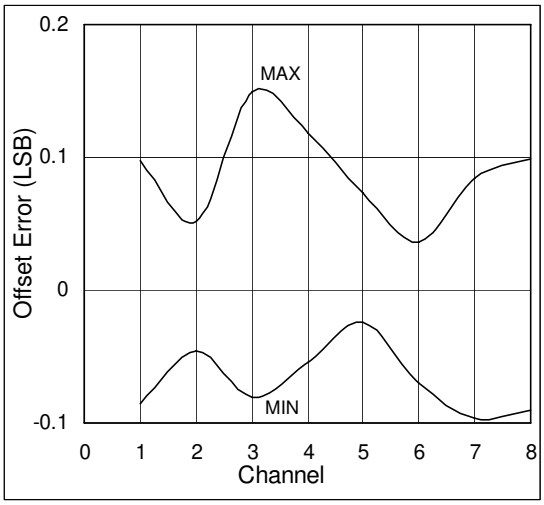


Figure 8. Offset Error vs. Channel; V_{DD} = 2.7V, T = 25ºC, all DACs (except selected) = 0x00h

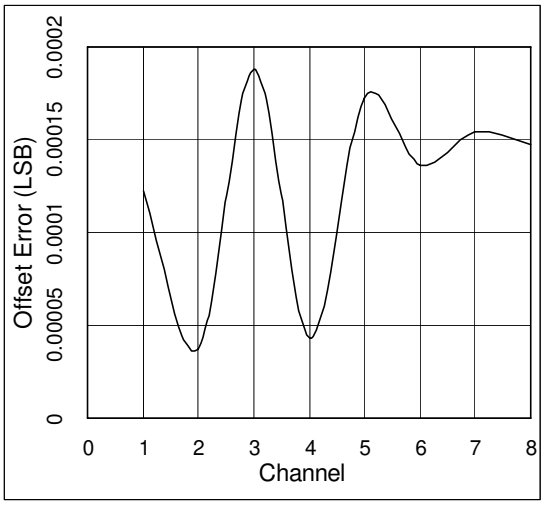


Figure 9. Gain Error vs. Channel;
V_{DD} = 2.7V, T = 25ºC, all DACs (except selected) = 0x00h

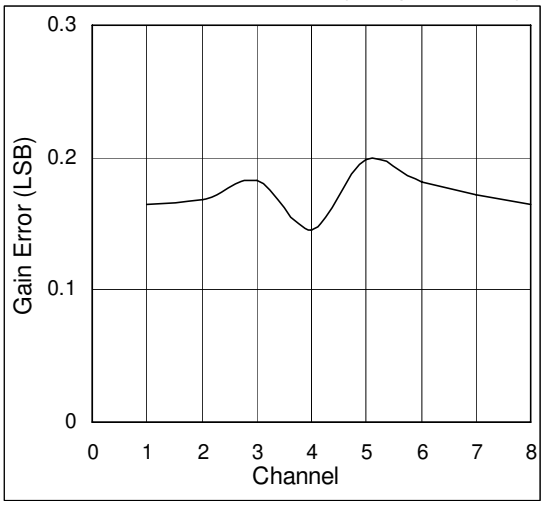
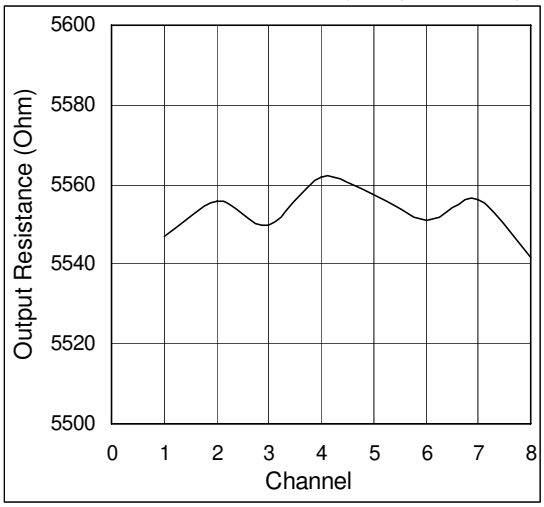


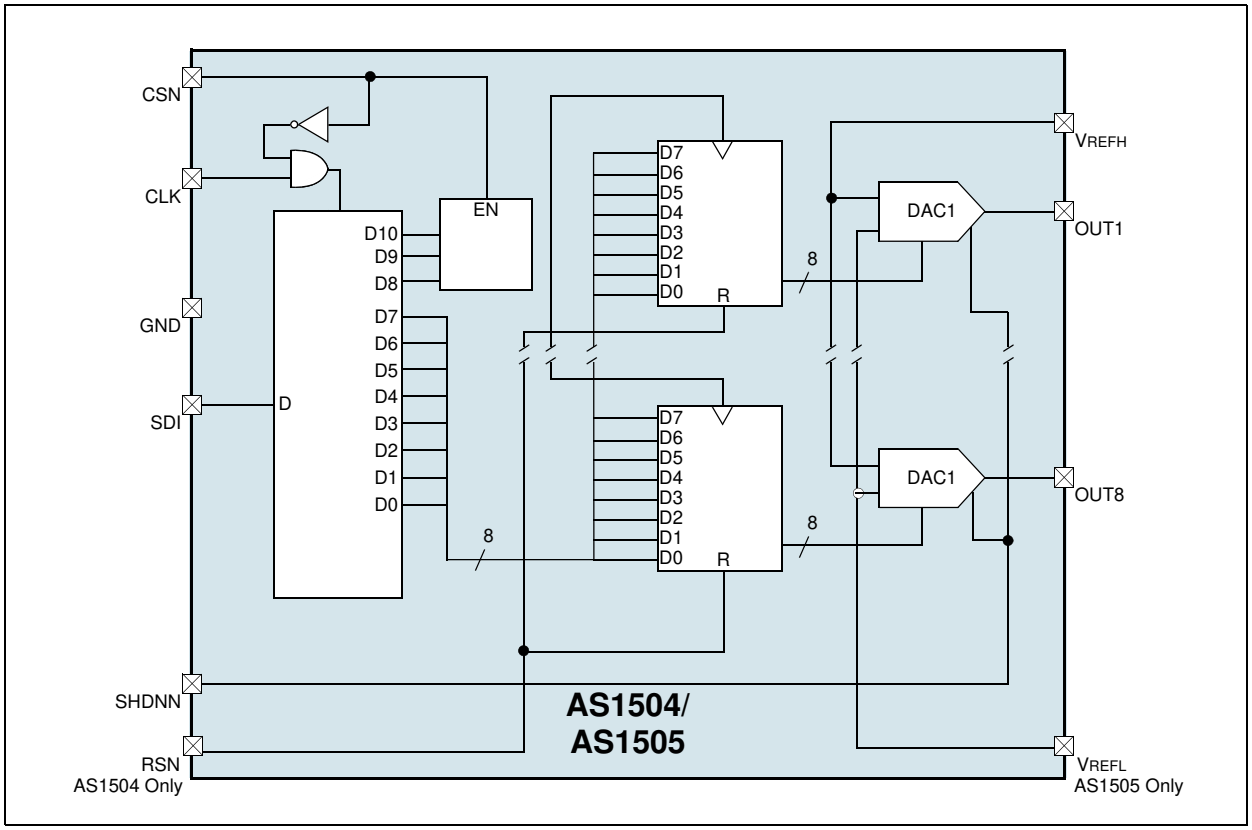
Figure 10. Output Resistance vs. Channel;
V_{DD} = 2.7V, T = 25ºC, all DACs (except selected) = 0x00h



8 Detailed Description

The AS1504/AS1505 contain eight DAC channels of programmable voltage output adjustment capability. OUT*x* can be individually changed in random sequence. The fast serial-data loading (33MHz) allows all eight DACs to be quickly loaded (3ms typ; 12 x 8 x 30ns).

Figure 11. Detailed Block Diagram



Each output voltage can be programmed by clocking an 11-bit serial data word into pin SDI (see Figure 12). The format of this data word is three address bits (MSB first, followed by eight data bits (see Table 5)).

To determine which of the DAC registers is to receive the serial register data (bits B7:B0) the DACx address is decoded as:

$$DACx = A2 \times 4 + A1 \times 2 + A0 + 1 \qquad (EQ\ 1)$$

Figure 12. Timing Diagram

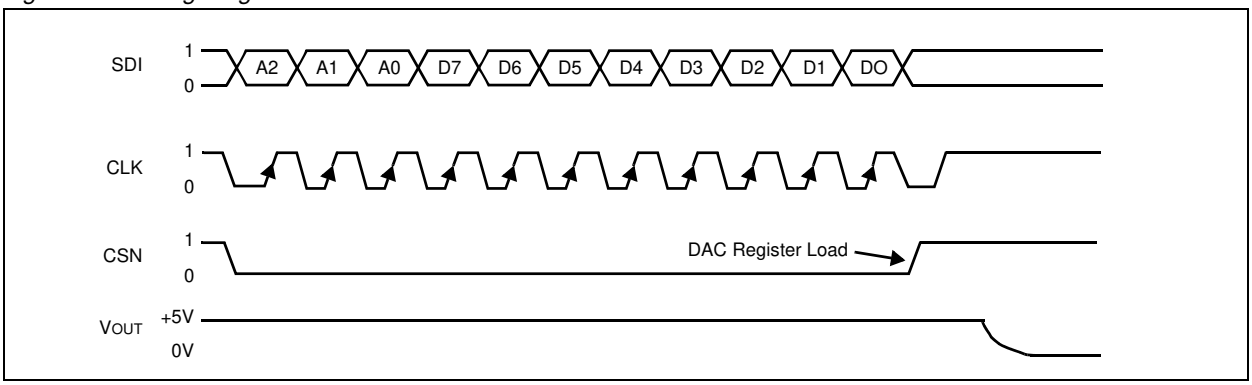


Table 5. AS1504/AS1505 Serial Data Word Format

Address Bits			Data Bits							
B10	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
MSB		LSB	MSB							LSB
2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

The AS1504 provides a mid-scale reset activated by pin RSN which simplifies settings on initial power up. The AS1505 has a high- and low-side reference (pins VREFH and VREFL) to determine independent positive full-scale and zero-scale settings to optimize resolution. -

Both devices feature a power-on reset which resets them to mid-scale.

Both models feature a low-power shutdown mode which places the device into low power-consumption mode resulting in only leakage currents being consumed from the power supply, VREFx inputs, and all 8 outputs. In shutdown mode the DAC*x* latch settings are maintained. When returning to normal operation from shutdown mode, the DAC*x* outputs return to their previous voltage settings.

Figure 13. Serial Data Input Timing Diagram; RSN = 1

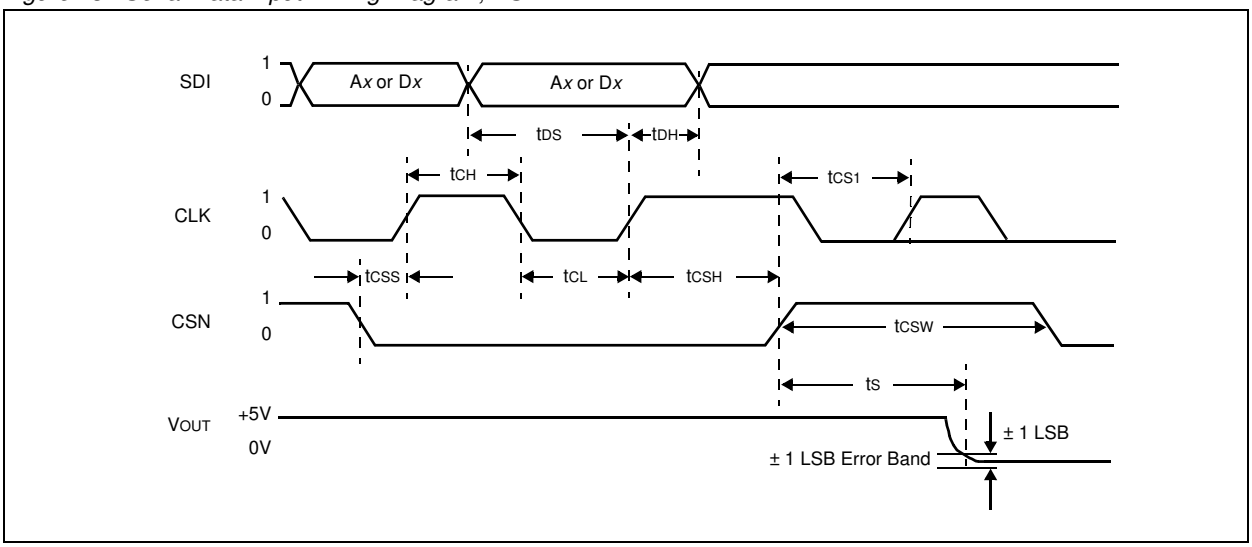


Figure 14. Reset Timing Diagram

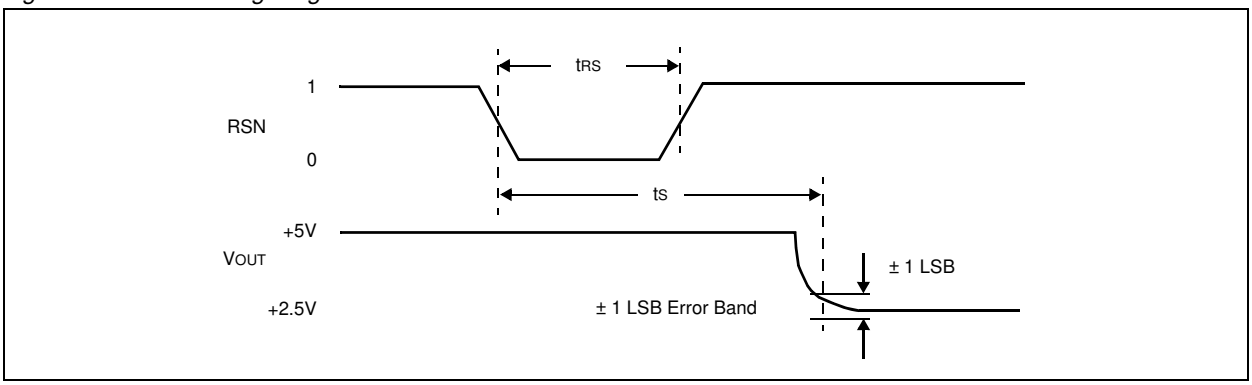
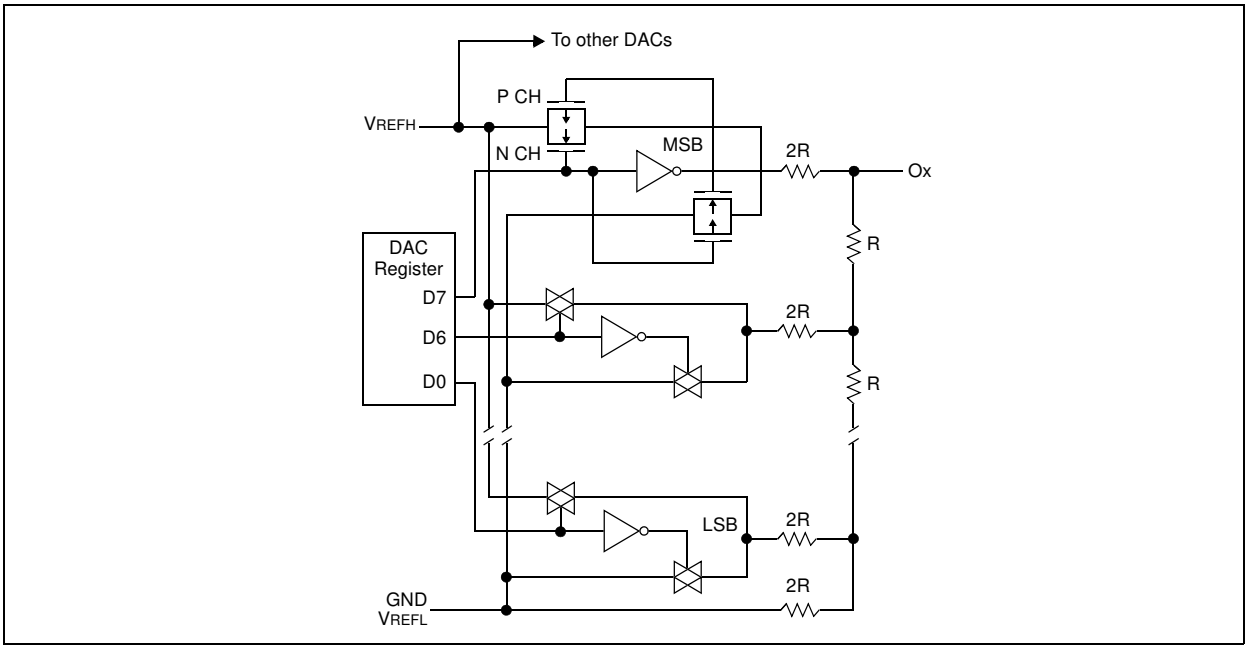


Figure 15. Equivalent DAC Circuit



Programming The Output Voltage

The output voltage range is determined by the external reference connected to pins VREFH and VREFL (see Figure 15 on page 10 for a simplified diagram of the equivalent DAC circuit).

VREFL for the AS1504 is internally connected to GND and therefore cannot be offset. Pin VREFH can be tied to VDD and pin VREFL can be tied to GND establishing a basic rail-to-rail output voltage programming range. Other output ranges are established by the use of different external voltage references.

The programmed output voltage is determined as:

$$V_{OUT}(Dx) = (Dx)/256 \times (V_{REFH} - V_{REFL}) + V_{REFL} \qquad (EQ\ 2)$$

Where:

Dx is the data contained in the 8-bit DAC*x* latch.

For example, when VREFH = +5V and VREFL = 0V the output voltages will be generated per the codes listed in Table 6.

Table 6. Output Voltages

Data Bits	VOUT*x*	Output State (VREFH = +5V, VREFL = 0V)
255	4.98V	Full-Scale
128	2.50V	Half-Scale (Mid-Scale Reset Value)
1	0.02V	1 LSB
0	0.00V	Zero-Scale

Reference Inputs

The reference input pins (VREFH and VREFL) set the output voltage range of all eight DACs. For the AS1504, only pin VREFH is available to establish a programmable full-scale output voltage.

Note: The external reference voltage can be any value between 0 and VDD but must not exceed VDD.

The AS1505 uses pin VREFL to establish the zero-scale output voltage. Any voltage can be applied between 0 and VDD. VREFL can be smaller or larger than VREFH since the DAC design uses fully bi-directional switches as shown in Figure 15. The input resistance to the DAC has a code dependent variation that has a nominal worst case measured at 55_h, which is approximately 2kΩ. When VREFH is greater than VREFL, the REFL reference must be able to sink current out of the DAC ladder, while the REFH reference is sourcing current into the DAC ladder. The DAC design minimizes reference glitch current, thus maintaining minimum interference between DAC channels during code changes.

DAC Outputs

The 8 DAC outputs (OUT1:OUT8) present a constant output resistance of approximately 5kΩ independent of code settings. The distribution of ROUT from DAC to DAC typically matches within ±1%. Device-to-device matching is process-lot dependent with a ±20% variation. The change in ROUT with temperature has a 500 ppm/°C temperature coefficient.

Note: During shutdown the OUT*x* outputs are open-circuited.

Serial Interface

The AS1504/AS1505 are controlled via a standard three-wire serial input. The three input pins are CLK, CSN and SDI.

The positive-edge sensitive CLK input requires a clean transition to avoid clocking spurious data into the serial input register (standard logic families are perfectly adequate). If mechanical switches are used for device evaluation, they should be de-bounced by a flip-flop or other suitable means.

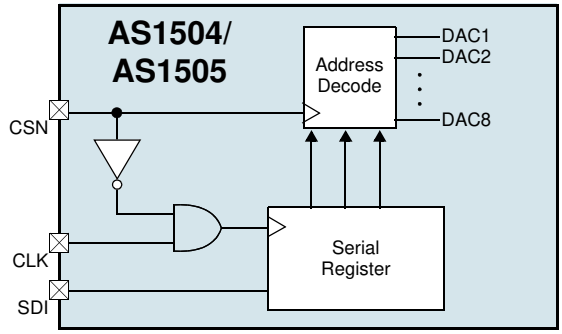
Figure 11 on page 8 shows details of the internal digital circuitry. When CSN is pulled low, the clock can load data into the serial register on each positive clock edge (see Table 7).

Table 7. Function of Pins CSN and CLK

CSN	CLK	Register Activity
1	X	No effect.
0	Positive Edge	Shifts serial register one bit loading the next bit in from the SDI pin.
Positive Edge	X	Data is transferred from the serial register to the decoded DAC register (see Figure 16).

The data setup and data hold times in Table 4 on page 4 determine the valid data time requirements. The last 11 bits of the data word entered into the serial register are held when CSN goes high. When CSN goes high it gates the address decoder which enables one of the eight positive-edge triggered DAC registers (see Figure 16).

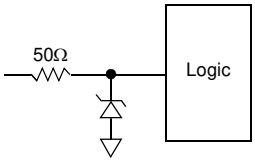
Figure 16. Equivalent Control Logic



The target DAC register is loaded with the last eight bits of the serial data word completing one DAC update. To change all eight output settings, eight separate 11-bit data words must be clocked in to the device.

Note: All digital inputs (CSN, SDI, RSN, SHDNN, and CLK) are protected with the series input resistor and parallel zener diode ESD circuit illustrated in Figure 17.

Figure 17. Equivalent ESD Protection Circuit



Note: Digital inputs can be driven by voltages exceeding VDD thus providing logic level translation from 5V logic when the device is operated from a 3V supply.

9 Application Information

Supply Bypassing

The AS1504/AS1505 require a well-filtered power source. In most applications, the AS1504/AS1505 should be powered directly from the system power supply (+3 to +5V). However, if the logic supply is a switch-mode design, it will probably generate noise in the 20kHz to 1MHz range. Additionally, fast logic gates can generate transients hundred of millivolts in amplitude from wiring resistance and inductance.

The circuit shown in Figure 18 isolates the analog section from any logic switching transients. Even if a separate power supply trace is not available, adequate supply bypassing will reduce supply-line induced errors. Local supply bypassing consisting of a 10µF tantalum electrolytic capacitor in parallel with a 0.1µF ceramic capacitor is recommended (see Figure 19).

Figure 18. Power Supply Traces

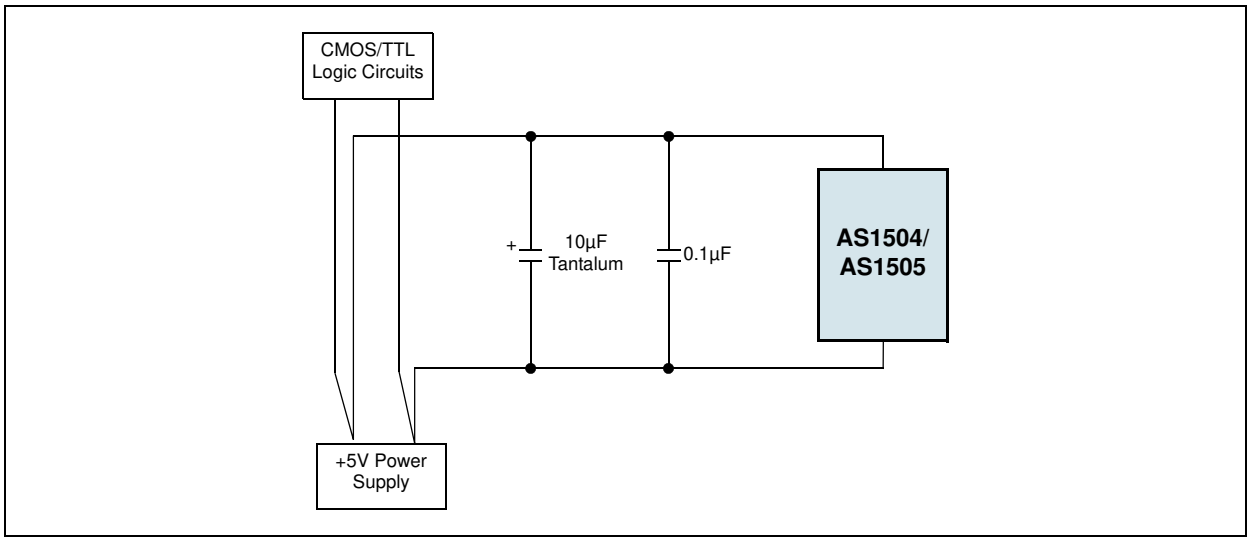
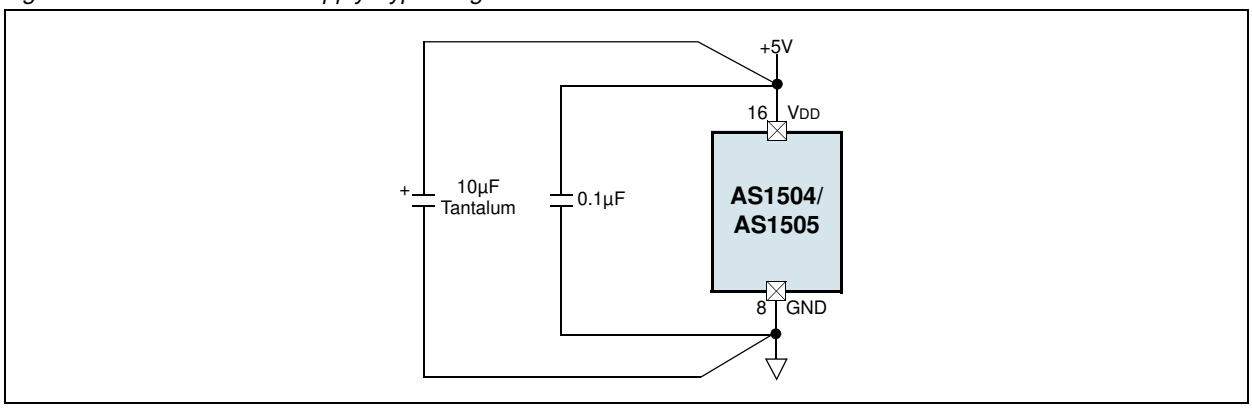


Figure 19. Recommended Supply Bypassing



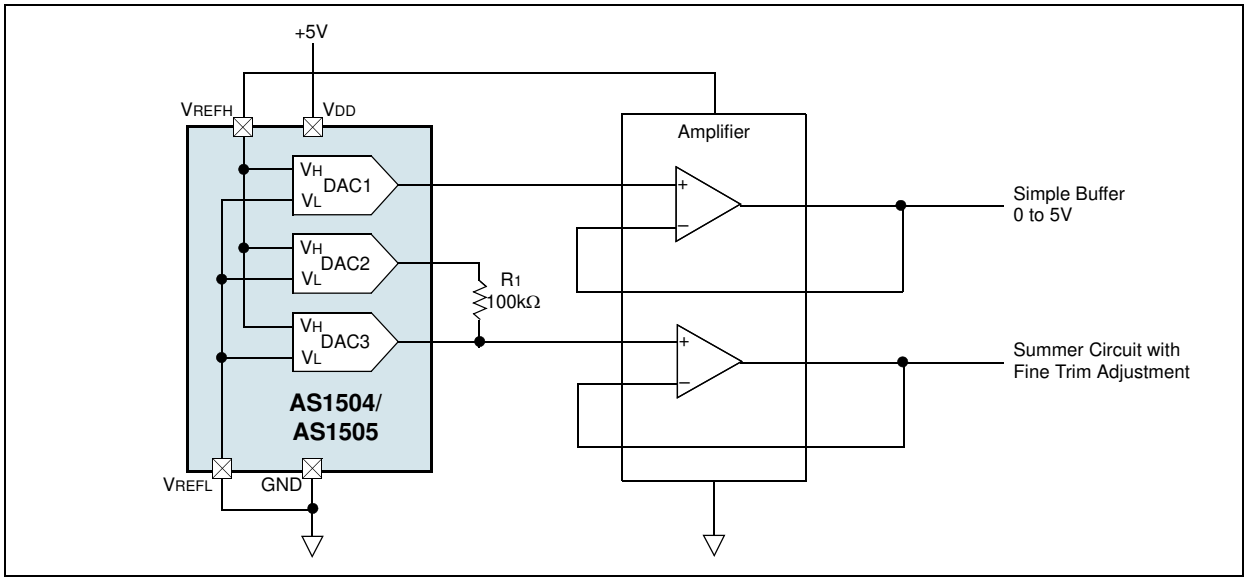
Output Buffering

For most designs, the nominal 5kΩ output impedance of the AS1504/AS1505 is sufficient to drive succeeding circuitry. If a lower output impedance is required, an external amplifier can be added (see Figure 20 on page 13).

A single amplifier should be used as a simple buffer to reduce the output resistance of DAC1. An amplifier with low offset voltage, low supply current, and operation at less than 3V is recommended due to its rail-to-rail input and output operation. DAC2 and DAC3 are configured in a summing arrangement where DAC3 provides the coarse output voltage setting and DAC2 is used for fine adjustments.

The use of R_1 in series with DAC2 (see Figure 20 on page 13)attenuates its contribution to the voltage sum node at the output of DAC3.

Figure 20. Output Buffering



Increasing Output Voltage Swing

An external amplifier can be used to extend the output voltage swing beyond the power supply rails of the AS1504/AS1505. This design allows for a simple digital interface to the DAC, while expanding the output swing to take advantage of higher voltage external power supplies (e.g., DAC 1 of Figure 21 is configured to swing from -5 to +5V). The actual output voltage is given by:

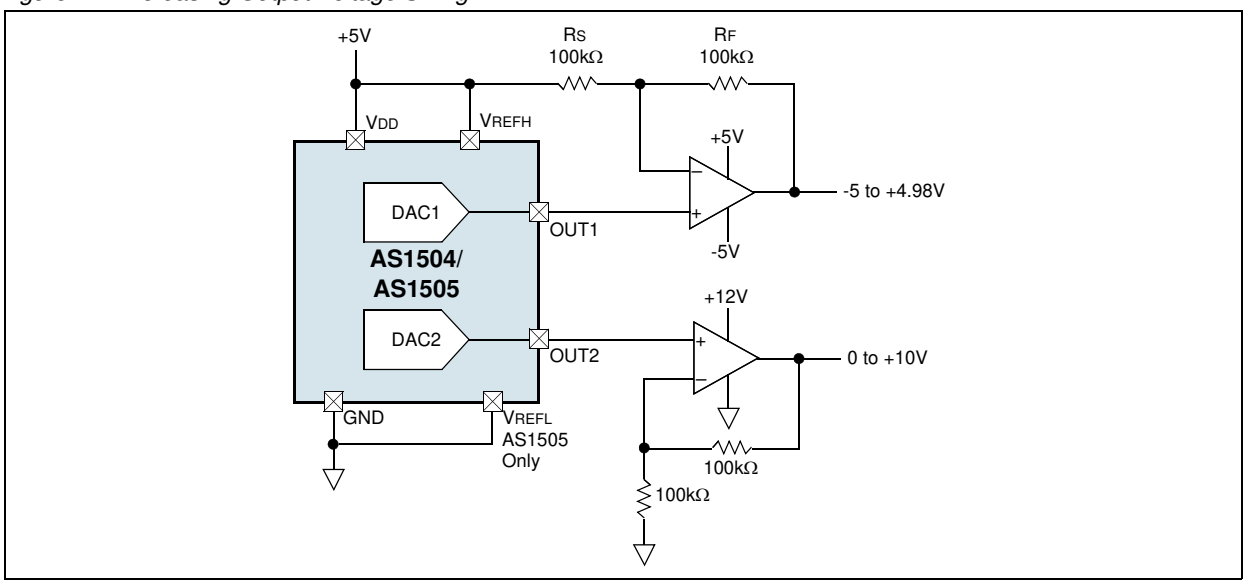
$$V_{OUT} = (1+ (R_F/R_S))((D/256)5V) - 5V \quad \text{(EQ 3)}$$

Where:

D is the DAC input value (i.e., 0 to 255).

This design can be combined with the circuit in Figure 20 if very accurate adjustments around 0V are required.

Figure 21. Increasing Output Voltage Swing



DAC 2 (non-inverting A_V = 2 configuration) of Figure 21 increases the available output swing to +10V. The feedback resistors can be adjusted to provide scaling of the output voltage, within the limits of the external operational amplifier power supplies.

Microprocessor Interfaces

The AS1504/AS1505 serial interface provides a simple connection to a wide range of microprocessors, most of which have built-in serial data capability that can be used for communicating with the device.

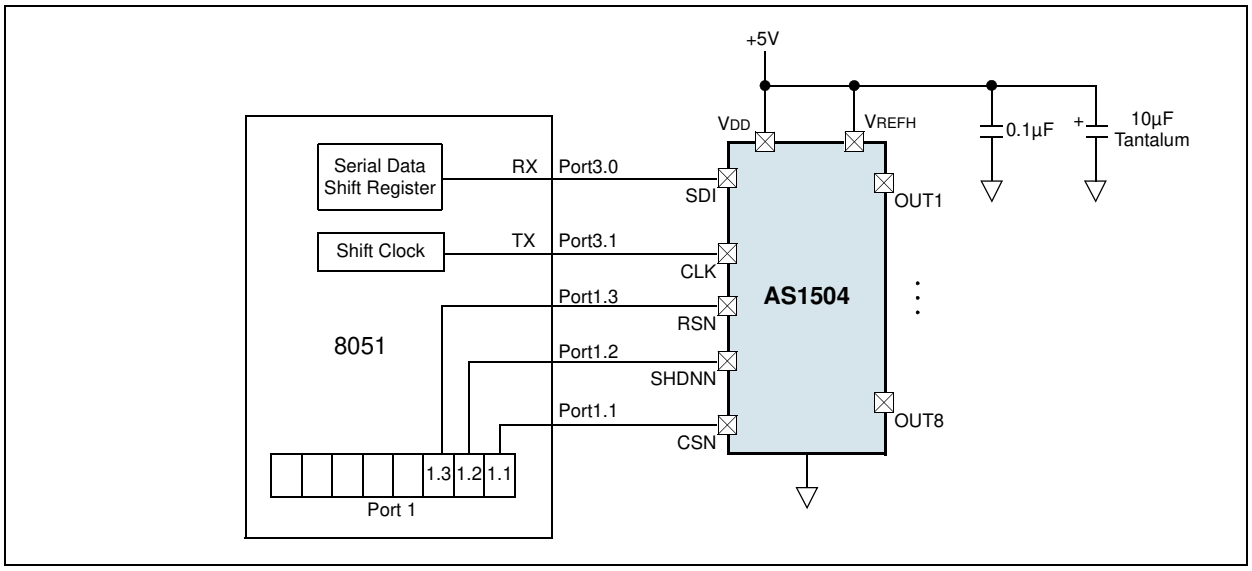
Note: In cases where a serial port is not available on the microprocessor, the AS1504/AS1505 can be addressed via software.

Eleven data bits are required to load data into the AS1504/AS1505 (3 bits for the DAC address and 8 bits for the DAC value). If more than eleven bits are transmitted before the microprocessor chip select input goes high, the most-significant bits are ignored. Because most microprocessors transmit data in 8-bit words, it will need to send 16 bits to the AS1504/AS1505; however, the AS1504/AS1505 only responds to the last 11 bits clocked into the SDI input, so the serial data interface is not affected.

8051 Microprocessor Interface

Figure 22 shows the AS1504/AS1505 interface to an 8051 microprocessor. This interface uses the 8051 internal serial port as a simple 8-bit shift register (Mode 0 operation). 8051 Port3.0 serves as the serial data output port and Port3.1 serves as the serial clock.

Figure 22. AS1504-to-8051 Microprocessor Interface



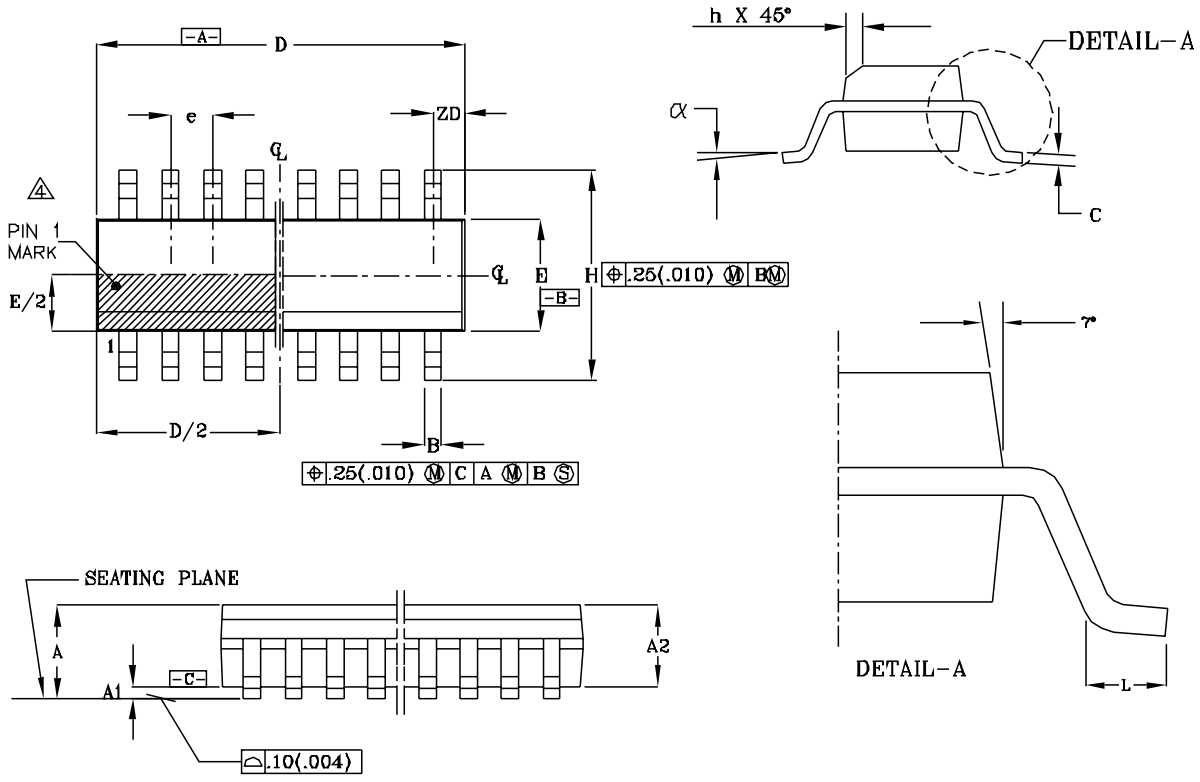
As data is written to the serial buffer register (SBUF, at Special Function Register location 99_h), the data is automatically converted to serial format and clocked out via Port3.0 and Port3.1. Once 8 bits have been transmitted, the transmit interrupt flag (SCON.1) is set and the next 8 bits can be transmitted.

The AS1504/AS1505 requires that CSN goes low at the start of the serial data transfer. Additionally, pin CLK must be high when CSN goes high at the end of each data transfer. The 8051 serial clock meets these requirements, since Port3.1 begins and ends the serial data transfer in a high state.

10 Package Drawings and Markings

The AS1504/AS1505 is available in a 16-pin SOIC-150 package.

Figure 23. 16-pin SOIC-150 Package



Notes:

1. Lead coplanarity should be 0 to 0.10mm (.004") max.
2. Package surface finishing:
   - Top, matte (charmilles #18-30)
   - All sides, matte (charmilles +18-30)
   - Bottom, smooth or matte (charmilles +18-30)
3. All dimensions excluding mold flashes and end flash from the package body shall not exceed 0.25mm (.010") per side.
4. Details of pin #1 mark are optional but must be located within the area indicated.

Symbol	Min	Max
A	1.52	1.72
A1	0.10	0.25
A2	1.37	1.57
B	0.36	0.46
C	0.19	0.25
D	9.80	9.98
E	3.81	3.99
e	1.27BSC	
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
α	0º	8º
ZD	0.51 REF	

11 Ordering Information

The devices are available as the standard products shown in Table 8.

Table 8. Ordering Information

Model	Description	Delivery Form	Package
AS1504-T	Octal 8-Bit DAC, Mid-Scale Reset	Tape and Reel	16-pin SOIC-150 Narrow
AS1505-T	Octal 8-Bit DAC, Separate V_{REFL} Range Settings	Tape and Reel	16-pin SOIC-150 Narrow

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