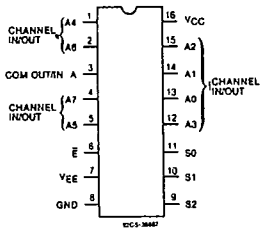


CD54/74HC4051, CD54/74HCT4051
CD54/74HC4052, CD54/74HCT4052
CD54/74HC4053, CD54/74HCT4053

File Number 1676

High-Speed CMOS Logic

HARRIS SEMICOND SECTOR 27E D ■ 4302271 0017921 2 ■ HAS



CD54/74HC/HCT4051
 TERMINAL ASSIGNMENT

**Analog Multiplexers/
 Demultiplexers**

Type Features:

- Wide analog input voltage range: ± 5 V max.
- Low "on" resistance:
 70 Ω typ ($V_{CC}-V_{EE} = 4.5$ V)
 40 Ω typ ($V_{CC}-V_{EE} = 9$ V)
- Low crosstalk between switches
- Fast switching and propagation speeds
- "Break-before-make" switching

The RCA CD54/74HC/HCT4051, 4052, and 4053 are digitally controlled analog switches which utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These analog multiplexers/demultiplexers control analog voltages that may vary across the voltage supply range (i.e. V_{CC} to V_{EE}). They are bidirectional switches thus allowing any analog input to be used as an output and visa-versa. The switches have low "on" resistance and low "off" leakages. In addition, all three devices have an enable control which when, high, disables all switches to their "off" state.

The CD54HC/HCT4051, 4052, and 4053 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT 4051, 4052, and 4053 are supplied in 16-lead plastic packages (E suffix) and in 16-lead surface mount plastic packages (M suffix). All devices are also available in chip form (H suffix).

Family Features:

- Wide Operating Temperature Range:
 CD74HC/HCT: -40 to +85°C
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:
 2 to 6 V Operation, control; 0 to 10 V, switch
 High Noise Immunity:
 $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} ; @ $V_{CC} = 5$ V
- CD54HCT/CD74HCT Types:
 4.5 to 5.5 V Operation, control; 0 to 10 V, switch
 Direct LSTTL Input Logic Compatibility
 $V_{IL} = 0.8$ V Max., $V_{IH} = 2$ V Min.
 CMOS Input Compatibility
 $I_i \leq 1 \mu A$ @ V_{OL} , V_{OH}

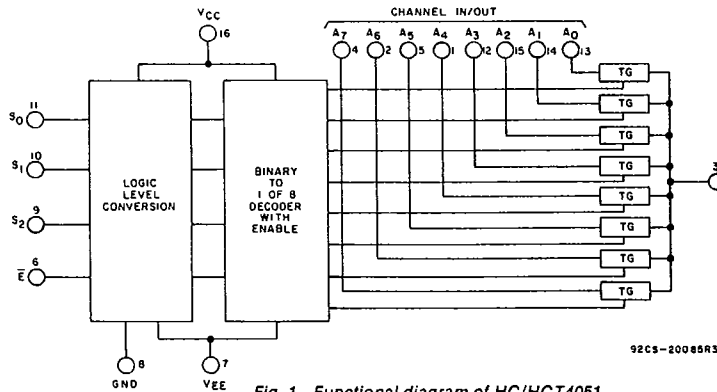


Fig. 1 - Functional diagram of HC/HCT4051.

TRUTH TABLE
 CD54/74HC/HCT4051

| INPUT STATES | | | | "ON" CHANNELS |
|--------------|----|----|----|---------------|
| ENABLE | S2 | S1 | S0 | |
| L | L | L | L | A0 |
| L | L | L | H | A1 |
| L | L | H | L | A2 |
| L | L | H | H | A3 |
| L | H | L | L | A4 |
| L | H | L | H | A5 |
| L | H | H | L | A6 |
| L | H | H | H | A7 |
| H | X | X | X | NONE |

X = Don't Care

**CD54/74HC4051, CD54/74HCT4051
CD54/74HC4052, CD54/74HCT4052
CD54/74HC4053, CD54/74HCT4053**

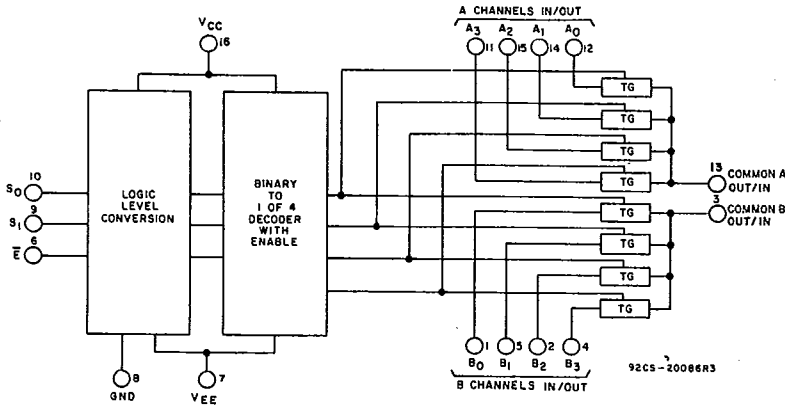
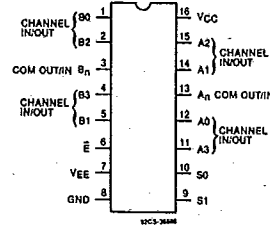


Fig. 2 - Functional diagram of HC/HCT4052.



**CD54/74HC/HCT4052
TERMINAL ASSIGNMENT**

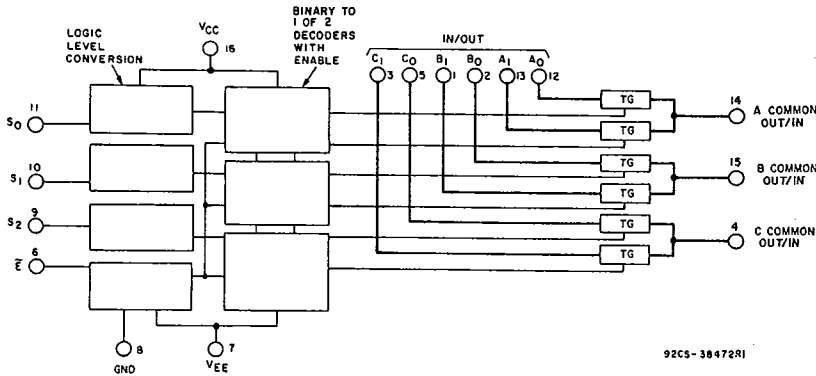
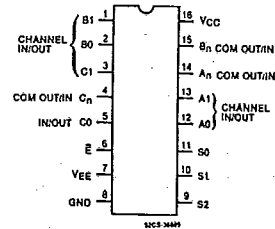


Fig. 3 - Functional diagram of HC/HCT4053.



**CD54/74HC/HCT4053
TERMINAL ASSIGNMENT**

TRUTH TABLES (Continued)

CD54/74HC/HCT4052

| INPUT STATES | | | "ON" CHANNELS |
|--------------|----|----|---------------|
| ENABLE | S1 | S0 | |
| L | L | L | A0, B0 |
| L | L | H | A1, B1 |
| L | H | L | A2, B2 |
| L | H | H | A3, B3 |
| H | X | X | NONE |

X = Don't Care

CD54/74HC/HCT4053

| INPUT STATES | | | | "ON" CHANNELS |
|--------------|----|----|----|---------------|
| ENABLE | S2 | S1 | S0 | |
| L | L | L | L | A0 B0 C0 |
| L | L | L | H | A0 B0 C1 |
| L | L | H | L | A0 B1 C0 |
| L | L | H | H | A0 B1 C1 |
| L | H | L | L | A1 B0 C0 |
| L | H | L | H | A1 B0 C1 |
| L | H | H | L | A1 B1 C0 |
| L | H | H | H | A1 B1 C1 |
| H | X | X | X | NONE |

X = Don't Care

T-51-12

CD54/74HC4051, CD54/74HCT4051
CD54/74HC4052, CD54/74HCT4052
CD54/74HC4053, CD54/74HCT4053

MAXIMUM RATINGS, Absolute-Maximum Values: (All voltages referenced to Gnd unless otherwise shown)

| | | |
|--|-------|---|
| DC SUPPLY-VOLTAGE ($V_{CC}-V_{EE}$) | | -0.5 to 10.5 V |
| DC SUPPLY-VOLTAGE (V_{CC}) | | -0.5 to +7 V |
| DC SUPPLY-VOLTAGE (V_{EE}) | | +0.5 to -7 V |
| DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V) | | ± 20 mA |
| DC SWITCH DIODE CURRENT, I_{OK} (FOR $V_i < V_{EE} - 0.5$ V OR $V_i > V_{CC} + 0.5$ V) | | ± 20 mA |
| DC SWITCH CURRENT (FOR $V_i > V_{EE} - 0.5$ V OR $V_i < V_{CC} + 0.5$ V) | | +25 mA |
| DC V_{CC} OR GROUND CURRENT (I_{CC}) | | ± 50 mA |
| DC V_{EE} CURRENT (I_{EE}) | | -20 mA |
| POWER DISSIPATION PER PACKAGE (P_D): | | |
| For $T_A = -40$ to $+60^\circ$ C (PACKAGE TYPE E) | | 500 mW |
| For $T_A = +60$ to $+85^\circ$ C (PACKAGE TYPE E) | | Derate Linearly at 8 mW/ $^\circ$ C to 300 mW |
| For $T_A = -55$ to $+100^\circ$ C (PACKAGE TYPE F, H) | | 500 mW |
| For $T_A = +100$ to $+125^\circ$ C (PACKAGE TYPE F, H) | | Derate Linearly at 8 mW/ $^\circ$ C to 300 mW |
| For $T_A = -40$ to $+70^\circ$ C (PACKAGE TYPE M) | | 400 mW |
| For $T_A = +70$ to $+125^\circ$ C (PACKAGE TYPE M) | | Derate Linearly at 6 mW/ $^\circ$ C to 70 mW |
| OPERATING-TEMPERATURE RANGE (T_A): | | |
| PACKAGE TYPE F, H | | -55 to $+125^\circ$ C |
| PACKAGE TYPE E, M | | -40 to $+85^\circ$ C |
| STORAGE TEMPERATURE (T_{stg}) | | -65 to $+150^\circ$ C |
| LEAD TEMPERATURE (DURING SOLDERING): | | |
| At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max. | | $+265^\circ$ C |
| Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm) with solder contacting lead tips only | | $+300^\circ$ C |

- In certain applications, the external load-resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6 volt (calculated from R_{ON} values shown in Electrical Characteristics chart). No V_{CC} current will flow through R_L if the switch current flows into terminal 3 on the HC/HCT4051; terminals 3 and 13 on the HC/HCT4052; terminals 4, 14 and 15 on the HC/HCT4053.

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | LIMITS | | UNITS |
|---|------------|----------|------------|
| | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range) V_{CC} .* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | V |
| Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range) $V_{CC}-V_{EE}$ | | | |
| CD54/74HC Types | 2 | 10 | V |
| CD54/74HCT Types | See Fig. 4 | | |
| Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range) V_{EE} .* | | | |
| CD54/74HC Types | 0 | -6 | V |
| CD54/74HCT Types | See Fig. 5 | | |
| DC Input Control Voltage, V_i | Gnd | V_{CC} | V |
| Analog Switch I/O Voltage, V_{is} | V_{EE} | V_{CC} | V |
| Operating Temperature T_A : | | | |
| CD74 Types | -40 | +85 | $^\circ$ C |
| CD54 Types | -55 | +125 | $^\circ$ C |
| Input Rise and Fall Times t_r, t_f | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | ns |
| at 6 V | 0 | 400 | ns |

*Unless otherwise specified, all voltages are referenced to Ground.

Recommended Operating Area as a Function of Supply Voltages.

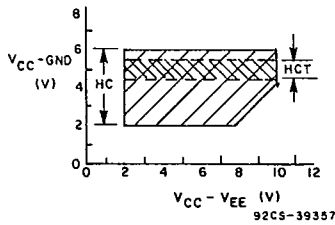


Fig. 4

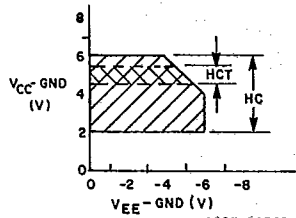


Fig. 5

HARRIS SEMICONDUCTOR SECTOR 27E D 430227J 0017923 6 HAS

**CD54/74HC4051, CD54/74HCT4051
CD54/74HC4052, CD54/74HCT4052
CD54/74HC4053, CD54/74HCT4053**

STATIC ELECTRICAL CHARACTERISTICS

| CHAR- ACTERISTIC | CD74HC/CD54HC4051,4052,4053 | | | | | | | | | | CD74HCT/CD54HCT4051,4052,4053 | | | | | | | | | | UNITS | | | | | | | | | |
|---|--|----------------------------|----------|----------|-----------------|------|-----|---------------|-----------|------|-------------------------------|------|---------|------------------|------------------|----------|----------|-------------------|-----|------|-----------|---------------|---------|-----------|----------------|---------|----------|---|---------|---------|
| | TEST CONDITIONS | | | | 74HC/54HC TYPES | | | 74HC TYPES | | | 54HC TYPES | | | TEST CONDITIONS | | | | 74HCT/54HCT TYPES | | | | 74HCT TYPES | | | 54HCT TYPES | | | | | |
| | V_{IS} | V_I | V_{EE} | V_{CC} | +25°C | | | -40/ +85°C | | | -55/ +125°C | | | V_{IS} | V_I | V_{EE} | V_{CC} | +25°C | | | | -40/ +85°C | | | -55/ +125°C | | | | | |
| | V | V | V | V | Min | Typ | Max | Min | Max | Min | Max | Min | Max | V | V | V | V | Min | Typ | Max | | Min | Max | Min | Max | Min | Max | | | |
| High-Level Input Voltage V_{IH} | | | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | | | | | 4.5 | | | | | | | | | V | | | | |
| | | | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | | | | to | 2 | — | — | 2 | — | 2 | — | | | | | | |
| | | | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | 5.5 | | | | | | | | | | | | | |
| Low-Level Input Voltage V_{IL} | | | | | 2 | — | — | 0.5 | — | 0.5 | — | 0.5 | | | | | 4.5 | | | | | | | | | V | | | | |
| | | | | | 4.5 | — | — | 1.35 | — | 1.35 | — | 1.35 | | | | | to | — | — | 0.8 | — | 0.8 | — | 0.8 | — | | | | | |
| | | | | | 6 | — | — | 1.8 | — | 1.8 | — | 1.8 | | | | | 5.5 | | | | | | | | | | | | | |
| "On" Resistance R_{ON} $I_O = 1 \text{ mA}$ (Fig. 15) | V_{CC} or V_{EE} | V_{IL} or V_{EH} | | | 0 | 4.5 | — | 70 | 160 | — | 200 | — | 240 | Same as HC | Same as HC | | | 0 | 4.5 | — | 70 | 160 | — | 200 | — | 240 | Ω | | | |
| | | | | | 0 | 6 | — | 60 | 140 | — | 175 | — | 210 | | | | | | | | | | | | | | | | | |
| | | | | | -4.5 | 4.5 | — | 40 | 120 | — | 150 | — | 180 | | | | | | | -4.5 | 4.5 | — | 40 | 120 | — | 150 | | — | 180 | |
| | V_{CC} to V_{EE} | | | | 0 | 4.5 | — | 80 | 180 | — | 225 | — | 270 | | | | | | | 0 | 4.5 | — | 90 | 180 | — | 225 | | — | 270 | |
| | | | | | 0 | 6 | — | 80 | 160 | — | 200 | — | 240 | | | | | | | 0 | 4.5 | — | 80 | 160 | — | 200 | | — | 240 | |
| | | | | | -4.5 | 4.5 | — | 45 | 130 | — | 162 | — | 195 | | | | | | | -4.5 | 4.5 | — | 45 | 130 | — | 162 | | — | 195 | |
| Maximum "On" Resistance between any two channels ΔR_{ON} | | | | | 0 | 4.5 | — | 10 | — | — | — | — | — | | | | | | | 0 | 4.5 | — | 10 | — | — | — | | — | | |
| | | | | | 0 | 6 | — | 8.5 | — | — | — | — | — | | | | | | | 0 | 4.5 | — | 10 | — | — | — | | — | | |
| | | | | | -4.5 | 4.5 | — | 5 | — | — | — | — | — | | | | | | | -4.5 | 4.5 | — | 5 | — | — | — | | — | | |
| Switch On/Off Leakage Current I_{LZ} 1&2 Channels (4053) 4 Channels (4052) 8 Channels (4051) | For Switch OFF: When $V_{IS} = V_{CC}$ $V_{OE} = V_{EE}$: When $V_{IS} = V_{EE}$ $V_{OE} = V_{CC}$ For Switch ON: All Applicable Combinations of V_{IS} & V_{OE} Voltage Levels | V_{IL} or V_{EH} | | | 0 | 6 | — | — | ± 0.1 | — | ± 1 | — | ± 1 | | | | | | | 0 | 6 | — | — | ± 0.1 | — | ± 1 | | — | ± 1 | μA |
| | | | | | -5 | 5 | — | — | ± 0.1 | — | ± 1 | — | ± 1 | | | | | | | -5 | 5 | — | — | ± 0.1 | — | ± 1 | | — | ± 1 | |
| | | | | | 0 | 6 | — | — | ± 0.1 | — | ± 1 | — | ± 1 | | | | | | | 0 | 6 | — | — | ± 0.1 | — | ± 1 | | — | ± 1 | |
| | | | | | -5 | 5 | — | — | ± 0.2 | — | ± 2 | — | ± 2 | | | | | -5 | 5 | — | — | ± 0.2 | — | ± 2 | — | ± 2 | | | | |
| | | | | | 0 | 6 | — | — | ± 0.2 | — | ± 2 | — | ± 2 | | | | | 0 | 6 | — | — | ± 0.2 | — | ± 2 | — | ± 2 | | | | |
| | | | | | -5 | 5 | — | — | ± 0.4 | — | ± 4 | — | ± 4 | | | | | -5 | 5 | — | — | ± 0.4 | — | ± 4 | — | ± 4 | | | | |
| Control Input Leakage Current I_{LZ} | — | V_{CC} or Gnd | | | 0 | 6 | — | — | ± 0.1 | — | ± 1 | — | ± 1 | | | | | 5.5 | — | — | ± 0.1 | — | ± 1 | — | ± 1 | μA | | | | |
| Quiescent Device Current I_{CC} $I_O = 0$ | When $V_{IS} = V_{EE}$, $V_{OE} = V_{CC}$: When $V_{IS} = V_{CC}$, $V_{OE} = V_{EE}$ | V_{CC} or Gnd | | | 0 | 6 | — | — | 8 | — | 80 | — | 160 | Same as HC | Same as HC | | | 0 | 5.5 | — | — | 8 | — | 80 | — | 160 | μA | | | |
| | | | | | -5 | 5 | — | — | 16 | — | 160 | — | 320 | | | | | | | -4.5 | 5.5 | — | — | 16 | — | 160 | | — | 320 | |
| Additional Quiescent Device Current per input pin, 1 unit load ΔI_{CC}^* | | | | | | | | | | | | | | | | | | | | | | | | | | μA | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

* For dual-supply systems theoretical worst case ($V_I = 2.4 \text{ V}$, $V_{CC} = 5.5 \text{ V}$) specifications is 1.8 mA.

** Any voltage between V_{CC} & Gnd.

HCT Input Loading Table

| Type | Input | Unit Loads* |
|------------|-------|-------------|
| 4051, 4053 | All | 0.5 |
| 4052 | All | 0.4 |

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

HARRIS SEMICONDUCTOR 27E D 430227J 0017924 8 HAS

T-51-12

CD54/74HC4051, CD54/74HCT4051
CD54/74HC4052, CD54/74HCT4052
CD54/74HC4053, CD54/74HCT4053

HARRIS SEMICONDUCTOR

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 6\text{ ns}$)

| CHARACTERISTIC | SYMBOL | C_L pF | Typical | | | | | | UNITS |
|-----------------------------------|--------------------|-------------|---------|-----|------|-----|------|-----|-------|
| | | | 4051 | | 4052 | | 4053 | | |
| | | | HC | HCT | HC | HCT | HC | HCT | |
| Propagation Delay | t_{PHL} | 15 | 4 | 4 | 4 | 4 | 4 | 4 | ns |
| Switch IN to OUT | t_{PLH} | | | | | | | | |
| Switch Turn-off (S or \bar{E}) | t_{PHZ}, t_{PLZ} | 15 | 19 | 19 | 21 | 21 | 18 | 18 | ns |
| Switch Turn-on (S or \bar{E}) | t_{PZH}, t_{PZL} | 15 | 19 | 23 | 27 | 29 | 18 | 20 | ns |
| Power Dissipation Capacitance* | C_{PD} | — | 50 | 52 | 74 | 76 | 38 | 42 | pF |

* C_{PD} is used to determine the dynamic power consumption, per package.
 $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L + C_S) V_{CC}^2 f_o$
 f_o = output frequency
 f_i = input frequency.
 C_L = output load capacitance.
 C_S = switch capacitance
 V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS ($C_L = 50\text{ pF}$, Input $t_r, t_f = 6\text{ ns}$)

| CHARACTERISTIC | SYMBOL | V_{EE} | V_{CC} | 25°C | | | | -40°C to +85°C | | | | -55°C to +125°C | | | | UNITS | |
|--|-----------|------------------------|----------|------|------|------|------|----------------|------|-------|------|-----------------|------|-------|------|-------|-----|
| | | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | | |
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Propagation Delay, Switch In to Out | t_{PLH} | 0 | 2 | — | 60 | — | — | — | 75 | — | — | — | 90 | — | — | ns | |
| | | 0 | 4.5 | — | 12 | — | 12 | — | 15 | — | 15 | — | 18 | — | 18 | | |
| | | 0 | 6 | — | 10 | — | — | — | 13 | — | — | — | 15 | — | — | | |
| | | -4.5 | 4.5 | — | 8 | — | 8 | — | 10 | — | 10 | — | 12 | — | 12 | | |
| Maximum Switch Turn "Off" Delay from S or \bar{E} to Switch Output | 4051 | 0 | 2 | — | 225 | — | — | — | 280 | — | — | — | 340 | — | — | ns | |
| | | 0 | 4.5 | — | 45 | — | 45 | — | 56 | — | 56 | — | 68 | — | 68 | | |
| | | 0 | 6 | — | 38 | — | — | — | 48 | — | — | — | 57 | — | — | | |
| | | -4.5 | 4.5 | — | 32 | — | 32 | — | 40 | — | 40 | — | 48 | — | 48 | | |
| | 4052 | t_{PHZ} t_{PLZ} | 0 | 2 | — | 250 | — | — | — | 315 | — | — | — | 375 | — | | — |
| | | | 0 | 4.5 | — | 50 | — | 50 | — | 63 | — | 63 | — | 75 | — | | 75 |
| | | | 0 | 6 | — | 43 | — | — | — | 54 | — | — | — | 65 | — | | — |
| | | | -4.5 | 4.5 | — | 38 | — | 38 | — | 48 | — | 48 | — | 57 | — | | 57 |
| | 4053 | t_{PHZ} t_{PLZ} | 0 | 2 | — | 210 | — | — | — | 265 | — | — | — | 315 | — | | — |
| | | | 0 | 4.5 | — | 42 | — | 44 | — | 53 | — | 55 | — | 63 | — | | 66 |
| | | | 0 | 6 | — | 36 | — | — | — | 45 | — | — | — | 54 | — | | — |
| | | | -4.5 | 4.5 | — | 29 | — | 31 | — | 36 | — | 39 | — | 44 | — | | 47 |
| Maximum Switch Turn "On" Delay from S or \bar{E} to Switch Output | 4051 | 0 | 2 | — | 225 | — | — | — | 280 | — | — | — | 340 | — | — | ns | |
| | | 0 | 4.5 | — | 45 | — | 55 | — | 56 | — | 69 | — | 68 | — | 83 | | |
| | | 0 | 6 | — | 38 | — | — | — | 48 | — | — | — | 57 | — | — | | |
| | | -4.5 | 4.5 | — | 32 | — | 39 | — | 40 | — | 49 | — | 48 | — | 59 | | |
| | 4052 | t_{PZH} t_{PZL} | 0 | 2 | — | 325 | — | — | — | 405 | — | — | — | 490 | — | | — |
| | | | 0 | 4.5 | — | 65 | — | 70 | — | 81 | — | 68 | — | 98 | — | | 105 |
| | | | 0 | 6 | — | 55 | — | — | — | 69 | — | — | — | 83 | — | | — |
| | | | -4.5 | 4.5 | — | 46 | — | 48 | — | 58 | — | 60 | — | 69 | — | | 72 |
| | 4053 | t_{PZH} t_{PZL} | 0 | 2 | — | 220 | — | — | — | 275 | — | — | — | 330 | — | | — |
| | | | 0 | 4.5 | — | 44 | — | 48 | — | 55 | — | 60 | — | 66 | — | | 72 |
| | | | 0 | 6 | — | 37 | — | — | — | 47 | — | — | — | 56 | — | | — |
| | | | -4.5 | 4.5 | — | 31 | — | 34 | — | 39 | — | 43 | — | 47 | — | | 51 |
| Input (Control) Capacitance | C_i | — | — | — | 10 | — | 10 | — | 10 | — | 10 | — | 10 | pF | | | |

CD54/74HC4051, CD54/74HCT4051
CD54/74HC4052, CD54/74HCT4052
CD54/74HC4053, CD54/74HCT4053

ANALOG CHANNEL CHARACTERISTICS — TYPICAL VALUES AT $T_A = 25^\circ\text{C}$

| CHARACTERISTIC | SYMBOL | CONDITIONS | TYPES | V_{EE} (V) | V_{CC} (V) | HC/HCT | UNITS |
|---|-----------|---------------------------|-------|--------------|--------------|--------|-------|
| Switch Input Capacitance | C_i | | All | | | 5 | pF |
| Common Capacitance | C_{COM} | | 4051 | | | 25 | |
| | | | 4052 | | | 12 | |
| | | | 4053 | | | 8 | |
| Minimum Switch Frequency Response @ -3 dB Figs. 11, 13, 15 | f_{MAX} | See Fig. 6 Notes 1, 2 | 4051 | -2.25 | 2.25 | 145 | MHz |
| | | | 4052 | | | 165 | |
| | | | 4053 | | | 200 | |
| | | | 4051 | -4.5 | 4.5 | 180 | |
| | | | 4052 | | | 185 | |
| | | | 4053 | | | >200 | |
| Crosstalk Between Any Two Switches Note 4 | | See Fig. 7 Notes 2, 3 | 4051 | -2.25 | 2.25 | N/A | dB |
| | | | 4052 | | | (TBE) | |
| | | | 4053 | | | (TBE) | |
| | | | 4051 | -4.5 | 4.5 | N/A | |
| | | | 4052 | | | (TBE) | |
| | | | 4053 | | | (TBE) | |
| Sine-Wave Distortion | | See Fig. 8 | All | -2.25 | 2.25 | 0.035 | % |
| | | | All | -4.5 | 4.5 | 0.018 | |
| E or S to Switch Feedthrough Noise | | See Fig. 9 Notes 2, 3 | 4051 | -2.25 | 2.25 | (TBE) | mV |
| | | | 4052 | | | (TBE) | |
| | | | 4053 | | | (TBE) | |
| | | | 4051 | -4.5 | 4.5 | (TBE) | |
| | | | 4052 | | | (TBE) | |
| | | | 4053 | | | (TBE) | |
| Switch "OFF" Signal Feedthrough Figs. 12, 14, 16 | | See Fig. 10 Notes 2, 3 | 4051 | -2.25 | 2.25 | -73 | dB |
| | | | 4052 | | | -65 | |
| | | | 4053 | | | -64 | |
| | | | 4051 | -4.5 | 4.5 | -75 | |
| | | | 4052 | | | -67 | |
| | | | 4053 | | | -66 | |

Notes:

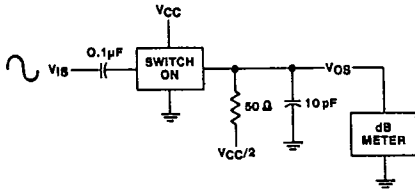
1. Adjust input voltage to obtain OdBm @ V_{OS} for $f_{in} = 1$ MHz.
2. V_{IS} is centered at $(V_{CC} - V_{EE})/2$.
3. Adjust input for OdBm.
4. Not applicable for HC/HCT4051.

CD54/74HC4051, CD54/74HCT4051
CD54/74HC4052, CD54/74HCT4052
CD54/74HC4053, CD54/74HCT4053

T-51-12

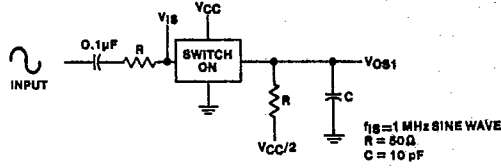
HARRIS SEMICOND SECTOR

27E D ■ 430227J 0017927 3 ■ HAS



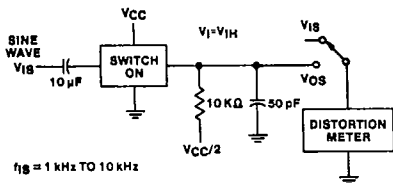
92CS-39354

Fig. 6 - Frequency response test circuit.



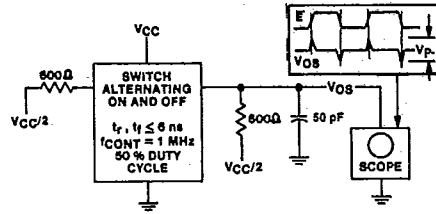
92CS-39355

Fig. 7 - Crosstalk between two switches test circuit.



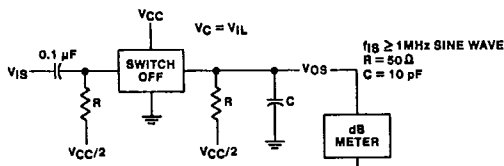
92CS-39356R1

Fig. 8 - Sine wave distortion test circuit.



92CS-39352

Fig. 9 - Control-to-switch feedthrough noise test circuit.



92CS-39353

Fig. 10 - Switch off signal feedthrough.

CD54/74HC4051, CD54/74HCT4051 CD54/74HC4052, CD54/74HCT4052 CD54/74HC4053, CD54/74HCT4053

430227J 0017928 5 HAS

27E D

HARRIS SEMICONDUCTOR

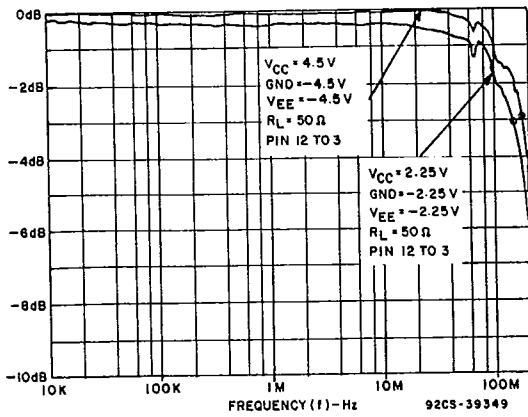


Fig. 11 - Channel on bandwidth (HC/HCT4051).

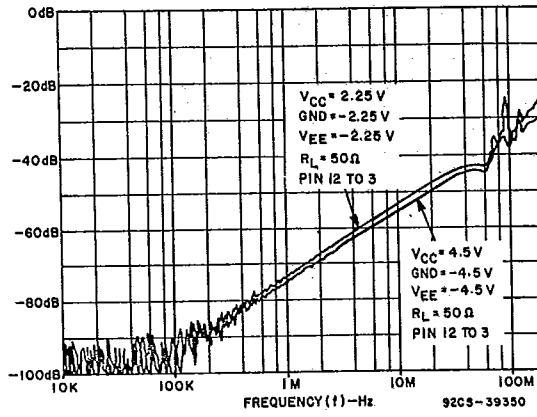


Fig. 12 - Channel off feedthrough (HC/HCT4051).

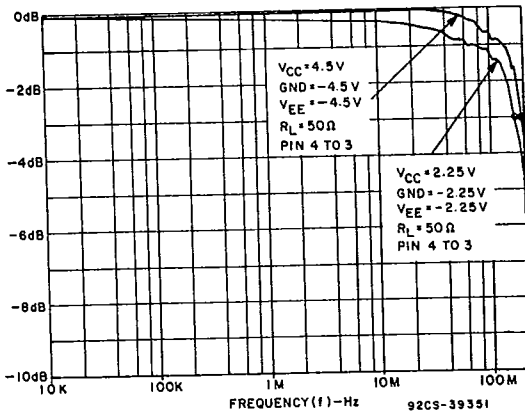


Fig. 13 - Channel on bandwidth (HC/HCT4052).

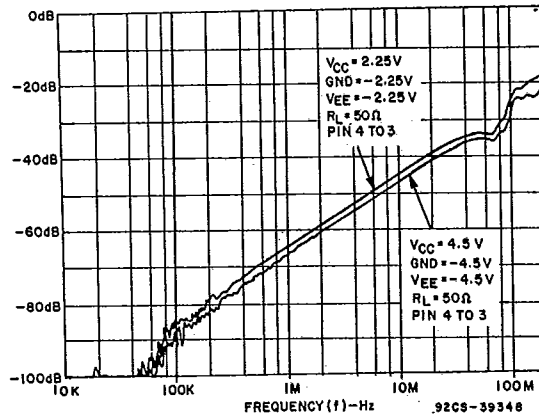


Fig. 14 - Channel off feedthrough (HC/HCT4052).

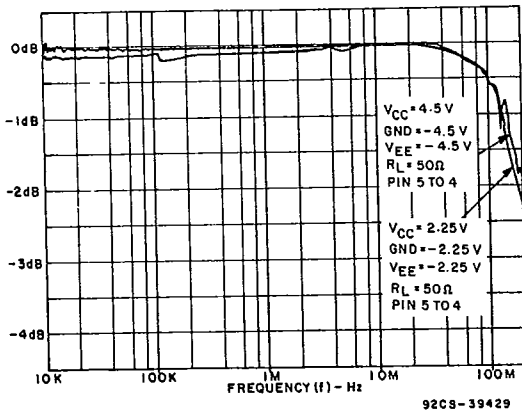


Fig. 15 - Channel on bandwidth (HC/HCT4053).

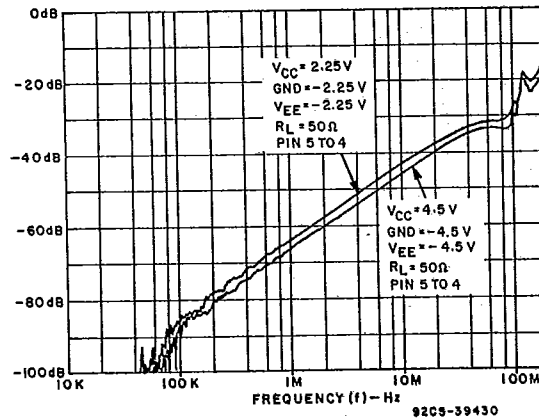


Fig. 16 - Channel off feedthrough (HC/HCT4053).

T-51-12

CD54/74HC4051, CD54/74HCT4051
CD54/74HC4052, CD54/74HCT4052
CD54/74HC4053, CD54/74HCT4053

HARRIS SEMICONDUCTOR SECTOR 27E D 4302271 0017929 7 HAS

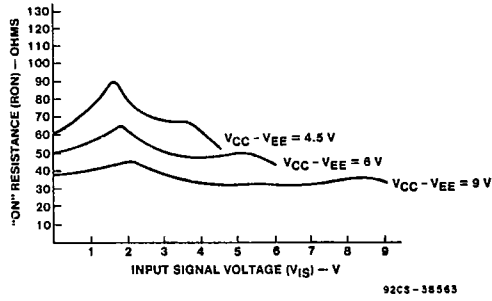


Fig. 17 - Typical ON resistance vs. input signal voltage.

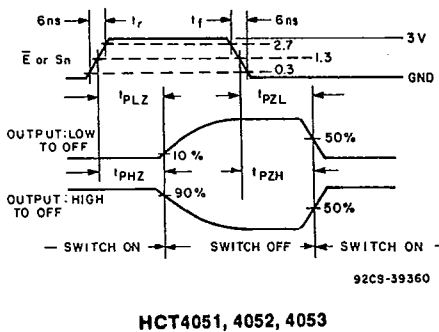
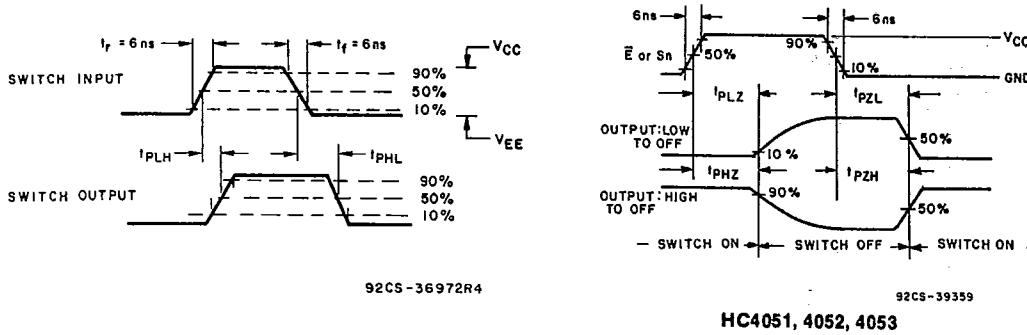


Fig. 18 - Switch propagation delay, turn-on, turn-off times.

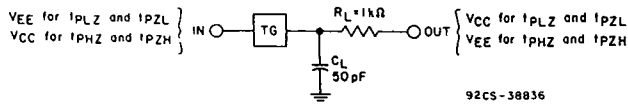


Fig. 19 - Switch on/off propagation delay test circuit.

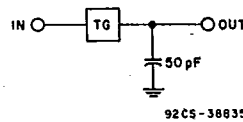


Fig. 20 - Switch In to Switch Out Propagation delay test circuit.