TOSHIBA Field Effect Transistor Silicon P Channel MOS Type(U-MOS VI)

SSM6P47NU

Power Management Switch Applications

• 1.5V drive

• Low ON-resistance: $R_{DS(on)}$ = 242 m Ω (max) (@V_{GS} = -1.5 V)

 $R_{\mathrm{DS}(on)}$ = 170 m Ω (max) (@V_{GS} = -1.8 V)

 $R_{DS(on)}$ = 125 m Ω (max) (@V_{GS} = -2.5 V)

 $R_{DS(on)} = 95 \text{ m}\Omega \text{ (max) } (@V_{GS} = -4.5 \text{ V})$

Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

Charac	teristics	Symbol	Rating	Unit	
Drain-Source voltage		V_{DSS}	-20	V	
Gate-Source voltage		V_{GSS}	±8	V	
Drain current	DC	I _D	-4.0	Α	
	Pulse	I _{DP} (Note 1)	-8.0	A	
Power dissipation (Note 2)		PD	P _D 1 W		
Fower dissipation (Note 2)		t < 10s			
Channel temperature		Tch	150	°C	
Storage temperature		T _{stg}	-55 to 125	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Unit: mm

2.0±0.1

B A

1. Source1 4. Source2
2. Gate1 5. Gate2
3. Drain2 6. Drain1

UDFN6

JEDEC

JEITA

TOSHIBA

2-2Y1A

Weight: 8.5 mg (typ.)

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

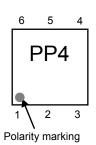
Note 1: The channel temperature should not exceed 150 °C during use.

Note 2: Total rating

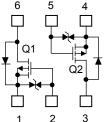
Mounted on an FR4 board.

 $(25.4 \text{ mm} \times 25.4 \text{ mm} \times 1.6 \text{ mm}, \text{ Cu Pad: } 645 \text{ mm}^2)$

Marking(Top View)

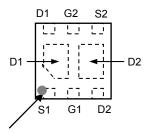


6 5 4 P P P



Equivalent Circuit(Top View)

Pin Condition(Top View)



Polarity marking (on the top)
*Electrodes : on the bottom

Start of commercial production 2010-06

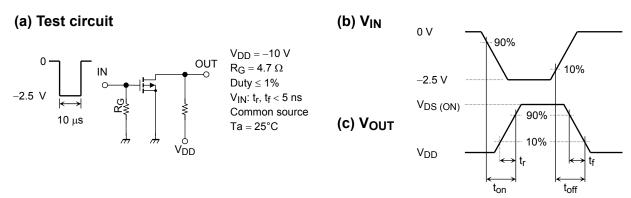
Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

Chara	cteristic	Symbol	Test Conditions		Min	Тур.	Max	Unit
Drain-Source breakdown voltage		V (BR) DSS	$I_D = -1 \text{ mA}, V_{GS} = 0 \text{ V}$ -20		-20	_	_	V
		V (BR) DSX	$I_D = -1 \text{ mA}, V_{GS} = 5 \text{ V}$ ((Note 4)	-15	_	_	v
Drain cut-off current		I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V		_	_	-1	μА
Gate leakage current		I _{GSS}	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$		_	_	±1	μΑ
Gate threshold voltage		V _{th}	$V_{DS} = -3 \text{ V}, I_{D} = -1 \text{ mA}$		-0.3	_	-1.0	V
Forward transfer admittance		Y _{fs}	$V_{DS} = -3 \text{ V}, I_{D} = -1.0 \text{ A}$ ((Note 3)	2.8	5.6	_	S
Drain–source ON-resistance		R _{DS} (ON)	$I_D = -1.5 \text{ A}, V_{GS} = -4.5 \text{ V}$ ((Note 3)	_	80.5	95	mΩ
			$I_D = -1.0 \text{ A}, V_{GS} = -2.5 \text{ V}$ ((Note 3)	_	99.5	125	
			$I_D = -0.5 \text{ A}, V_{GS} = -1.8 \text{ V}$ ((Note 3)	_	122	170	
			$I_D = -0.25 \text{ A}, V_{GS} = -1.5 \text{ V}$ ((Note 3)	_	143	242	
Input capacitance		C _{iss}			_	290	_	
Output capacitance		Coss	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		_	44	_	pF
Reverse transfer capacitance		C _{rss}		_	32	_		
Total Gate Charge		Qg			_	4.6	_	nC
Gate-Source Charge		Q _{gs1}	$V_{DD} = -10 \text{ V}, I_D = -3.5 \text{ A}$ $V_{GS} = -4.5 \text{ V}$		_	0.5	_	
Gate-Drain Charge		Q _{gd}	VG5 4.0 V		_	1.2	_	
Switching time	Turn-on time	t _{on}	V _{DD} = -10 V, I _D = -0.5 A,		_	12.0		20
	Turn-off time	t _{off}	V_{GS} = 0 to -2.5 V, R_{G} = 4.7 Ω		_	46.2	_	ns
Drain-Source forward voltage		V _{DSF}	$I_D = 4.0 \text{ A}, V_{GS} = 0 \text{ V}$ ((Note 3)	_	0.9	1.2	٧

Note 3: Pulse test

Note 4: If a forward bias is applied between gate and source, this device enters V(BR)DSX mode. Note that the drain-source breakdown voltage is lowered in this mode.

Switching Time Test Circuit



Notice on Usage

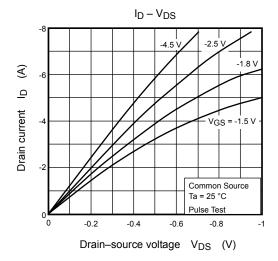
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (-1 mA for the SSM6P47NU). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$. Take this into consideration when using the device.

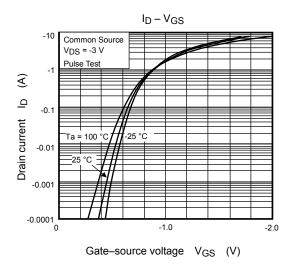
Handling Precaution

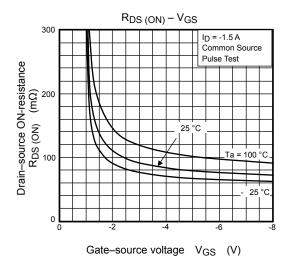
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

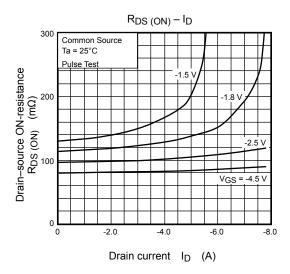
Thermal resistance R_{th} (ch-a) and power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration.

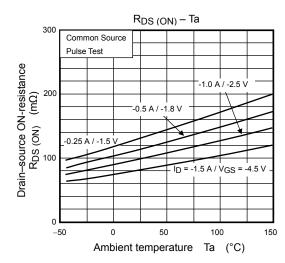
(Q1, Q2 Common)

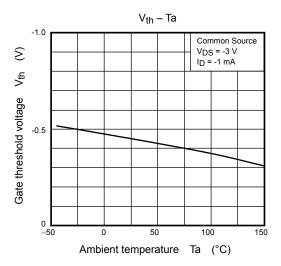






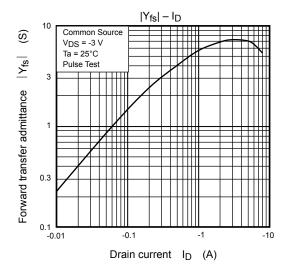


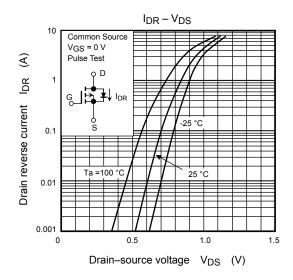


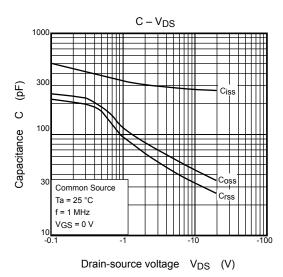


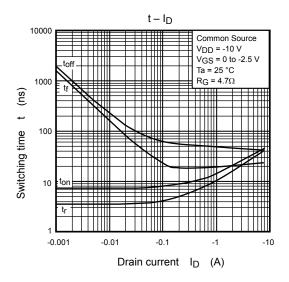
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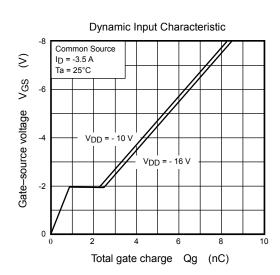
(Q1, Q2 Common)



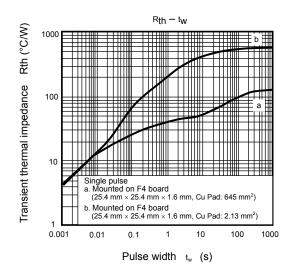


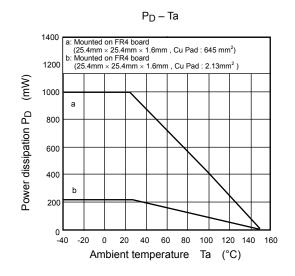






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