

74ACT18825 18-Bit Buffer/Line Driver with 3-STATE Outputs

General Description

The ACT18825 contains eighteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is byte controlled. Each byte has separate 3-STATE control inputs which can be shorted together for full 18-bit operation.

Features

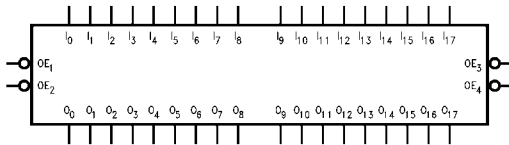
- Broadside pinout allows for easy board layout
- Separate control logic for each byte
- Extra data width for wider address/data paths or buses carrying parity
- Outputs source/sink 24 mA
- TTL-compatible inputs

Ordering Code:

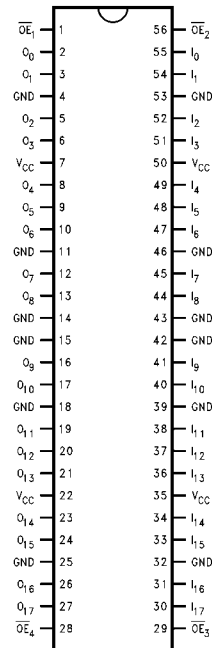
Order Number	Package Number	Package Description
74ACT18825SSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ACT18825MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active LOW)
I_0-I_{17}	Inputs
O_0-O_{17}	Outputs

Functional Description

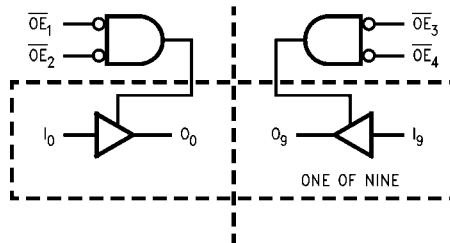
The ACT18825 contains eighteen non-inverting buffers with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independently of the other. The control pins may be shorted together to obtain full 8-bit operation. The 3-STATE outputs are controlled by an Output Enable (\overline{OE}_n) input for each byte. When \overline{OE}_n is LOW, the outputs are in 2-state mode. When \overline{OE}_n is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Truth Table

Inputs				Outputs			
Byte 1 (0:8)		Byte 2 (8:17)		I_0-I_8	I_9-I_{17}	O_0-O_8	O_9-O_{17}
\overline{OE}_1	\overline{OE}_2	\overline{OE}_3	\overline{OE}_4				
L	L	L	L	H	H	H	H
H	X	L	L	X	L	Z	L
X	H	L	L	X	H	Z	H
L	L	H	X	L	X	L	Z
L	L	X	H	H	X	H	Z
H	H	H	H	X	X	Z	Z
L	L	L	L	L	L	L	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = HIGH Impedance

Logic Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source/Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
Per Output Pin	±50 mA
Storage Temperature	-65°C to +150°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum HIGH Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	1.5	2.0	2.0			
V_{IL}	Maximum LOW Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	1.5	0.8	0.8			
V_{OH}	Minimum HIGH Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ (Note 2)	
		5.5		4.86	4.76			
V_{OL}	Maximum LOW Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ (Note 2)	
		5.5		0.36	0.44			
I_{OZ}	Maximum 3-STATE Leakage Current	5.5		±0.5	±5.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, \text{GND}$	
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}, \text{GND}$	
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$	
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	μA	$V_{IN} = V_{CC}$ or GND	
I_{OLD}	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V \text{ Max}$	
I_{OHD}	Output Current (Note 3)				-75	mA	$V_{OHD} = 3.85V \text{ Min}$	

Note 2: All outputs loaded; thresholds associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

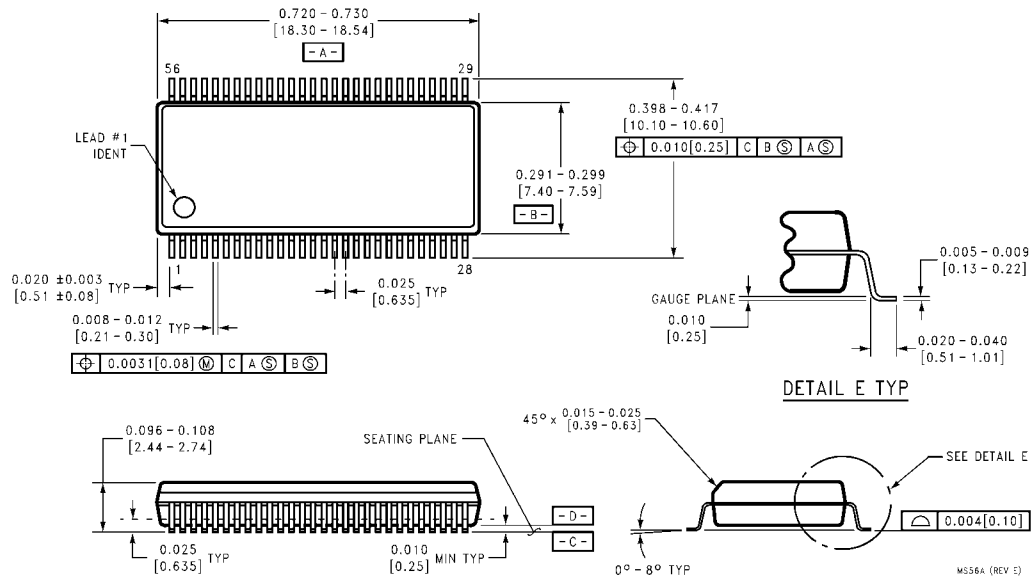
Symbol	Parameter	V _{CC} (V) (Note 4)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t _{PHL}	Propagation Delay	5.0	2.0	5.3	8.4	2.0	9.0	ns
t _{PLH}	Data to Output		2.0	5.6	8.7	2.0	9.2	
t _{PZL}	Output Enable	5.0	2.0	6.3	9.6	2.0	10.3	ns
t _{PZH}	Time		2.0	6.5	9.7	2.0	10.4	
t _{PLZ}	Output Disable	5.0	1.5	4.5	7.3	1.5	7.6	ns
t _{PHZ}	Time		1.5	5.1	8.5	1.5	8.8	

Note 4: Voltage Range 5.0 is 5.0V ± 0.5V.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Pin Capacitance	4.5	pF	V _{CC} = 5.0V
C _{PD}	Power Dissipation Capacitance	95	pF	V _{CC} = 5.0V

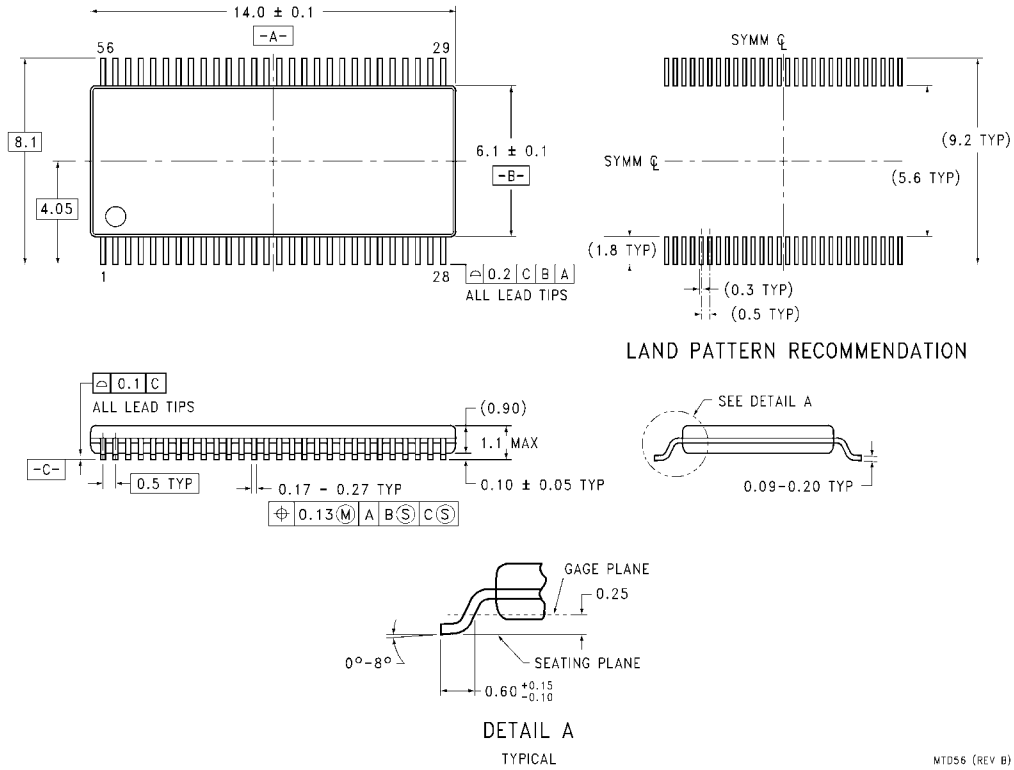
Physical Dimensions inches (millimeters) unless otherwise noted



**56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS56A**

MS56A (REV 5)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56**

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