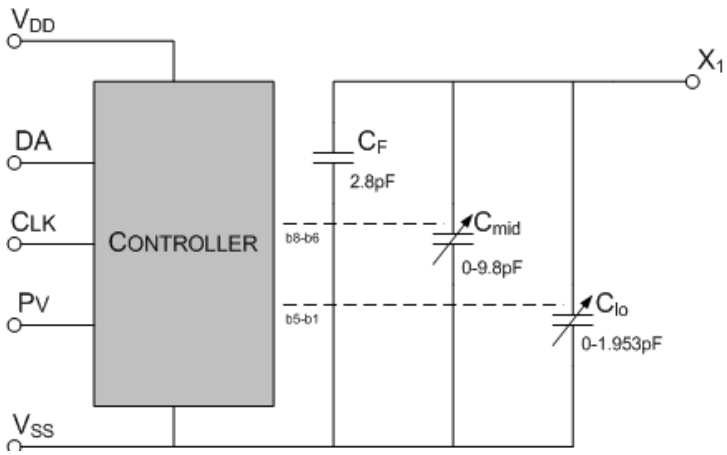
Programmable Capacitive Tuning IC

SON8, MLP6

FEATURES

- Capacitive Tuning Range of 6.6pF to 37.553pF
- 0.063pF Minimum Step Size
- Continually Programmable with Register or EEPROM Data Storage
- May Be Placed in Parallel for Greater Capacitance Values
- 2.5V to 5.0V Supply Voltage
- RoHS compliant Pb Free Packages

BLOCK DIAGRAM



DESCRIPTION

The CTST571 is a digitally programmed capacitor designed to tune a filter or crystal/SAW based oscillator to a desired center frequency. Through a bank of registers, the capacitance value is set by a serial data stream and if desired, can be permanently stored in the nonvolatile EEPROM memory. The CTST571 is designed to be a labor and cost saving device within the oscillator production process and provide the desired functionality for tunable filter banks.

While incorporating very small step sizes (0.063pF), multiple CTST571 devices can also be used in parallel to obtain higher overall capacitance values.

The CTST571 is available in an SON8 package (1.5mm x 1.0mm) for very small form factor designs. Also available in MLP6.

ENGINEERING NOTES

Capacitor Structure

The CTST571 capacitance value is composed of four parallel capacitors banks, CF is a fixed capacitor value of 6.6pF and C_{HI}, C_{MID} and C_{LO} are variable capacitors of differing ranges and resolutions as seen in Table 1. Capacitors composing C_{HI}, C_{MID} and C_{LO} are set with a binary control word through an 11-bit shift register described in “Programming the CTST571” section. The values of each C_{HI}, C_{MID} and C_{LO} stepping are detailed in the complete Nominal Capacitance Binary Mapping spreadsheet.

$$C_{TOTAL} = C_F + C_{HI} + C_{MID} + C_{LO}$$

Table 1 – Capacitor Structure

Internal Capacitor	Min Value (pF)	Max Value (pF)	Step Size (pF)
C_F	6.6	6.6	n/a
C_{HI}	0	19.2	6.4
C_{MID}	0	9.8	1.4
C_{LO}	0	1.953	0.063
Total	6.6	37.553	

CTST571 Functional Mode

The CTST571 has two methods for setting the capacitance value on the X_1 pin.

- **Reading the Control Word Directly From the Shift Register**
  In tunable filter applications, reading from the shift register will be desirable as the control word can be constantly varied. New control words can be serially inputted as required to change the capacitance value in real time. (Note: With a serial data input, the capacitance value during transitions between control words is deterministic upon their differences.) The shift register is also useful for testing the capacitance and subsequent oscillator frequency. *This mode is active when the CLK pin is left logic high. For the shift register, capacitors are selected when bits are active HIGH.*

- **Reading the Control Word From the Value Contained in the EEPROM**
  If a certain control word needs to be stored, it can be written to the nonvolatile EEPROM memory. This is useful in oscillator applications where it prevents customer adjustment and retains factory programming. *This mode is active when the CLK pin is at logic low or not connected. For the EEPROM, capacitors are selected when bits are active LOW.*

Oscillator Application

In oscillator applications, the CTST571 is designed to be used in 2 modes, Programming and Operational.

In the *Programming mode*, the CTST571 is used by the manufacturer to set the capacitance value to control the desired center frequency of the oscillator. The programming phase gives the manufacturer access to pins DA, CLK, and PV where the shift registers are used to first determine the required control word. That control word is then stored in the EEPROM memory. CTS can provide this board (CTS10EL89) along with software that works through all the programming steps/functions described in the next sections (Figure 1).

In the *Operational mode*, the EEPROM internal to the CTST571 has already been programmed with the desired factory settings. Pins DA, CLK, and PV are to be disconnected, thereby allowing the CTST571's internal pull-downs to place the pins at ground potential. In the operational mode, only 3 pins are necessary for hookup (Figure 2).

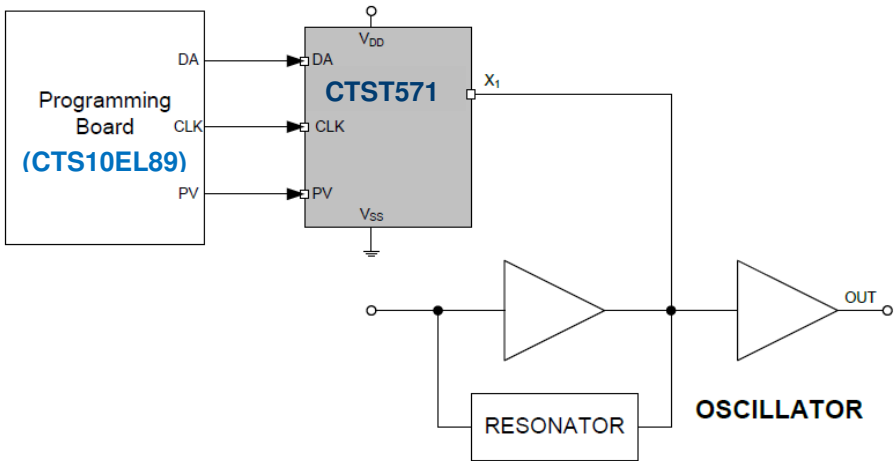


Figure 1 – CTST571 in Programming Mode

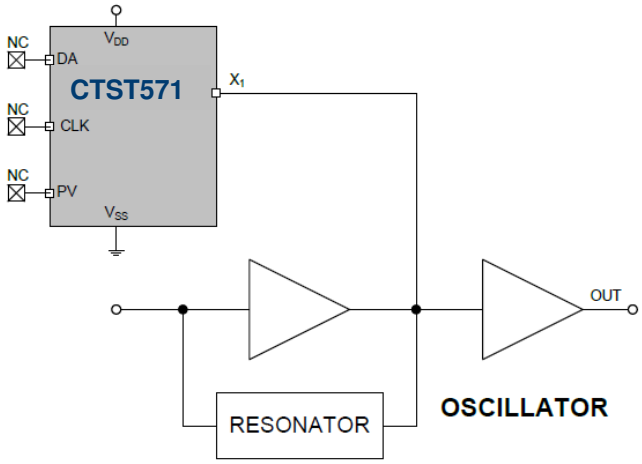


Figure 2 – CTST571 in Operational Mode

Programing the CTST570

Control Word

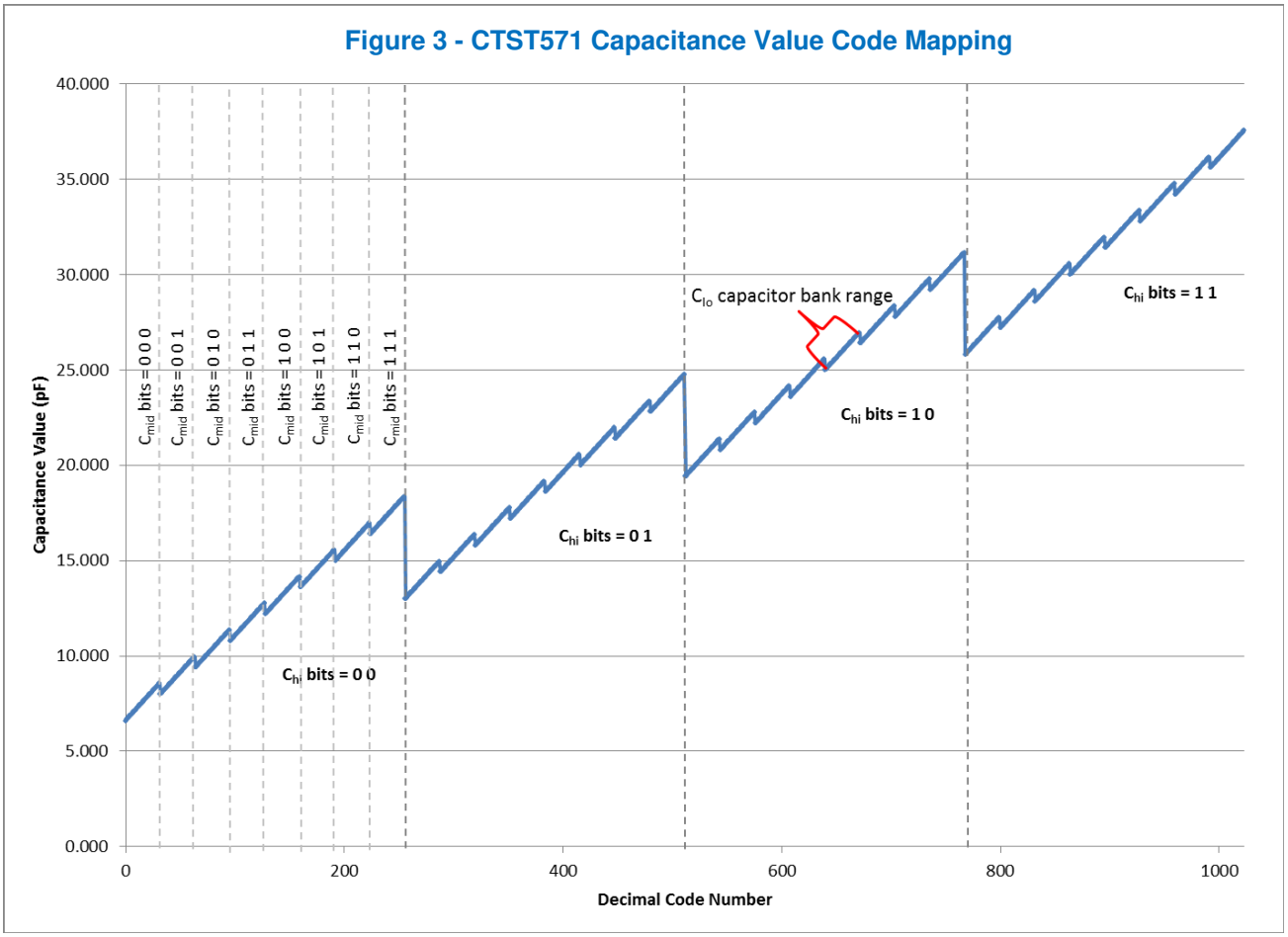
The capacitance in the CTST571 is controlled by an 11-bit shift register with the data input bit definitions shown in Table 2. The control word data is inputted serially on the rising edge of the CLK signal with bit-0 first and bit-10 last.

Table 2 – CTST571 Control Word Definition

11-bit Control Word										
bit-10	bit-9	bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
C_{HI}		C_{MID}			C_{LO}					Not Used
MSB	LSB	MSB	---	LSB	MSB	---	---	---	LSB	

The control word mapping is a binary word for each of C_{HI}, C_{MID} and C_{LO} where higher number bits are more significant. Figure 3 shows the capacitance value mapping for the CTST571. The detailed Nominal Capacitance Binary Mapping can be located on the CTS website.

Figure 3 - CTST571 Capacitance Value Code Mapping



Programming from the Shift Register

Control word bits are inputted serially through the DA pin timed with the rising edge of the CLK pin. Figure 4 shows the control word 11001100100 has been serially entered into the register. Note that bit-0 is the 1st bit to enter and bit-10 is the last. In the CTST571, bit-0 does not affect the capacitance value but still must be included in the serial bit stream. For the shift register, capacitors are selected when bits are active HIGH. For the CTST571 to read from the shift register, the CLK pin must remain HIGH.

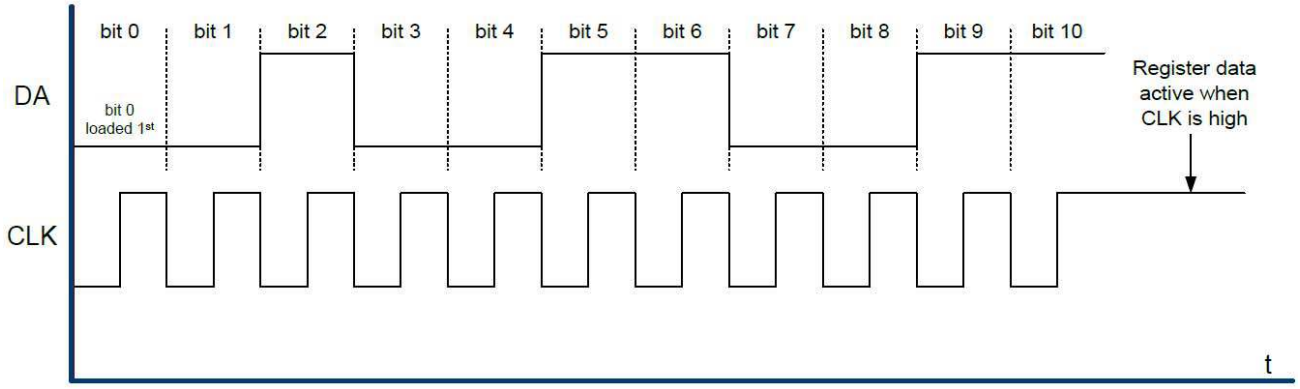


Figure 4 – Shift Register Programming

Writing Data to the EEPROM

Once the desired capacitance value has been determined, the digital control word can be written or re-written into the EEPROM. By storing the control word in the EEPROM, the customer is prevented from making adjustments from the factory set programming data. This is accomplished within the CTST571 with internal pull-downs on the DA, PV, and CLK pins. The detailed sequence for writing data to the EEPROM within the CTST571 is described in Table 5. Note that with EEPROM, capacitors are selected when bits are active LOW.

Table 3 – Data Writing Sequence for EEPROM

Step	Action
1	Determine the desired capacitor control word with the operational power supply voltage and desired oscillator conditions.
2	Set the V_{DD} supply voltage to +5.0V.
3	If EEPROM is not already erased, erase EEPROM (see “Erasing the EEPROM” section).
4	Read the current state of the EEPROM bits (see “Reading Back from the EEPROM” section).
5	Compare the desired control word to the stored EEPROM control word. Count the number of differences so as to prevent double/redundant writing.
6	One bit at a time, load the first desired control word bit (bit selection for EEPROM is active LOW).
7	Set the PV pin to +6V (≥5.6V, ≤6.1V) with the pulse and idle shown in timing diagram (Figure 7).
8	Progress through all necessary control word bits by repeating steps 5 & 6 until all bits are set to the desired control word.
9	Verify the correct EEPROM contents by reading back the individual bits.

For an example of writing bits into the EEPROM, suppose the desired capacitance is 3.43pF. The control word becomes '00000010100' (Figure 5). Also suppose the EEPROM bits have been erased and therefore logic high (The CTST571 is initially shipped in this condition). Since bit-0 is the first bit to be loaded, the bit sequence becomes 0-0-1-0-1-0-0-0-0-0-0. However, as described before, selecting bits for the EEPROM are active LOW, which will invert the logical values in the sequence to 1-1-0-1-0-1-1-1-1-1-1 (Figure 6). Note the differences between the EEPROM bits and the converted control word. Since there are 2 differences, two write cycles are required as only 1 bit should be written at a time. Figure 7 shows the timing for bit-2 while Figure 8 shows the timing for bit-4.

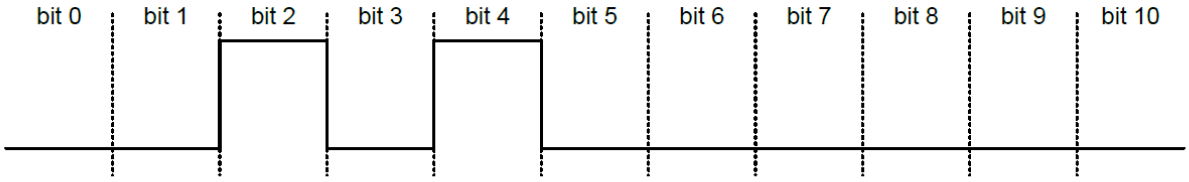


Figure 5 – Desired Control Word

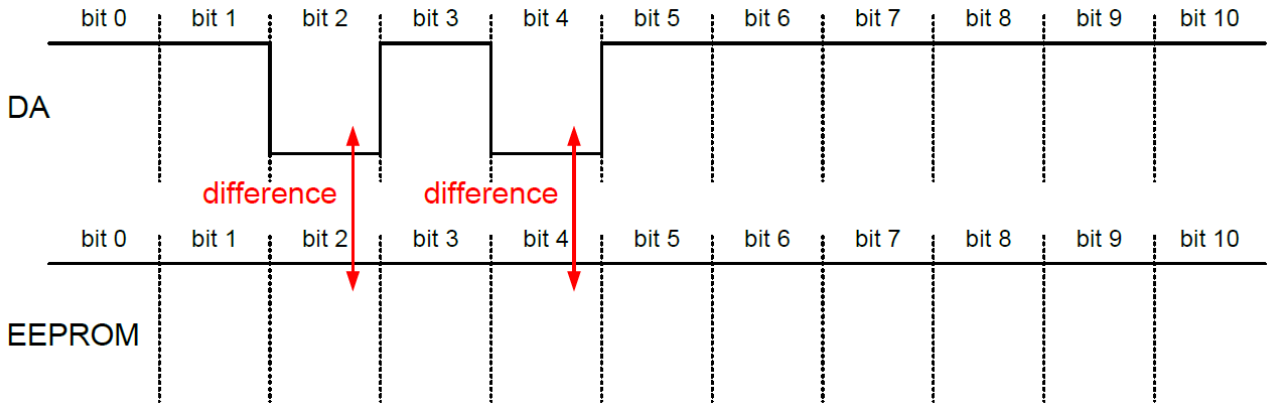


Figure 6 – Converted control word and differences from known EEPROM states

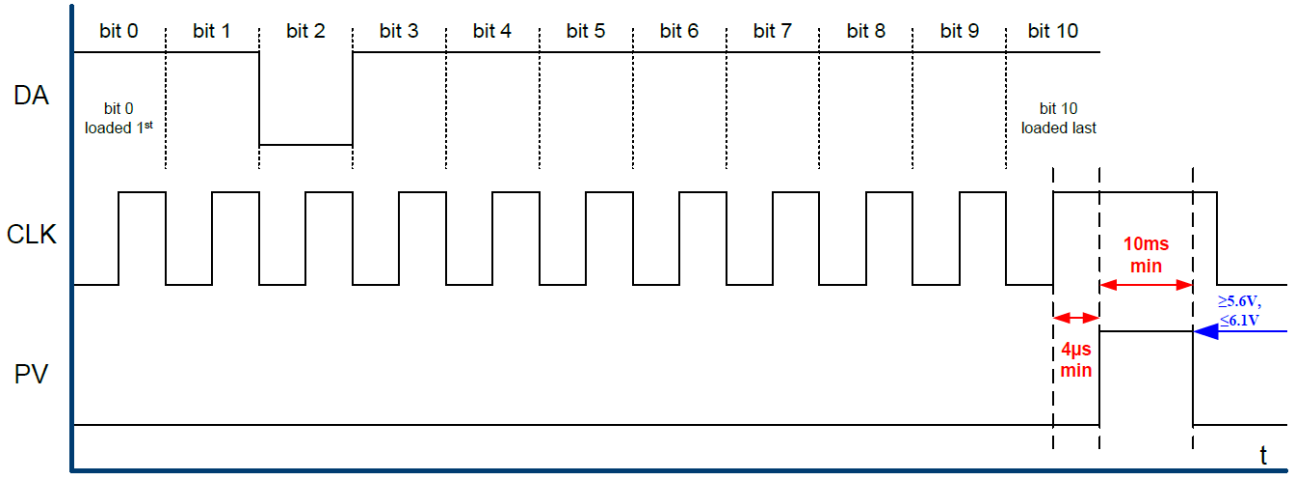


Figure 7 – First Programming Cycle to Program bit-2 into the EEPROM

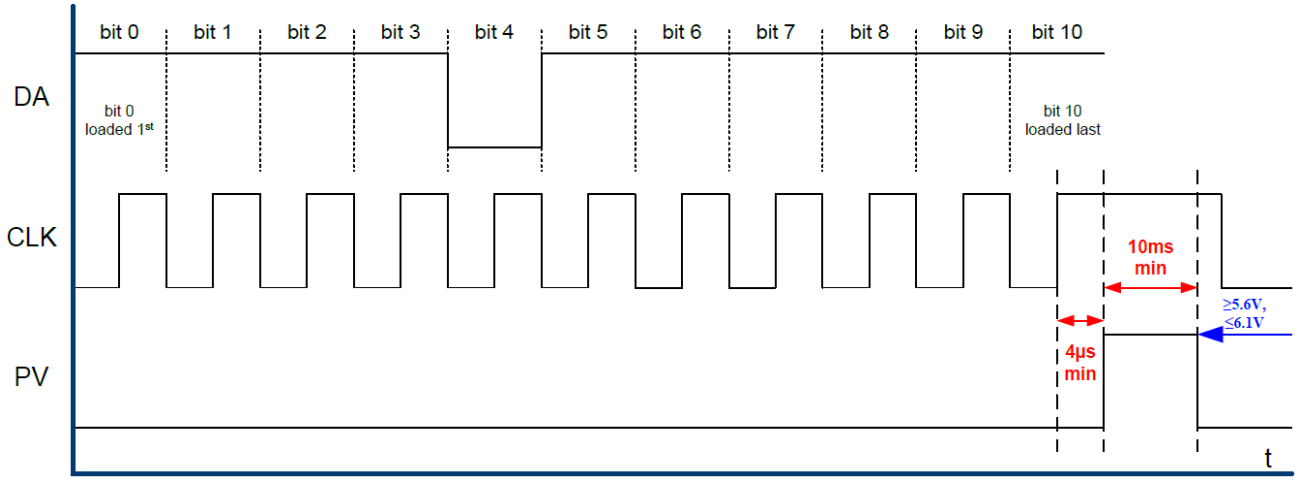


Figure 8 – Second Programming Cycle to Program bit-4 into the EEPROM

Reading Back from the EEPROM

During programming, the PV pin is used to program the necessary control bits into the EEPROM. However, it is also used to read the bits currently programmed into the EEPROM. When the PV pin is not used during programming, the CTST571 provides a weak pull-up and pull-down on the pin. This allows the EEPROM data to be shifted out to the PV pin and read after the CLK sequence is complete and when the DA & CLK pins are high (Figure 9). Each EEPROM bit is selected by setting the DA signal low (EEPROM selection is active low) during the CLK sequence. With an external 68kΩ resistor pull-up to V_{DD} on the PV pin, a low EEPROM bit produces ≤ 0.4*V_{DD} level while a high EEPROM bit produces a ≥ 0.6*V_{DD} level.

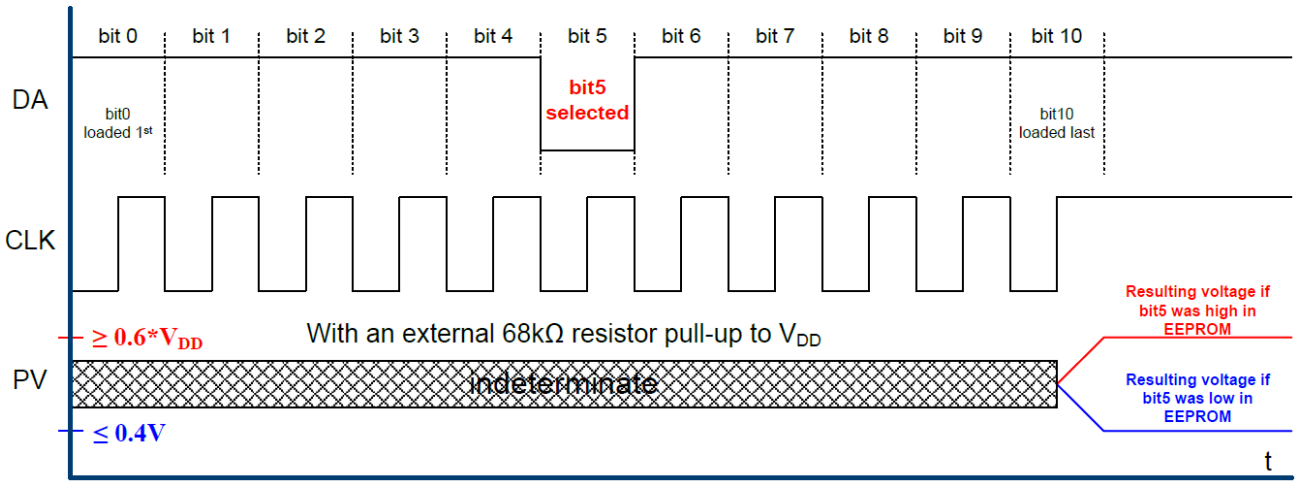


Figure 9 – Timing Diagram to Read bits from EEPROM

Erasing the EEPROM

The EEPROM can be erased by initiating a programming cycle with all DA bits set high, including bit-9 and bit-10. After the programming cycle, all the EEPROM bits are set low (logical high) except for the check bit (bit-0), which remains high.

Table 4 – Erase Sequence for EEPROM

Step	Action
1	Set the V_{DD} supply voltage to +5.0V.
2	Load the programming word bits all high.
3	Set the PV pin to +6V (≥5.6V, ≤6.1V) with the pulse and idle shown in timing diagram (Figure 10).
4	Verify the correct EEPROM contents by reading back the individual bits.

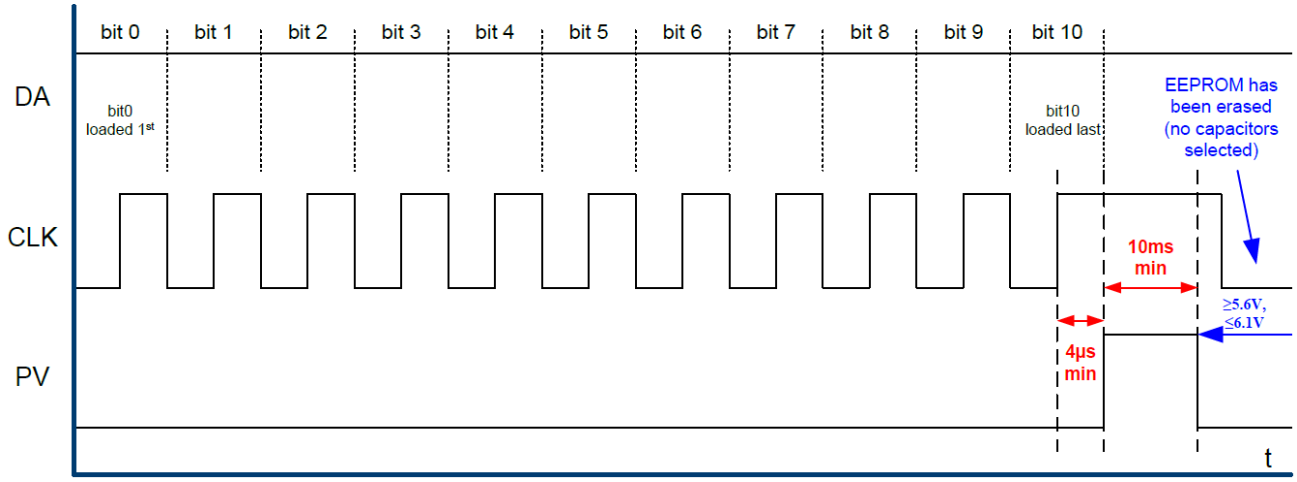


Figure 10 – Programming Sequence for Erasing the EEPROM

Programming Voltage Limit Circuit

Some existing programming circuits use a current source connected to a 6.5 – 8.0V supply. That circuit produces an excessive voltage on the PV pin, which can damage the CTST571. A simple modification eliminates the issue and maintains full programming compatibility with existing programming methods. A 5.6V, ½ watt Zener, 1N5232B or equivalent, placed between the PV pin and ground will limit the voltage while still allowing the programming circuit to generate the current required for programming fuse link type parts.

ELECTRICAL SPECIFICATIONS

Table 5 – Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Power Supply	Supply voltages between 4.0V-4.5V may not allow for reliable operation	2.375		3.63	V
			4.5		5.5	
$V_{ABSOLUTE}$	Power Supply		0		6.5	V
V_I[1]	Input Voltage		-0.5		V_{DD} + 0.5	V
T_A	Operating Temperature Range		-40		+125	°C
T_{STG}	Storage Temperature Range		-65		+150	°C
ESD_{HBM}	Human Body Model		2000			V
ESD_{MM}	Machine Model		200			V
ESD_{CDM}	Charged Device Model		2000			V

[1] PV pin can exceed V_{DD} by 1.2V during the programming interval.

Table 6 – DC Characteristics

DC Characteristics (V_{DD} = 2.375V to 5.5V unless otherwise specified, TA = -40 to +125°C)

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
C_{PV}	Capacitance variation across process		-15		+15	%
C_{VV}	Capacitance variation across output voltage	Voltage variation at X_1 pin, 100MHz			±150	ppm/V
C_{TV}	Capacitance variation across temperature	100MHz – Zero Code		325		ppm/°C
		100MHz – Mid Code[1]		40		
		100MHz – Full Scale		130		
V_{IH}	Input HIGH Voltage	DA, CLK	0.8 * V_{DD}			V
V_{IL}	Pull-down Resistor	DA, CLK	0.2 * V_{DD}			V
$R_{PD,D}$	Pull-down Resistor	DA		55k		Ω
$R_{PD,CLK}$	Pull-down Resistor	CLK		75k		Ω
$R_{PD,PV}$	Pull-down Resistor	PV		170k		Ω
V_{OH}	Output HIGH Voltage	PV pin when reading EEPROM bits 68kΩ pull-up resistors to V_{DD}		0.6 * V_{DD}		V
V_{OL}	Output LOW Voltage			0.4 * V_{DD}		V
V_{PP}	Programming Voltage (V_{DD} = 5.0V)	PV pin when programming EEPROM	5.6	6.0	6.1	V
I_{DD}	Power Supply Current	Normal Operation, V_{DD} <3.63V		10.0	35	µA
		Normal Operation, V_{DD} >3.63V		20.0	70	
I_{DDPROG}	Power Supply Current	Programming Mode			20	µA
t_{MEM}	EEPROM Data Retention			20		yrs
t_{PROG}	Programming Temperature	Recommended		25		°C
Cy_{PROG}	Programming Cycle		10			k

[1] bit-4, bit-7 High.

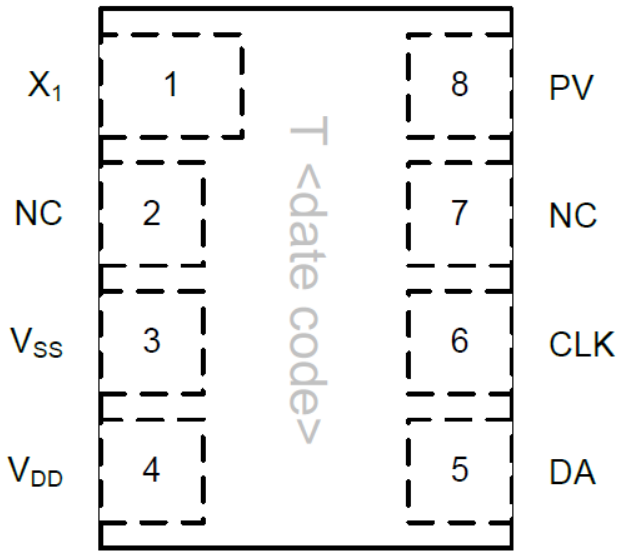
Table 8 – AC Characteristics
AC Characteristics (V_{DD} = 2.375V to 5.5V unless otherwise specified, T_A = -40 to +125°C)

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
C_F	Fixed Capacitance			6.6		pF
C_{HI}	Step Size			6.4		pF
	Max Value			19.2		
C_{MID}	Step Size			1.4		pF
	Max Value			9.8		
C_{LO}	Step Size			0.063		pF
	Max Value			1.953		
CLK	Max CLK Rate	50% duty cycle			100	kHz
T_{PROG}	Programming Time (V_{DD} = 5.0V, PV = 6.0V)			10.0		ms
Q	Q Value	20MHz – Full Scale	200	320		
		20MHz – Mid Scale	100	200		
		100MHz – Full Scale	50	80		
		100MHz – Mid Scale	50	70		
		200MHz – Full Scale	25	40		
		200MHz – Mid Scale	35	50		
		800MHz – Full Scale	8	12		
		800MHz – Mid Scale	10	15		

Pin Description and Configuration

Pin Assignments for SON8 Package

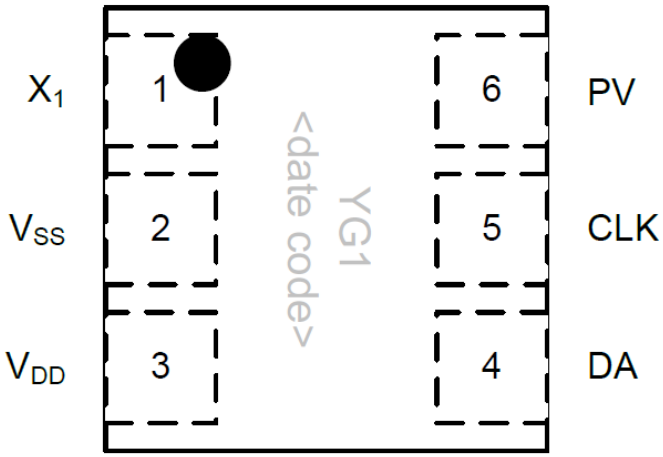
Pin	Name	Type	Function
1	X_1	Output	Capacitance
2	NC	n/a	Not connected
3	V_{SS}	Power	Negative Supply (GND)
4	V_{DD}	Power	Positive Supply
5	DA	Input	Programming Data Input
6	CLK	Input	Programming Clock Input
7	NC	n/a	Not connected
8	PV	Input	Programming Voltage



SON8

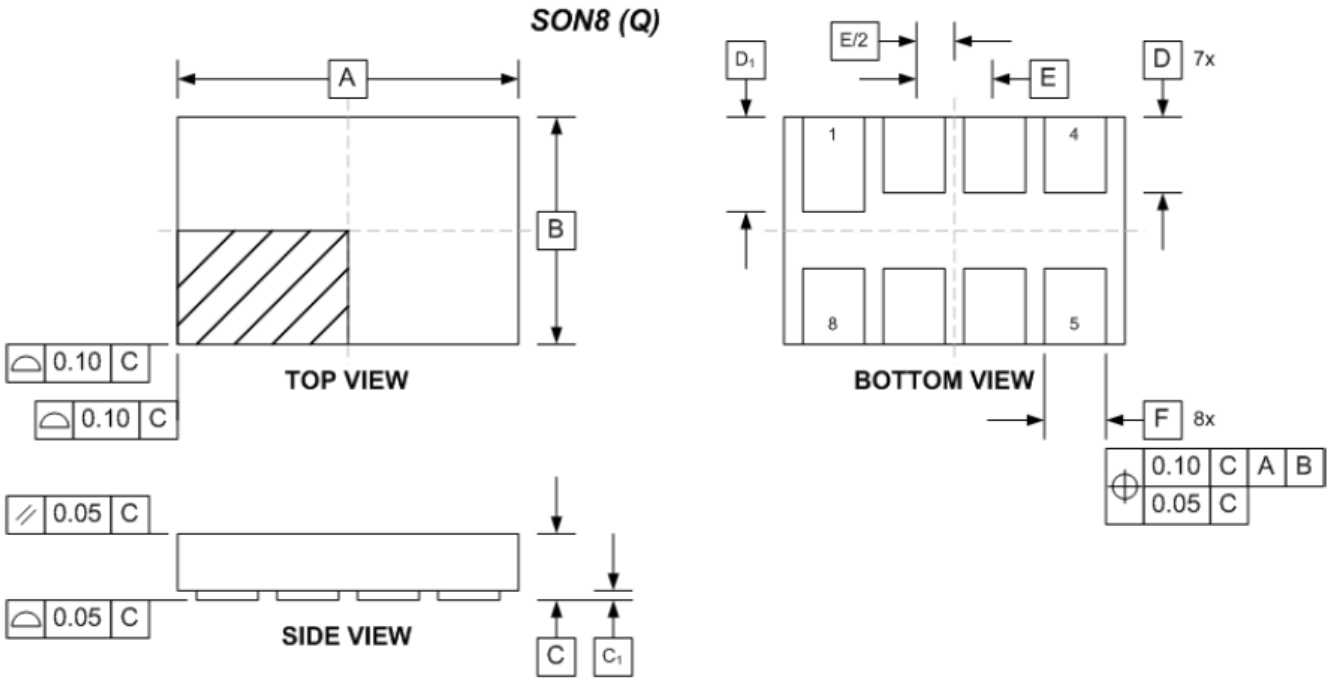
Pin Assignments for 6MLP

Pin	Name	Type	Function
1	X_1	Output	Capacitance
2	V_{SS}	Power	Negative Supply (GND)
3	V_{DD}	Power	Positive Supply
4	DA	Input	Programming Data Input
5	CLK	Input	Programming Clock Input
6	PV	Input	Programming Voltage



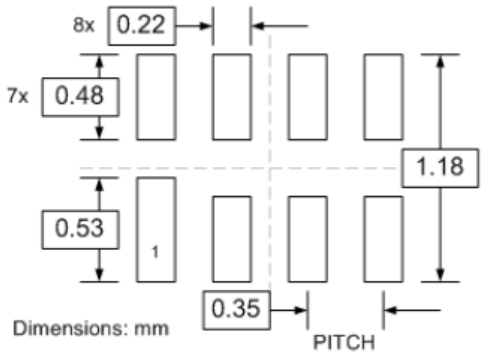
MLP6

PACKAGE DIMENSIONS

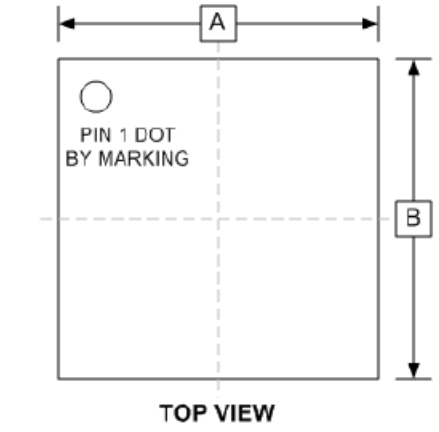


	MILLIMETERS	
DIM	MIN	MAX
A	1.50 BSC	
B	1.00 BSC	
C	---	0.40
C_1	0.00	0.05
D	0.25	0.35
D_1	0.30	0.40
E	0.35 BSC	
F	0.15	0.25

PCB LAND PATTERN/FOOTPRINT

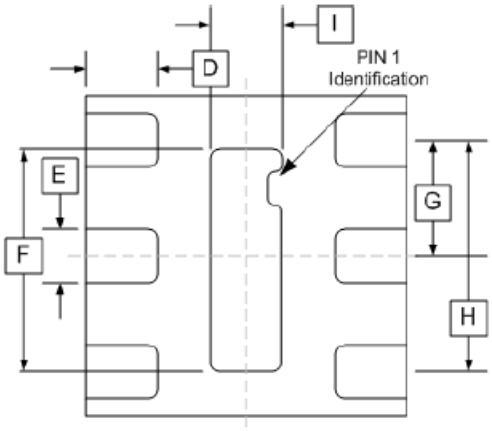


PACKAGE DIMENSIONS

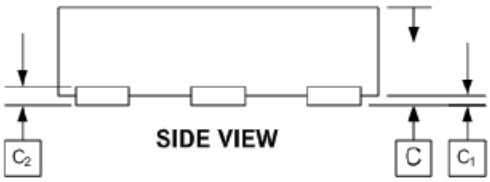


TOP VIEW

MLP6 (M)



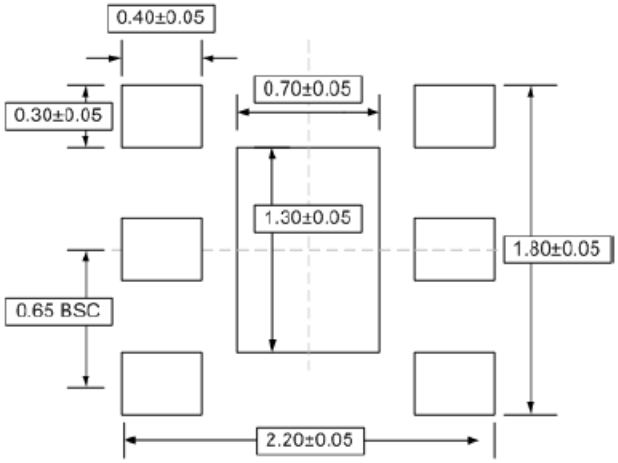
BOTTOM VIEW



SIDE VIEW

DIM	MILLIMETERS MIN	MAX
A	2.00±0.050	
B	2.00±0.050	
C	0.75±0.050	
C_1	0.00	0.05
C_2	0.203 Ref.	
D	0.35±0.050	
E	0.25±0.050	
F	1.40±0.050	
G	0.650 BSC	
H	1.300 REF	
I	0.80±0.050	

PCB LAND PATTERN/FOOTPRINT



PART ORDERING INFORMATION

Part Number	Package	Marking
CTST571QG	SON8	Y YM
CTST571MG	MLP6	Y1G / YM