HMC420QS16 / 420QS16E

v03.0810

CELLULAR RFIC DOWNCONVERTER, 0.7 - 1.0 GHz

Typical Applications

The HMC420QS16 / HMC420QS16E is ideal for:

- GSM & CDMA Infrastructure
- GPRS & EDGE Infrastructure
- Wireless Data/CDPD

Features

+15 dBm Input IP3

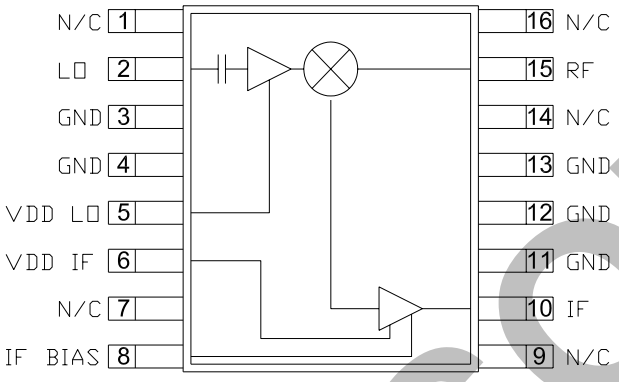
Integrated IF & LO Amps: 0 dBm LO

Conversion Gain: 12.5 dB

Noise Figure: 13 dB

Single Positive Supply: +5V, 52 mA

Functional Diagram



General Description

The HMC420QS16 & HMC420QS16E are linear downconverter receiver ICs suitable for cellular infrastructure applications from 0.7 - 1.0 GHz. An integrated mixer coupled with a high dynamic range IF amplifier achieves an input intercept point (OIP3) of +15 dBm, and an input P1dB of +1 dBm. The converter provides a gain of 12.5 dB and 13 dB typical single side band noise. The IC operates from positive +5V rails consuming 52 mA of current while requiring only 0 dBm LO drive. The design requires no external baluns, and minimal off chip components. The HMC420QS16 & HMC420QS16E have the same package footprint as the HMC380QS16G & HMC421QS16 1.4 - 2.3 GHz downconverter ICs.

Electrical Specifications, T_A = +25 °C, LO = 0 dBm, IF = 120 MHz, Vdd = 5V

Parameter	Min.	Typ.	Max.	
Frequency Range, RF & LO		0.7 - 1.0		GHz
Frequency Range, IF *		50 - 250		MHz
Conversion Gain	9	12.5		dB
Noise Figure (SSB)		13		dB
LO to RF Isolation	15	25		dB
LO to IF Isolation	23	30 - 42		dB
RF to IF Isolation	33	40 - 55		dB
IP3 (Input)	12	15		dBm
1 dB Compression (Input)	-2	+1		dBm
LO Input Drive Level (Typical)		-2 to +4		dBm
Supply Current (Idd for IF + LO) (IF bias resistor= 6.8 ohms)		52		mA

** IF matching must be tuned for optimal results. See application circuit herein.*

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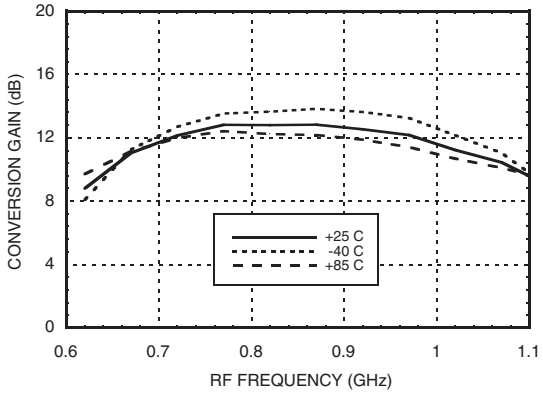
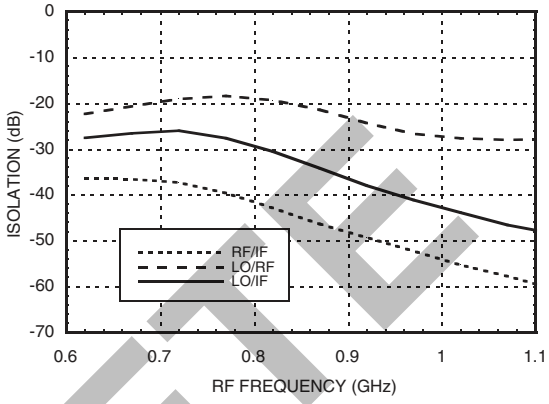
Application Support: Phone: 1-800-ANALOG-D

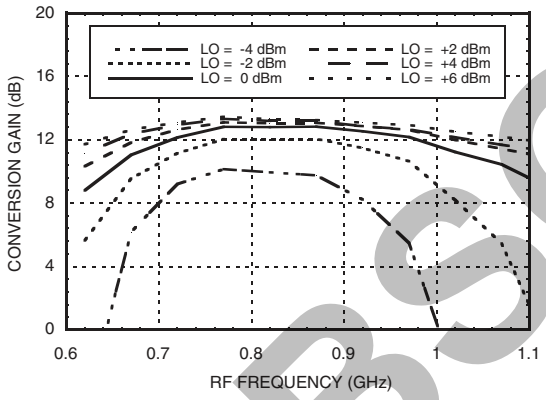
Conversion Gain vs. Temperature @ LO = 0 dBm



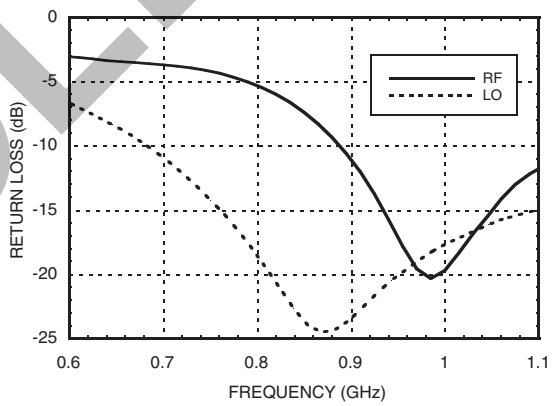
Isolation @ LO = 0 dBm



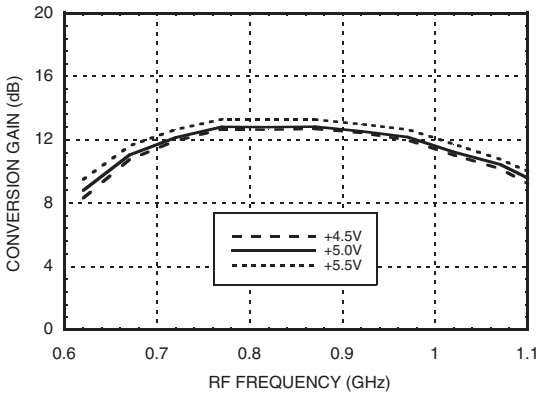
Conversion Gain vs. LO Drive



Return Loss @ LO = 0 dBm



Conversion Gain vs. Vdd @ LO = 0 dBm



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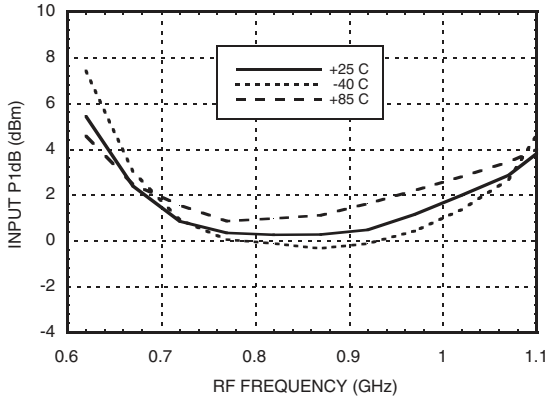
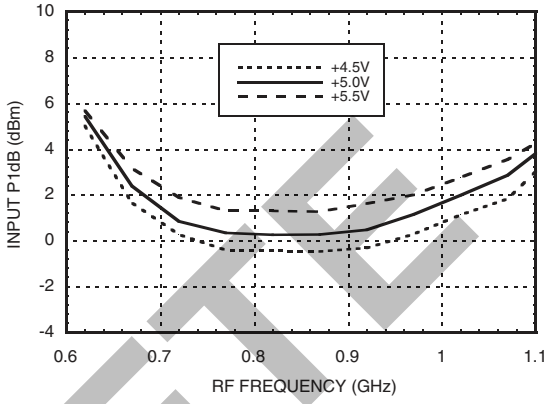
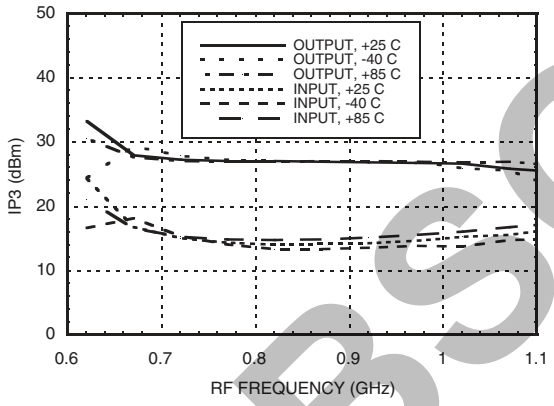
Input P1dB vs. Temperature @ LO = 0 dBm



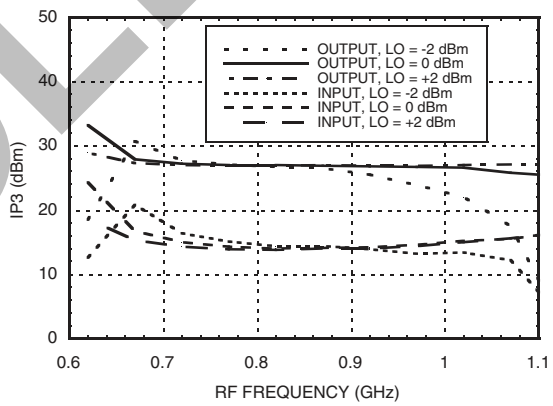
Input P1dB vs. Vdd @ LO = 0 dBm



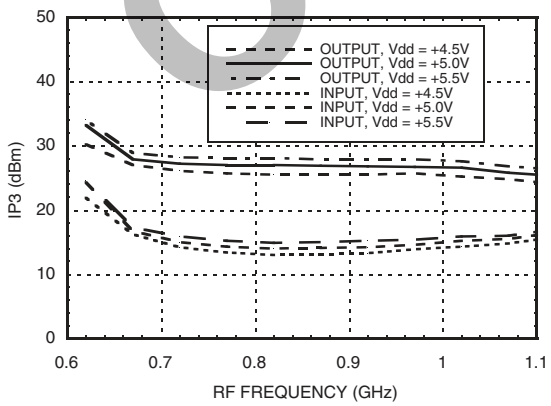
Input and Output IP3 vs. Temperature @ LO = 0 dBm*



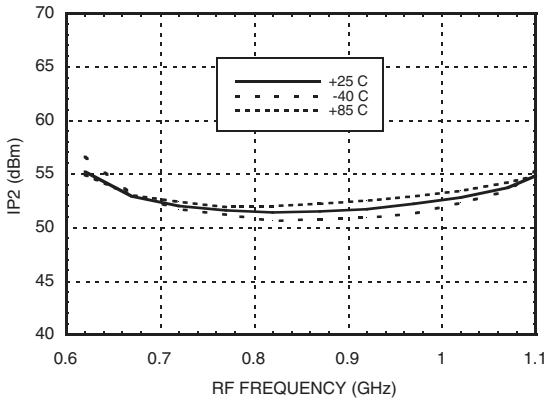
Input and Output IP3 vs. LO Drive*



Input and Output IP3 vs. Vdd @ LO = 0 dBm*



Input IP2 vs. Temperature @ LO = 0 dBm*



** Two-tone input power= -5 dBm each tone, 1 MHz spacing.*

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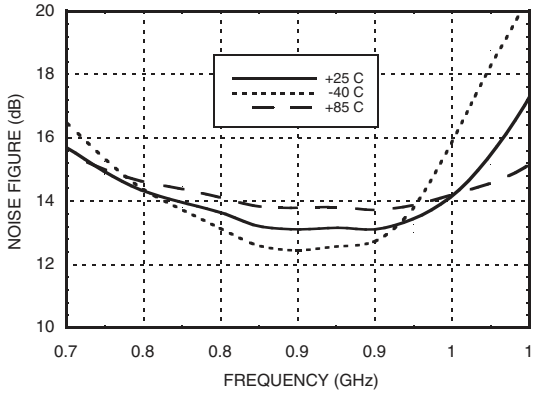
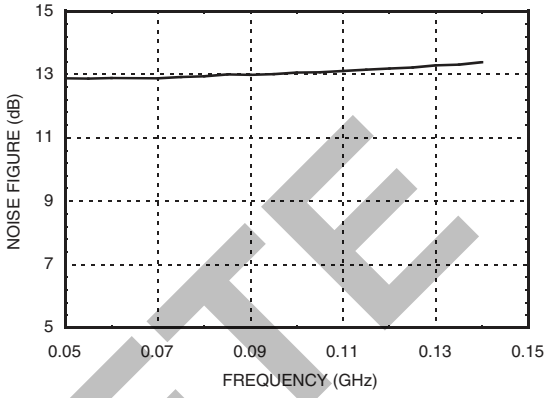
CELLULAR RFIC DOWNCONVERTER, 0.7 - 1.0 GHz

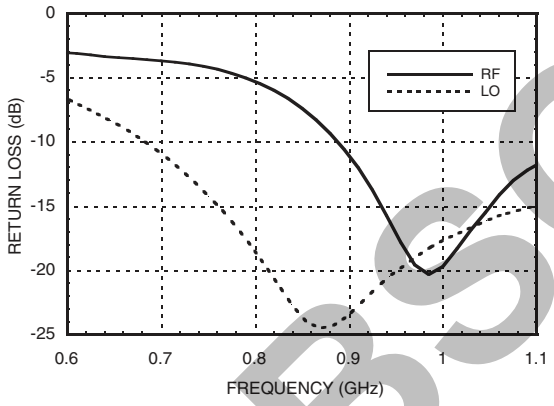
Noise Figure vs. Temperature, Swept LO, Fixed IF= 120 MHz



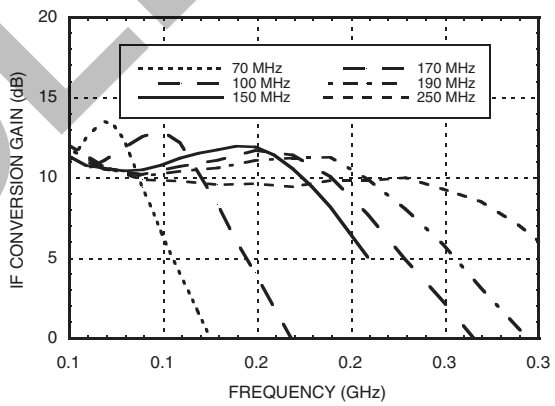
Noise Figure Swept IF, Fixed LO = 800 MHz



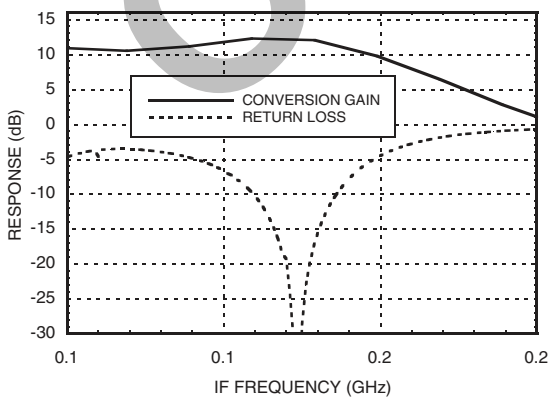
IF Return Loss @ Various Tuned IF Frequencies*



IF Bandwidth @ Various Tuned IF Frequencies*



IF Bandwidth @ LO = 0 dBm, IF= 120 MHz*



Harmonics of LO

	nLO Spur @ RF Port			
LO Freq. (GHz)	1	2	3	4
0.55	21	14	50	45
0.65	18	12	48	43
0.75	22	15	42	38
0.85	27	20	40	46
0.95	28	26	44	57
1.05	27	31	54	66

LO = 0 dBm
Values in dBc below input LO level measured at RF port.

** Refer to HMC420QS16 Application Circuit herein for IF port tuning information.*

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MxN Spurious @ IF Port

	nLO				
mRF	0	1	2	3	4
0	xx	41	89	66	75
1	62	0	64	>113	103
2	>113	102	51	82	>113
3	>113	>113	>113	71	>113
4	>113	>113	>113	>113	>113

RF Freq.= 0.92 GHz @ -10 dBm
LO Freq.= 0.8 GHz @ 0 dBm
All values in dBc relative to the IF power level.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Absolute Maximum Ratings

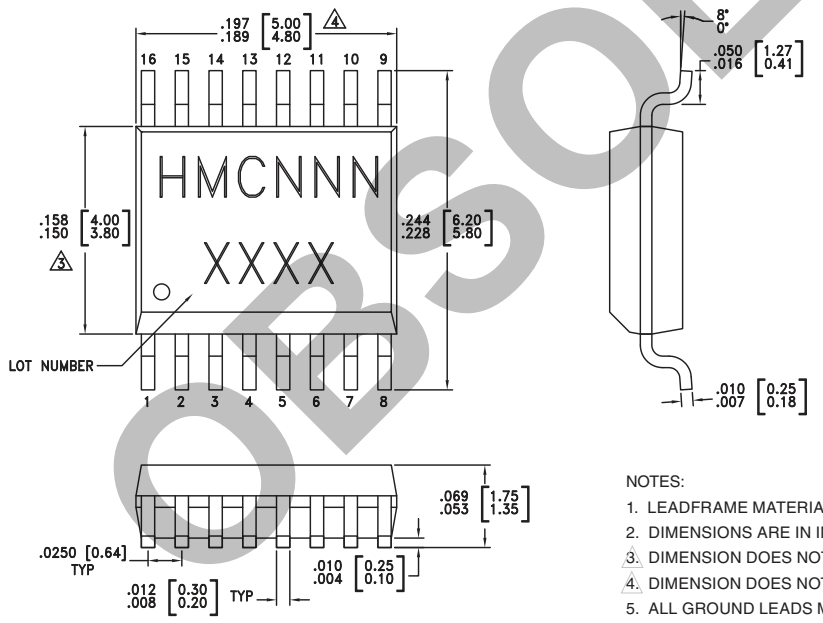
RF / IF Input (Vdd= +5V)	+13 dBm
LO Drive (Vdd= +5V)	+15 dBm
Vdd (LO or IF)	+7 Vdc
Channel Temperature	150°C
Continuous Pdiss (T = 85°C) (derate 6.34 mW/°C above 85°C)	0.41 W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 deg °C

Typical Supply Current vs. Vdd

Vdd (Vdc)	Idd (mA)
4.5	51
5.0	52
5.5	53

Note: Mixer will operate over full voltage range shown above.

Outline Drawing



NOTES:
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
4. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
5. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC420QS16	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	HMC420 XXXX
HMC420QS16E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	HMC420 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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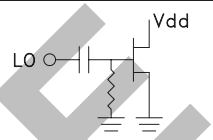
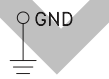
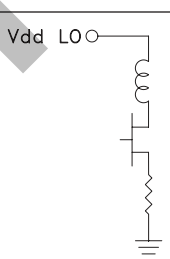
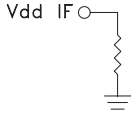
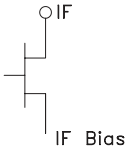
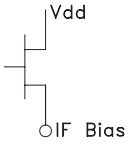
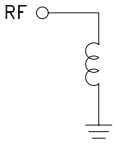
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 7, 9, 14, 16	N/C	Not Connected	
2	LO	This pin is AC coupled and matched to 50 Ohm from 0.7 - 1.0 GHz. An external series inductor (6.8 nH) is required.	
3, 4, 11, 12, 13	GND	Pin must connect to RF ground.	
5	Vdd LO	Power supply for the LO amplifier. One external RF bypass capacitor (10,000 pF) is required.	
6	Vdd IF	Bias voltage for IF amplifier. One external RF bypass capacitor (10,000 pF) is required.	
8	IF Bias	DC bias setting for IF amplifier.	
10	IF	Output of IF and bias port for amplifier. A pull up inductor (L1), output matching network (C5, C6, L2), and 10,000 pF bypass capacitor (C4) are required.	
15	RF	This pin is DC coupled and matched to 50 Ohm from 0.7 - 1.0 GHz.	

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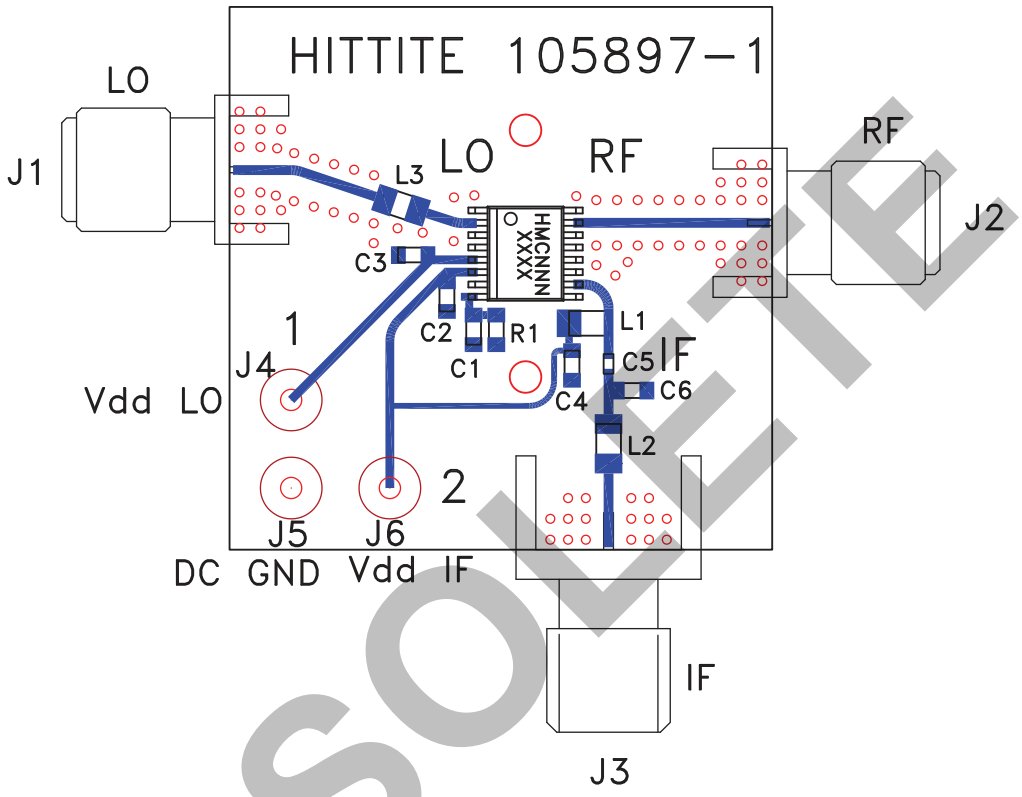
Evaluation PCB



List of Materials for Evaluation PCB 105361 [1]

Item	Description
J1 - J3	PCB Mount SMA RF Connector
J4 - J6	DC Pins
C1	1000 pF Chip Capacitor, 0603 Pkg.
C2, C3, C4	0.01µF Chip Capacitor, 0603 Pkg.
C5	33 pF Chip Capacitor, 0402 Pkg.
C6 [3]	12 pF Chip Capacitor, 0603 Pkg.
L1	330 nH Chip Inductor, 0805 Pkg.
L2 [3]	150 nH Chip Inductor, 0805
L3	6.8 nH Inductor, 0805 Pkg.
R1	6.8 Ohm Resistor, 0603
U1	HMC420QS16 / HMC420QS16E Mixer
PCB [2]	105897 Evaluation Board, 1.100" x 1.100"

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

[3] For 120 MHz IF. See Application Circuit for alternate IF frequency tuning.

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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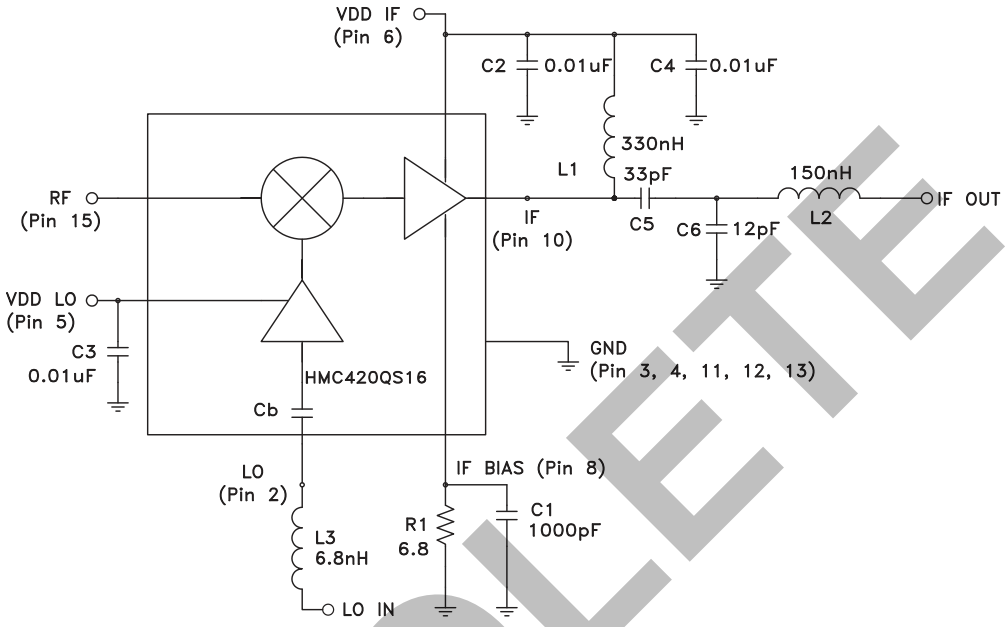
Application Circuit



Note: Pin 5 and Pin 6 may be connected to a common Vdd Supply.

Selection of L2 & C6 For Various Tuned IF Frequencies

IF	L2*	C6*
120 MHz	150 nH	12 pF
70 MHz	180 nH	39 pF
100 MHz	180 nH	18 pF
150 MHz	120 nH	9 pF
170 MHz	120 nH	7 pF
190 MHz	100 nH	6 pF
250 MHz	82 nH	4 pF

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