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60V Current-Mode Buck Controller with Lossless Current Sense

MAX15157D

General Description

The MAX15157D is the evolution of the MAX15157B HV buck controller family. The MAX15157D implements a single-phase, PWM valley current-mode controller and drives two external power MOSFETs in a buck configuration. The output voltage can be dynamically set through the 1V to 2.2V reference input (REFIN) for modular design support.

The switching frequency is controlled either through external resistor that sets the internal oscillator, or by synchronizing the regulator to an external clock. The device is designed to support 60kHz to 1MHz switching frequencies. The controller has a dedicated undervoltage lockout pin (UVLO) and an accurate enable input threshold for flexible power sequence configuration. The controller also has multiple fault-protection circuits to protect against overcurrent (OCP) adjustable through the ILIM pin, output overvoltage (OVP), input undervoltage (UVLO), and thermal shutdown.

The MAX15157D features an adjustable internal compensation ramp. The device incorporates an accurate current-sense amplifier that reports output current through an analog output (IMON).

The MAX15157D features lossless LS FET R_{DSON} or resistor current sensing. The device allows programmable single-phase or multiphase operation, up to eight interleaved phases, and implements an accurate current balance scheme. The MAX15157D can operate with either discrete inductors or coupled inductors in case of multiphase operation.

The device is available in a 5mm × 5mm, 32-pin TQFN package and supports a -40°C to +125°C junction temperature range.

Benefits and Features

- Wide Operating Range Reduces Development Time
  - 8V to 60V Input Voltage Range
  - 3V to 0.95 × V_{IN} Output Voltage Range
  - 60kHz to 1MHz Switching Frequency Range
  - Interleaved 1/2/3/4/6/8-Phase Operation
  - -40°C to +125°C Temperature Range
- Integration Reduces Design Footprint
  - Internal LDO for Bias Supply Generation
  - Synchronization Input
  - Current Monitor Output
  - Internal 2V Precision Reference
  - 2Ω Pullup and 0.6Ω Pulldown Fast Power FET Drivers
  - Accurate MOSFET Dead Time Adaptive Control
- Robust Fault Protection Improves Quality and Simplifies System Design
  - Adjustable Input Undervoltage Lockout
  - Adjustable Input EN
  - Adjustable Cycle-by-Cycle Overcurrent Protection
  - Input Undervoltage Fault Protection
  - Multiple Levels of Overvoltage Protection
  - Thermal Shutdown
- Flexible, Simple System Design
  - Adjustable Slope Compensation
  - Discrete Inductor or Compact Coupled Inductor Architecture
  - Lossless R_{DSON} or Resistor Current Sensing
- Small 5mm × 5mm, 32-Pin TQFN, 0.5mm Pitch

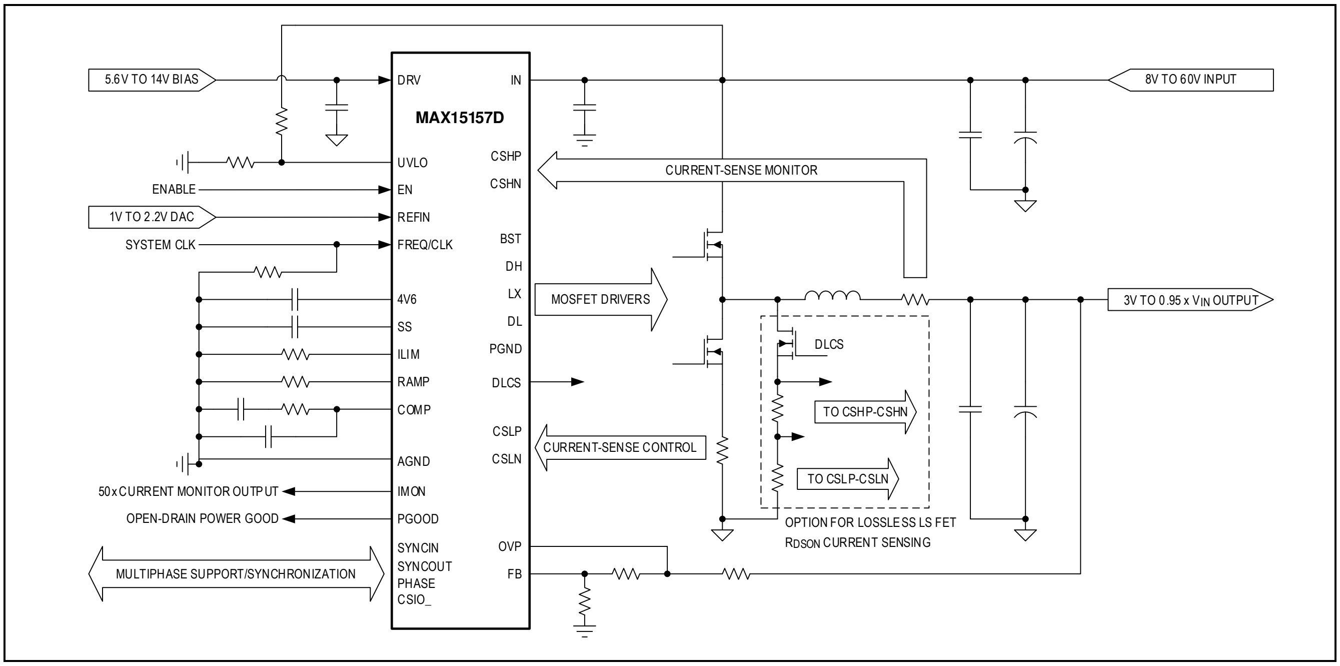
Applications

- Data Center
- Industrial
- Multiphase Buck

***Ordering Information* appears at end of data sheet.**

19-101127; Rev 1; 1/22

Typical Application Circuit



Absolute Maximum Ratings

IN to PGND .... -0.3V to +70V
CSLP, CSLN to PGND...................................... -0.3V to +0.3V
CSLP to CSLN .... -0.3V to +0.3V
CSHP, CSHN to PGND...................................... -0.3V to +70V
CSHP to CSHN .... -0.3V to +0.3V
LX to PGND .... -1V to +70V
LX + DRV ....< +80V
LX to PGND less than 50ns ....-2V
BST to PGND .... -0.3V to +80V
BST to LX... -0.3V to +16V
DH to LX... -0.3V to (V_{BST} + 0.3V)
DL, DLCS to PGND.............................. -0.3V to (V_{DRV} + 0.3V)
DRV to PGND .... -0.3V to +16V
4V6 to AGND .... -0.3V to +6V
DRV to 4V6 .... -0.3V to +16V
EN, FB, PGOOD, REFIN to AGND ....-0.3V to +6V
UVLO, OVP, FREQ/CLK, SYNCIN to AGND ....-0.3V to +6V
COMP, SS, IMON, RAMP to AGND...... -0.3V to (V_{4V6} + 0.3V)
SYNCOUT, PHASE, ILIM to AGND ...... -0.3V to (V_{4V6} + 0.3V)
CSION, CSIOP to AGND....................... -0.3V to (V_{4V6} + 0.3V)
PGND to AGND ....-0.3V to +0.3V
Maximum Current out of 4V6 .... 100mA
Operating Temperature Range....................... -40°C to +125°C
Continuous Power Dissipation (T_A = +70°C) TQFN (derate 34.5mW/°C above +70°C) 2.76W
Junction Temperature..+150°C
Storage Temperature Range.......................... -40°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow)...................................+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	T3255+4
Outline Number	21-0140
Land Pattern Number	90-0012
Thermal Resistance, Four-Layer Board	
Junction to Ambient (θ_{JA})	+29°C/W
Junction to Case (θ_{JC})	+1.7°C/W

For the latest package outline information and land patterns (footprints), go to http://www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to http://www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{IN} = 35V, V_{DRV} = 9V, V_{EN} = 3.3V, V_{UVLO} = 3.3V, OVP = 0V, REFIN = 4V6, R_{FREQ} = 100kΩ (600kHz), C_{4V6} = 4.7µF, C_{SS} = 10nF, T_A = T_J = -40°C to +125°C unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES						
IN Operating Range	V_{IN}		8		60	V
DRV Operating Range	V_{DRV}		5.6		14	V
IN Quiescent Current	I_{IN}	Not switching, including current-reporting bias current		504	950	µA
IN Shutdown Current	$I_{IN(SHDN)}$	EN = AGND		2.8	8.0	µA
DRV Quiescent Current	I_{DRV}	Not switching		4.8	8.0	mA
DRV Shutdown Current		EN = AGND		16	35	µA
IN Undervoltage-Lockout Threshold	$V_{IN(UVLO)}$	V_{IN} rising, single phase	5.04	5.2	5.35	V
		V_{IN} falling, single phase	4.85	5	5.2	
		V_{IN} rising, multiphase	7.3	7.5	7.7	
		V_{IN} falling, multiphase	7.05	7.25	7.45	
DRV Undervoltage-Lockout Threshold	$V_{DRV(UVLO)}$	V_{DRV} rising	4.9	5.06	5.22	V
		V_{DRV} falling	4.8	4.97	5.1	
4V6 BIAS LINEAR REGULATOR						
Bias LDO Output Voltage	V_{4V6}	No load	4.42	4.5	4.56	V
Bias LDO Current Limit			33	51	75	mA
4V6 Undervoltage-Lockout Threshold	$V_{4V6(UVLO)}$	V_{4V6} rising	4.12	4.25	4.38	V
		V_{4V6} falling	4.08	4.2	4.3	
CONTROLLER ENABLE						
EN Logic Threshold	V_{EN}	EN rising	0.67	0.7	0.74	V
		EN falling, after LDO in regulation	0.51	0.54	0.58	
EN Input-Leakage Current	I_{EN}	V_{EN} = 0 to 5V	-1		+1	µA
UVLO Adjustable Undervoltage-Lockout Threshold	V_{UVLO}	V_{UVLO} rising	0.965	1.000	1.035	V
		V_{UVLO} falling	0.865	0.900	0.935	

(V_{IN} = 35V, V_{DRV} = 9V, V_{EN} = 3.3V, V_{UVLO} = 3.3V, OVP = 0V, REFIN = 4V6, R_{FREQ} = 100kΩ (600kHz), C_{4V6} = 4.7µF, C_{SS} = 10nF, T_A = T_J = -40°C to +125°C unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UVLO Input-Leakage Current	I_{UVLO}	V_{UVLO} = 0 to 4.6V	-200		+200	nA
UVLO Deglitch Time				20	35	µs
CONTROL LOOP						
FB Regulation Threshold (Preset Mode)	V_{FB}	REFIN = 4V6	1.98	2.00	2.02	V
FB-to-REFIN Offset Voltage (Tracking Mode)		V_{FB} - V_{REFIN}, V_{REFIN} = 1V to 2.2V	-4.5		+4.5	mV
REFIN Input-Voltage Range	V_{REFIN}	(Note 2)	1		2.2	V
Preset Mode REFIN Threshold		REFIN rising	2.33	2.36	2.4	V
		REFIN falling	2.22	2.26	2.29	
FB Input-Leakage Current	I_{FB}	V_{FB} = 0 to 2.2V	-200		+200	nA
REFIN Input-Leakage Current	I_{REFIN}	V_{REFIN} = 1V to 2.2V	-100		+100	nA
Low-Side Current-Sense Differential Voltage Range	$\Delta V_{CSL\_}$	V_{CSLP} - V_{CSLN}		±200		mV
Low-Side Current-Sense Common-Mode Voltage Range	$V_{CSL\_}$	With respect to AGND		±300		mV
CSL_ Input-Leakage Current	$I_{CSL\_}$		-0.8		+0.8	µA
CSL_ Current-Sense Amplifier Gain	$A_{CSL\_}$			4.2		V/V
Error-Amplifier Transconductance	G_{MEA}		0.83	1.1	1.4	mS
Internal Slope-Compensation Ramp-Amplitude Adjustable Range	V_{RAMP}		380		1200	mV
RAMP Pin Input-Voltage Range	V_{RAMP_PIN}		120		380	mV
V_{RAMP}-to-V_{RAMP_PIN} Ratio		V_{RAMP_PIN} = 0.3V		3.18		V/V
RAMP Bias Current	I_{RAMP}	V_{RAMP_PIN} = 0V	5.4	6.0	6.6	µA
SWITCHING FREQUENCY						
Preset Switching Frequency	f_{SW}	R_{FREQ} = open, R_{PHASE} = 270kΩ	293	300	307	kHz
Adjustable Switching Frequency	f_{SW}	R_{FREQ} = 10kΩ, R_{PHASE} = 270kΩ	48	56	68	kHz
		R_{FREQ} = 25kΩ, R_{PHASE} = 270kΩ	135	145	156	
		R_{FREQ} = 100kΩ, R_{PHASE} = 270kΩ	550	592	642	
Synchronization Range	f_{SW}	FREQ/CLK driven by external clock	60		1000	kHz
CLK Frequency-Detection Range	f_{CLK}		0.12		6.00	MHz
CLK Logic Level	V_{CLK}	Logic-high (rising)		1.8	1.9	V

(V_{IN} = 35V, V_{DRV} = 9V, V_{EN} = 3.3V, V_{UVLO} = 3.3V, OVP = 0V, REFIN = 4V6, R_{FREQ} = 100kΩ (600kHz), C_{4V6} = 4.7µF, C_{SS} = 10nF, T_A = T_J = -40°C to +125°C unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		Logic-low (falling)	1.52	1.6		
FREQ/CLK Input Bias Current	I_{CLK}	$V_{FREQ/CLK}$ = AGND	-10.5	-9.8	-9.2	µA
CLK Switching Frequency-Divider Ratio	f_{CLK}/f_{SW}	R_{PHASE} = 270kΩ (1 phase)		2		kHz/kHz
		R_{PHASE} = 133kΩ (2 phases)		2		
		R_{PHASE} = 169kΩ (3, 6 phases)		6		
		R_{PHASE} = 210kΩ (4, 8 phases)		4		
SYNCHRONIZATION AND PHASE						
SYNCOUT Output-Voltage Level	$V_{SYNCOUT}$ - V_{4V6}	Logic-high, I_{SOURCE} = 10mA	4V6 - 0.4			V
	$V_{SYNCOUT}$	Logic-low, I_{SINK} = 10mA			0.4	
PHASE Source Current	I_{PHASE}		9.2	10	10.8	µA
OUTPUT-FAULT PROTECTION						
ILIM Bias Current	I_{ILIM}	ILIM = 0.615V	8.8	9.8	10.8	µA
ILIM Voltage Range	V_{ILIM}		0.35		1.95	V
ILIM to CSLP-CSLN Voltage Ratio		ILIM = 0.615V, low-side FET ON, cycle-by-cycle |40mV| typ threshold		15.375		V/V
CSLP-CSLN Cycle-by-Cycle Current-Limit Threshold		Low-side FET ON, |ADJ range|	21		124	mV
CSLP-CSLN Hiccup Current-Limit Threshold		Low-side FET ON, |ADJ range|	31.5		186	mV
CSLP-CSLN POCP Cycle-by-Cycle Current-Limit Threshold		Low-side FET ON, ILIM = BIAS	-43	-40	-37	mV
CSLP-CSLN NOCP Cycle-by-Cycle Current-Limit Threshold		Low-side FET ON, ILIM = BIAS	30	40	50	mV
CSLP-CSLN POCP Hiccup Current-Limit Threshold		Low-side FET ON, ILIM = BIAS	-69	-60	-50	mV
CSLP-CSLN NOCP Hiccup Current-Limit Threshold		Low-side FET ON, ILIM = BIAS	50	60	69	mV
Minimum REFIN and SS Voltage for Valid FB Faults		REFIN = SS, 80mV hysteresis	0.998	1.02	1.03	V
FB Undervoltage Threshold (Preset Mode)	FB_UV	Measured with respect to target voltage (REFIN = 4V6 and V_{REFIN} = 2V), V_{FB} falling, 3% hysteresis	-8	-9	-10	%
FB Undervoltage Threshold (Tracking Mode)	FB_UV	Measured with respect to target voltage (V_{REFIN} = 1.2V), V_{FB} falling, 3% hysteresis	-8	-9	-10	%
FB Overvoltage Threshold (Preset Mode)	FB_OV	Measured with respect to target voltage (REFIN = 4V6 and V_{REFIN} = 2V), V_{FB} falling, 3% hysteresis	+8	+9	+10	%
FB Overvoltage Threshold (Tracking Mode)	FB_OV	Measured with respect to target voltage (V_{REFIN} = 1.2V), V_{FB} falling, 3% hysteresis	+8	+9	+10	%

(V_{IN} = 35V, V_{DRV} = 9V, V_{EN} = 3.3V, V_{UVLO} = 3.3V, OVP = 0V, REFIN = 4V6, R_{FREQ} = 100kΩ (600kHz), C_{4V6} = 4.7µF, C_{SS} = 10nF, T_A = T_J = -40°C to +125°C unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Adjustable Overvoltage-Protection Threshold	V_{OVP}	V_{OVP} rising	1.96	2.00	2.04	V
		V_{OVP} falling	1.87	1.90	1.94	
Overvoltage-Protection Input-Leakage Current	I_{OVP}	V_{OVP} = 0 to 4.6V	-200		+200	nA
Fixed-Output Overvoltage-Protection Threshold	$V_{OVP(CSH\_)}$	V_{CSHN} rising, 2.9V hysteresis	63.5	65.4	67.5	V
Fault Propagation Delay		UVP falling edge		34		µs
		OVP rising edge		20		
		Consecutive cycle-by-cycle CSL_ current-limit events		4		cycles
		EXT UVLO, EXT OVLO		28		µs
		IMON average OCP		32		cycles
		FB_OV, FB_UV		32		CLK cycles
PGOOD Startup Delay				64		CLK cycles
PGOOD Output-Low Voltage	V_{PGOOD}	I_{SINK} = 3mA		38	85	mV
PGOOD Leakage Current	I_{PGOOD}	FB = REFIN (PGOOD in high-impedance state), V_{PGOOD} = 5V			2	µA
Thermal Shutdown	T_{SHDN}	15°C hysteresis		165		°C
SOFT-START and HICCUP						
SS Current Capability	I_{SS}	Source	4.8	5.0	5.2	µA
		Sink	-5.5	-5.0	-4.2	
SS Pulldown Resistance	R_{SS}	Discharge		5		Ω
SS Undervoltage-Lockout Threshold	$V_{UVLO(SS)}$	SS rising, PWM enabled	41	50	59	mV
Hiccup Autoretry Period				32,768		CLK cycles
MOSFET DRIVERS						
DH/DL Driver On-Resistance	R_D	Pullup		2		Ω
		Pulldown		0.6		
DLCS Driver On-Resistance	R_{DLCS}	Pullup		6		Ω
		Pulldown		1.8		
DH Minimum On-Time	t_{DH}	(Note 3)		55		ns
DL Minimum On-Time	t_{DL}	(Note 3)		72		ns
Driver Rise Time		C_{LOAD} = 3nF		20		ns
Driver Fall Time		C_{LOAD} = 3nF		10		ns
DH-to-DL Dead-Time Delay		C_{LOAD} = 3nF		20		ns
DL-to-DH Dead-Time Delay		C_{LOAD} = 3nF		20		ns
DL to DLCS Delay				40		ns
BST-to-LX Operating Range	V_{BST}		4.5		14	V

(V_{IN} = 35V, V_{DRV} = 9V, V_{EN} = 3.3V, V_{UVLO} = 3.3V, OVP = 0V, REFIN = 4V6, R_{FREQ} = 100kΩ (600kHz), C_{4V6} = 4.7µF, C_{SS} = 10nF, T_A = T_J = -40°C to +125°C unless otherwise noted.) (Note 1)

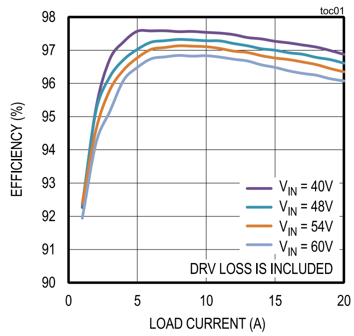
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BST Quiescent Current	I_{BST}	EN = AGND, LX = PGND, V_{BST} = 9V		35	55	µA
CURRENT MONITOR						
CSH_ High-Side Current-Sense Common-Mode Voltage Range	$V_{CSH\_}$	With respect to AGND	0		60	V
CSH_ High-Side Current-Sense Differential Voltage Range	$\Delta V_{CSH\_}$	Current-monitor range, V_{CSHP} - V_{CSHN}	0		50	mV
CSHP Input Bias Current	I_{CSHP}	V_{CSHP} = 60V		72	120	µA
		V_{CSHP} = 0V		136	260	
CSHN Input Bias Current	I_{CSHN}	V_{CSHN} = 60V		52	95	µA
		V_{CSHN} = 0V		144	260	
Current-Monitor Amplifier Gain	$A_{CSH\_}$	$V_{IMON}/\Delta V_{CSH\_}$		50		V/V
Current-Monitor Amplifier Accuracy	V_{IMON}	$V_{CSH\_}$ = 48V, $\Delta V_{CSH\_}$ = 30mV	1.41	1.50	1.63	V
IMON Average Current-Limit Threshold	$V_{OCP(AVE)}$		2.45	2.50	2.55	V
IMON Amplifier Output Capacitive Load Stability	C_{IMON}	No sustained oscillations		200		pF

Note 1:	Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization.
Note 2:	Operating REFIN below 1V is not recommended due to disabled fault protection.
Note 3:	Not tested, guaranteed by design.

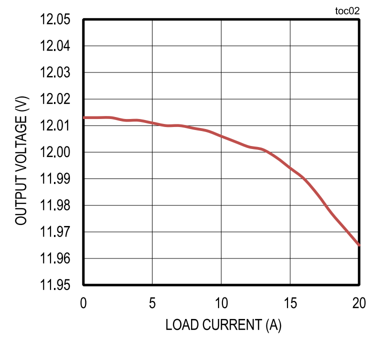
Typical Operating Characteristics

(T_A = -40°C to +125°C, V_{IN} = 54V, V_{OUT} = 12V, unless otherwise noted. See the *Standard Application Circuit*.)

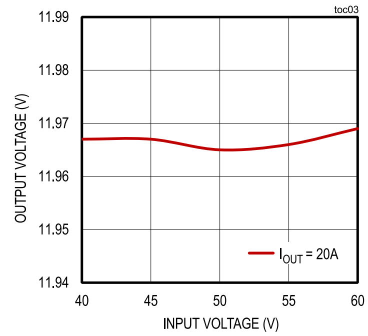
EFFICIENCY vs. OUTPUT LOAD



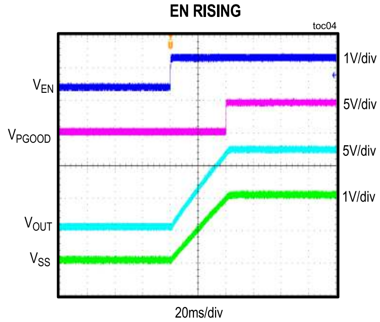
LOAD REGULATION



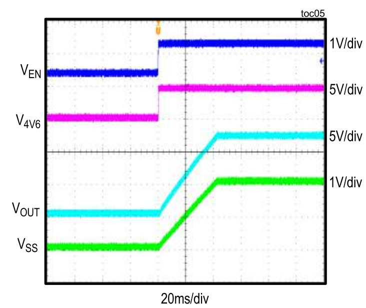
LINE REGULATION



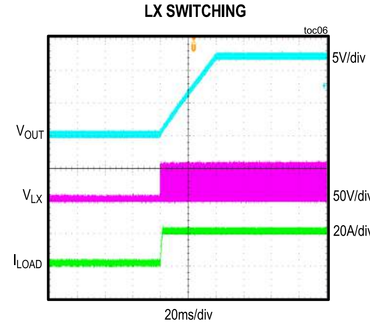
STARTUP WAVEFORM
EN RISING



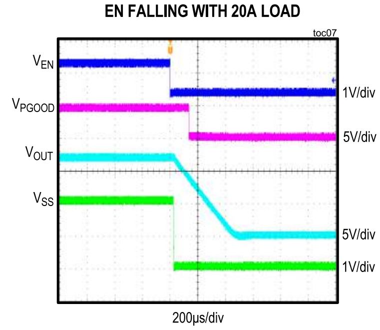
SOFT-START WAVEFORM



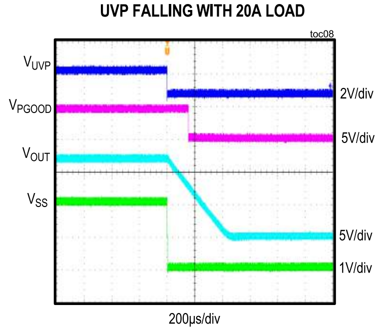
SOFT-START WAVEFORM
LX SWITCHING



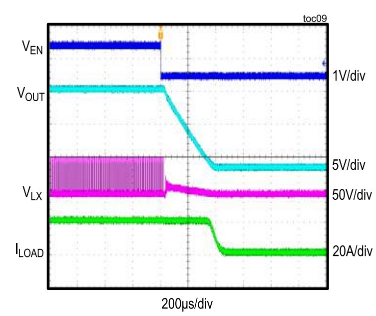
ACTIVE SHUTDOWN WAVEFORM
EN FALLING WITH 20A LOAD



ACTIVE SHUTDOWN WAVEFORM
UVP FALLING WITH 20A LOAD

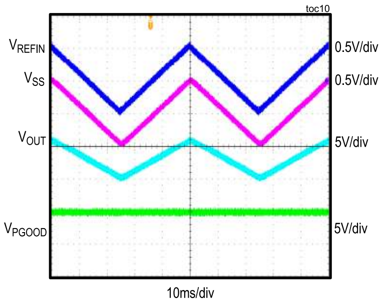


ACTIVE SHUTDOWN WAVEFORM
EN FALLING vs. LX SWITCHING

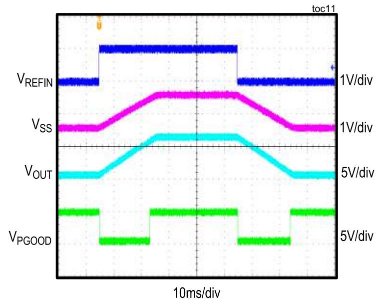


(T_A = -40°C to +125°C, V_{IN} = 54V, V_{OUT} = 12V, unless otherwise noted. See the *Standard Application Circuit*.)

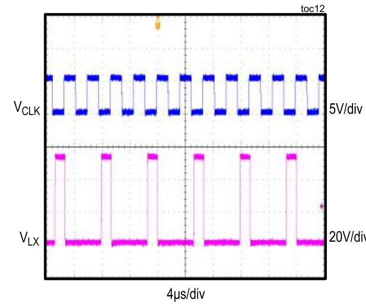
DYNAMIC REFIN RAMP RESPONSE
6V TO 12V OUTPUT



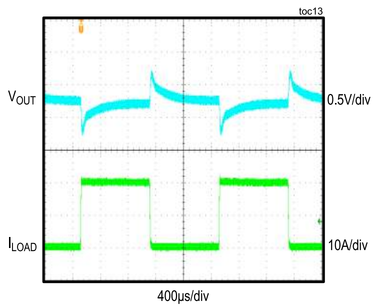
DYNAMIC REFIN STEP RESPONSE
6V TO 12V OUTPUT



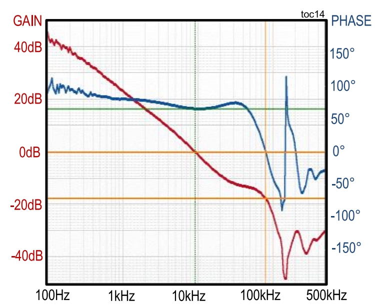
CLK SYNCHRONIZATION



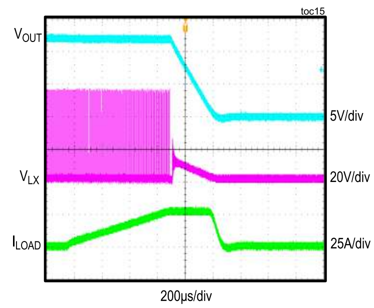
LOAD TRANSIENT WAVEFORM
WITH 20A LOAD STEP



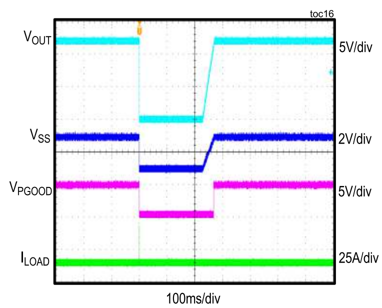
BODE PLOT WITH 20A LOAD



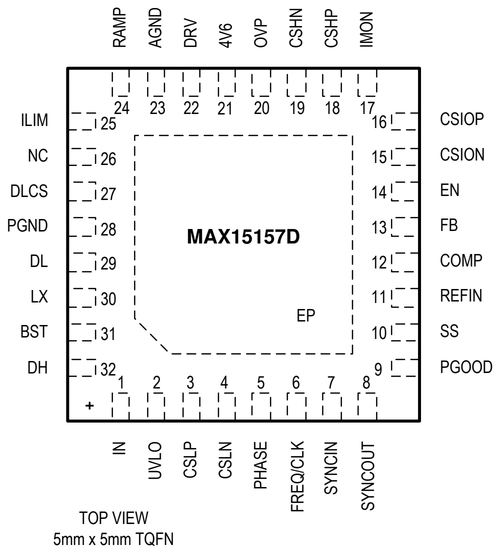
OUTPUT OVERCURRENT
WAVEFORM



AUTORETRY AFTER
OVERCURRENT FAULT



Pin Configurations

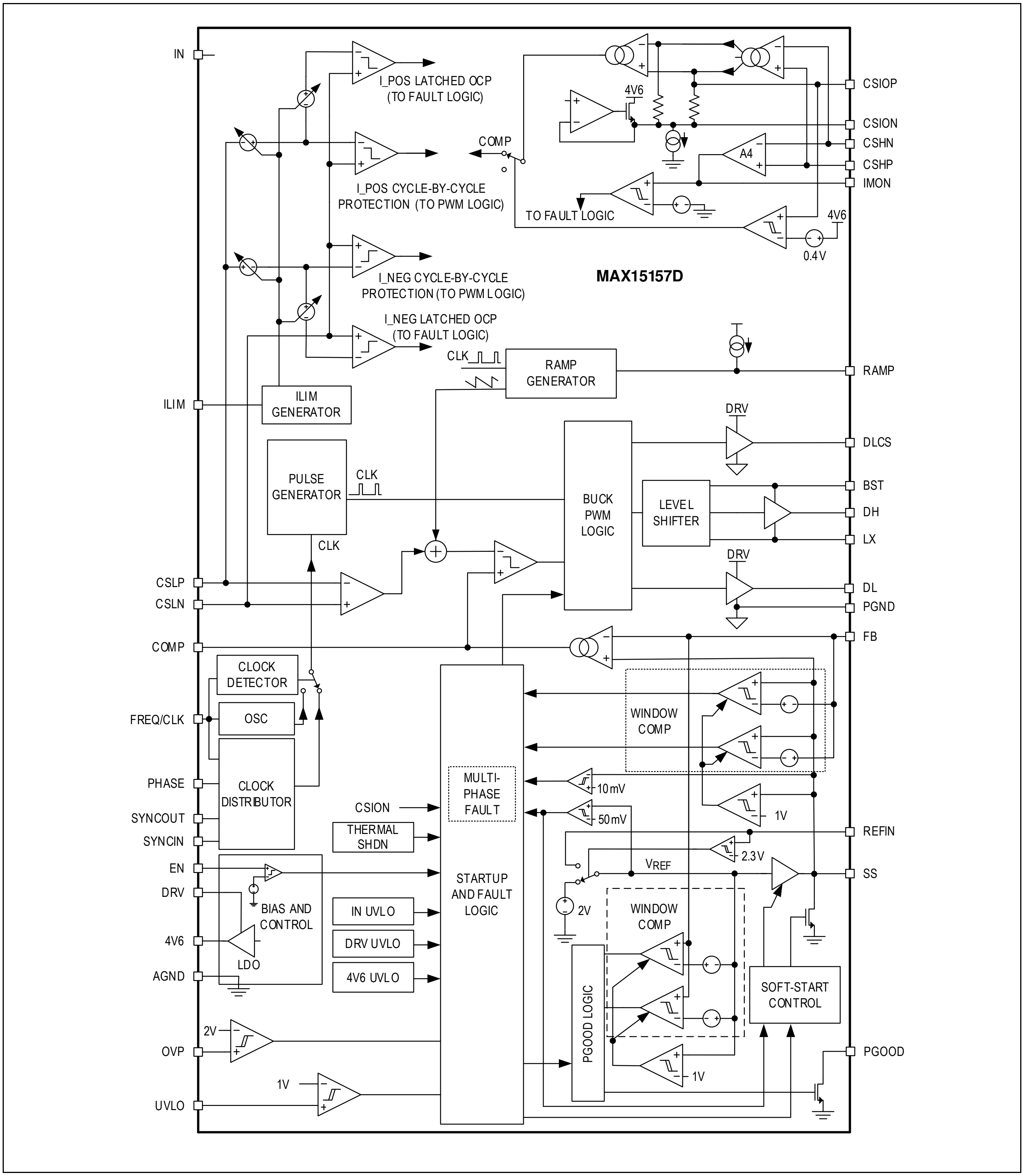


Pin Descriptions

PIN	NAME	FUNCTION
1	IN	Primary Input Supply. Connect IN to the 8V to 60V high-voltage system supply used to deliver power to the step-down power stage. IN serves as the system supply for the current-monitor amplifier and provides input undervoltage sensing.
2	UVLO	Adjustable Undervoltage-Lockout Input. When the UVLO voltage is below 0.9V, the device disables the controller. Connect UVLO to the center of a resistive-divider between the input and ground to adjust the undervoltage-lockout voltage, as shown in the *Standard Application Circuit*.
3	CSLP	Positive Low-Side Differential Current-Sense Input. The device uses the CSL_ differential current-sense signal in the current-mode control loop. See the *Standard Application Circuit* for CSLP connection.
4	CSLN	Negative Low-Side Differential Current-Sense Input. The device uses the CSL_ differential current-sense signal in the current-mode control loop. See the *Standard Application Circuit* for CSLN connection.
5	PHASE	Synchronized Phase Selection. Leave floating for single-phase operating or see *Table 1* for multiphase settings.
6	FREQ/CLK	Frequency Selection/Clock Synchronization Input. The device supports switching frequencies between 60kHz to 1MHz. Set the switching frequency by either selecting the appropriate external resistor to use the internal oscillator frequency, or by synchronizing the regulator to an external system clock (see *Table 1*). Leave FREQ/CLK unconnected to select the preset 300kHz switching frequency. For multiphase applications, FREQ/CLK serves as the master clock input.
7	SYNCIN	Synchronization Input/Clock Output for Multiphase Configurations. Connect SYNCIN to the SYNCOUT signal of the previous phase for multiphase synchronization. For the master phase, SYNCIN serves as the master clock output and should be connected to the FREQ/CLK input of all the power-stage phases (see *Figure 5*).
8	SYNCOUT	Multiphase Synchronization Output. Connect to the next phase when used in multiphase configurations (see *Figure 5*). For single-phase operation, leave SYNCOUT unconnected.
9	PGOOD	Open-Drain Power-Good Output. The device pulls PGOOD low when the output voltage exceeds the OVP threshold, or below the output undervoltage-protection threshold, during soft-start and shutdown (EN pulled low). The PGOOD output goes high impedance when the controller completes soft-start and remains in regulation.

		In multiphase operation, the PGOOD output of the slave ICs is always pulled low; do not tie the PGOOD output of the slave ICs and master IC together. Use the PGOOD output of the master IC for the system sequencing, if needed.
10	SS	Soft-Start Control. The capacitance (C_{SS}) between SS and AGND sets the startup period. An internal pulldown MOSFET holds SS low until the controller begins the startup sequence.
11	REFIN	External Reference Input. REFIN sets the feedback regulation voltage when supplied with a voltage between 0.4V and 2.2V. Operation between 0.4V < REFIN < 1V is possible, but the FB_OV and FB_UV fault functions are disabled.
12	COMP	Compensation Amplifier Output. COMP is the output of the internal transconductance error amplifier. Connect a Type II compensation network, as shown in *Figure 2*.
13	FB	Feedback Input. Connect FB to the center of a resistive-divider between the output and AGND. FB regulates to the preset 2V feedback threshold (REFIN = 4V6), or tracks the REFIN voltage (REFIN between 0.4V and 2.2V). Operation between 0.4V < REFIN < 1V is possible, but the FB_OV and FB_UV fault functions are disabled.
14	EN	Enable Control Input. Pull EN below 0.54V to place the device into its low-power shutdown state. When disabled, the controller pulls PGOOD low, pulls all the driver outputs low, and turns off the bias regulator.
15	CSION	Negative Input of Multiphase Current-Sense Signal. The device uses a differential current-sense signal to ensure proper startup and current-balance behavior in multiphase configurations.
16	CSIOP	Positive Input of Multiphase Current-Sense Signal. The device uses a differential current-sense signal to ensure proper startup and current-balance behavior in multiphase configurations.
17	IMON	High-Side Current-Sense Amplifier Output. IMON amplifies the voltage sensed from CSHP to CSHN.
18	CSHP	Positive High-Side Differential Current-Sense Input. See the *Standard Application Circuit* for CSHP connection. The controller amplifies this differential signal to generate the IMON current-monitor output voltage.
19	CSHN	Negative High-Side Differential Current-Sense Input. See the *Standard Application Circuit* for CSHN connection. The controller amplifies this differential signal to generate the IMON current-monitor output voltage.
20	OVP	Adjustable Output Overvoltage-Protection Threshold. Connect OVP to the center of an external resistive-divider network between the output and AGND to set the output overvoltage-protection limit.
21	4V6	4.6V Linear Regulator Output and Controller Bias Supply. Bypass to AGND with a 2.2μF or greater ceramic capacitor.
22	DRV	Driver Supply Voltage Input. Provides a 5.6V to 14V supply to power the low-side MOSFET gate drivers.
23	AGND	Analog Ground
24	RAMP	Slope Compensation Input. A resistor connected from RAMP to AGND programs the amount of slope compensation. See the *Adjustable Slope Compensation* section.
25	ILIM	Adjustable CSLP-CSLN Cycle-by-Cycle/Hiccup Current-Limit Threshold. Leave floating for internal current-limit threshold or connect a resistor from ILIM to AGND to program the adjustable current-limit threshold.
26	NC	Not Connected
27	DLCS	External Low-Side Cascode MOSFET Gate Driver. DLCS switches between DRV and PGND.
28	PGND	Power Ground. Connect PGND directly to the system ground plane.
29	DL	External Low-Side MOSFET Gate Driver. DL switches between DRV and PGND.
30	LX	Inductor Switch Node
31	BST	Boost Flying-Capacitor Connection. BST serves as the supply for the high-side driver. Connect to a Schottky diode from DRV to BST and an external 0.22nF, 25V ceramic capacitor between BST and LX, as shown in the *Standard Application Circuit*.
32	DH	External High-Side MOSFET Gate Driver. DH switches between BST and LX. The controller pulls DH low whenever the controller is disabled.
—	EP	Exposed Pad. Connect EP to AGND.

Block Diagram



Detailed Description

The MAX15157D fixed-frequency, current-mode PWM controller drives two power MOSFETs in buck configuration, allowing the regulator to operate as a step-down regulator.

The switching frequency is controlled either through an external resistor setting the internal oscillator frequency, or by synchronizing the regulator to an external clock. The device is designed to support 60kHz to 1MHz switching frequencies.

The controller has a dedicated input undervoltage-lockout input (UVLO) and an accurate enable-input threshold for flexible power-sequence configuration. The regulator also has multiple fault-protection circuits to protect against overcurrent, output overvoltage, output undervoltage, and thermal shutdown. The MAX15157D monitors CSHN and latches off immediately when the voltage exceeds 65V.

Current-Mode Control Loop

The controller relies on a fixed-frequency, current-mode architecture to regulate the output. Using two MOSFETs and a single inductor, the buck configuration shown in the *Typical Application Circuit* allows the controller to regulate output voltages below the input voltage. The control loop uses a valley current-mode architecture to optimize low duty cycle performance and provide the shortest possible minimum on-time.

On each clock edge, the controller drives on the low-side MOSFET (DL driven high). When the PWM comparator detects that the amplified low-side, current-sense signal (CSLP to CSLN) and slope compensation have fallen below the COMP voltage, the controller pulls DL low and drives DH high.

Driver Supply (DRV)

The MAX15157D requires an input supply and an external driver supply. The MOSFET drivers require a 5.6V to 14V supply capable of supporting the supply current needed to drive the MOSFETs. The power loss through an internal linear regulator would be significant, so the driver supply typically comes from the regulated 12V system supply. The maximum current required is determined by the switching frequency (f_{SW}) and gate-charge of each MOSFET (Q_G):

$$I_{DRV} = 2 \times f_{SW} \times Q_G$$

Bias Regulator (4V6)

The controller includes an internal linear regulator that generates a regulated 4.6V bias supply to power the internal analog and digital control circuitry. Bypass the regulator with a 1μF or greater ceramic capacitor to maintain noise immunity and stability. The DRV input supply powers the 4V6 linear regulator to reduce the power loss, as shown in the *Block Diagram*. The 4V6 bias regulator provides up to 30mA of load current, and the controller requires up to 5mA. The remaining current capability can be used to support pullup resistors.

The 4V6 linear regulator and internal reference power up only when DRV exceeds its undervoltage-lockout threshold and EN is driven high.

Input Undervoltage Lockout

The controller has input undervoltage-lockout thresholds on IN and DRV. The undervoltage-protection circuits inhibit switching until IN and DRV rise above their respective undervoltage thresholds.

If either supply drops below its undervoltage threshold, the controller determines the insufficient supply voltage to make valid control decisions. To protect the regulator and the output, the controller immediately pulls PGOOD low, disables the drivers (all driver outputs pulled low), and discharges the SS capacitor through an internal 5Ω discharge MOSFET, placing the regulator into a high-impedance output state. Hence, the output capacitance passively discharges through the load current.

Undervoltage-Lockout Pin (UVLO)

The external UVLO sense pin allows the input voltage operating range to be externally adjusted for power-sequence control. The input power source (IN) or driver supply (DRV) can be monitored. As long as UVLO exceeds and remains above 1V, the controller will power up and stay active. Once UVLO drops below 0.9V (typ), the controller pulls PGOOD low, disables the drivers (all driver outputs pulled low), and discharges the SS capacitor through an internal 5Ω discharge MOSFET.

The system can use the UVLO input as an auxiliary enable control pin; however, the controller remains powered (linear regulator and control circuitry biased) as long as the primary EN input remains high. Since the UVLO detection places the regulator into a high-impedance output state, the output capacitance passively discharges through the load current.

UVLO has a 6V absolute maximum voltage rating. Do not connect it directly to the high-voltage input power or driver supplies; short UVLO to the 4V6 bias supply if unused.

Soft-Start/Shutdown

The controller begins the startup sequence when both IN and DRV exceed their undervoltage-lockout thresholds and after EN is driven high. With the controller enabled, the bias regulator and internal reference power up. Once the reference stabilizes, the regulator checks the UVLO input to determine if it exceeds 1V, checks the PHASE configuration, and determines if any preset settings are selected. The controller pulls SS low through a 5Ω discharge MOSFET during this initialization period.

The regulator charges the SS capacitor with a constant 5µA current source until the SS voltage reaches the preset 2V target voltage (REFIN = 4V6) or the externally driven REFIN voltage (V_{REFIN} = 0.4V to 2.2V). The drivers start switching once SS exceeds 50mV, and the controller detects that FB voltage is below the SS voltage. The controller enables the fault-protection circuitry when SS exceeds 1V.

Once EN drops below 0.54V or UVLO drops below 0.9V, the controller pulls SS low, stops switching, and enters a low-power shutdown state.

Adjustable Slope Compensation (RAMP)

When the MAX15157D operates at a duty cycle of less than 50%, additional slope compensation is required to prevent the subharmonic instability that occurs naturally in valley-current-mode-controlled converters.

The MAX15157D provides RAMP input to select the internal compensation ramp within 380mV to 1200mV.

By connecting a resistor (R_{RAMP}) between RAMP and AGND, internal compensation ramp voltage V_{RAMP} is calculated as follows:

$$V_{RAMP} = 3.18 \times I_{RAMP} \times R_{RAMP}$$

where I_{RAMP} is the current sourced from RAMP to AGND (6µA, typ).

To guarantee stable, jitter-free operation, select R_{RAMP} so that:

$$R_{RAMP} \geq \frac{A_{CSL} \times R_{SENSE} \times V_{IN(MAX)}}{3.18 \times I_{RAMP} \times f_{SW} \times L}$$

where:

$V_{IN(MAX)}$ = Maximum input voltage

A_{CSL} = Current-sense amplifier gain (4.2V/V, typ)

R_{SENSE} = Value of equivalent current-sense resistor between CSLP and CSLN

f_{SW} = Switching frequency

L = Value of inductor

Switching Frequency (FREQ/CLK)

The controller supports 60kHz to 1MHz switching frequencies. Leave FREQ/CLK unconnected to select the preset 300kHz switching frequency. To adjust the switching frequency, place an external resistor from FREQ/CLK to AGND or drive FREQ/CLK with an external system clock (see Table 1). The resistively programmable switching frequency is determined by:

$$f_{SW} = \frac{R_{FREQ}}{R_{INT}} \times 600kHz$$

where R_{INT} is an internal parameter that depends on the number of phases selected (see Table 1).

Multiphase Synchronization

The MAX15157D can be configured in single-phase or multiphase operation by selecting the resistor at the PHASE pin. The PHASE setting communicates the master SYNCIN signal frequency and the clock count needed to set out-of-phase operation. See Table 1 and Figure 5 for the R_{PHASE} (1% tolerance resistor) selection and the phase shift of each phase. R_{INT} in Table 1 is an internal parameter that used to set the switching frequency.

For proper synchronization between phases in a multiphase configuration, the SYNCIN of the master device acts as a master clock. Connect this SYNCIN output to the FREQ/CLK signals of all the slave devices (see *Figure 5*).

Additionally, the interleaved phase control is communicated by connecting the SYNCOUT signal to the SYNCIN input of the next phase (see *Figure 5*). The daisy-chained signal ensures that the phases run out of phase.

Table 1. PHASE Configuration

	U1-MASTER	U2-SLAVE	U3-SLAVE	U4-SLAVE	U5-SLAVE	U6-SLAVE	U7-SLAVE	U8-SLAVE	N_{PHASE}	R_{INT}	f_{CLK}
R_{PHASE}	270kΩ	—	—	—	—	—	—	—	1-Phase	100kΩ	2 × f_{SW}
Phase Shift	0°	—	—	—	—	—	—	—			
R_{PHASE}	133kΩ	133kΩ	—	—	—	—	—	—	2-Phase	100kΩ	2 × f_{SW}
Phase Shift	0°	180°	—	—	—	—	—	—			
R_{PHASE}	169kΩ	169kΩ	169kΩ	—	—	—	—	—	3-Phase	112kΩ	6 × f_{SW}
Phase Shift	0°	120°	240°	—	—	—	—	—			
R_{PHASE}	210kΩ	210kΩ	210kΩ	210kΩ	—	—	—	—	4-Phase	108kΩ	4 × f_{SW}
Phase Shift	0°	90°	180°	270°	—	—	—	—			
R_{PHASE}	169kΩ	169kΩ	169kΩ	68kΩ	68kΩ	68kΩ	—	—	6-Phase	112kΩ	6 × f_{SW}
Phase Shift	0°	120°	240°	60°	180°	300°	—	—			
R_{PHASE}	210kΩ	210kΩ	210kΩ	210kΩ	100kΩ	100kΩ	100kΩ	100kΩ	8-Phase	108kΩ	4 × f_{SW}
Phase Shift	0°	90°	180°	270°	45°	135°	225°	315°			

Multiphase Current-Balance (CSIO_)

The device uses the differential CSIO_ connection at startup to configure the multiphase configuration. Once this configuration period is complete, the differential interconnect communicates the average per-phase current of each regulator. The current-mode slave devices regulate their current so that all phases share the output load.

MOSFET Gate Drivers

The MAX15157D uses 12V gate drivers optimized for driving the 80V power MOSFETs required for a typical high-voltage application. The drivers use a 2Ω pullup and 0.6Ω pulldown to turn on and off the MOSFETs quickly. These strong gate drivers support high-frequency operation and minimal on-time/off-time periods.

The regulator powers the DH high-side drivers by BST and LX. When switching, the BST voltage is determined by the charge-pump circuit formed by the DRV-to-BST high-voltage Schottky diode, BST-to-LX capacitor, and low-side MOSFET. The Schottky diode should be rated at $V_{IN(MAX)}$ + 30V.

Adaptive dead-time circuits monitor the DL-to-DH drivers, preventing either driver from turning on its MOSFET until the other MOSFET has fully turned off. The adaptive shoot-through protection allows robust operation with a wide range of MOSFETs while minimizing dead-time power losses. The layout must provide a low-resistance, low-inductance path between the driver outputs and the MOSFET gates for the adaptive dead-time circuits to function correctly. Otherwise, the sense circuitry in the controller interprets the MOSFET gates as “off” while the charge remains.

To support lossless current sense, the MAX15157D integrates a dedicated gate driver, DLCS, to drive the external current-sense cascode MOSFET, as shown in the *Standard Application Circuit*.

Hiccup Fault Protection

The MAX15157D features multiple hiccup-protection features (e.g., overcurrent protection, CSH_ overvoltage protection, and thermal shutdown) that trigger an autorestart of the regulator. The regulator disables the drivers (all driver outputs pulled low) and discharges the SS capacitor through a 5Ω pulldown MOSFET when any protection event is triggered. After 32,768 clock cycles, the regulator automatically restarts using the soft-start sequence.

Overcurrent Protection (OCP)

The MAX15157D detects the current-sense signal (CSLP to CSLN) and compares it with the cycle-by-cycle current-limit threshold during low-side on-time. The high-side switch turn-on is paused when the current exceeds the cycle-by-cycle current-limit threshold until the current falls below the threshold falling level.

A resistor sets the cycle-by-cycle current-limit threshold at the ILIM pin. A 10μA source current flows into the resistor and generates a voltage level in the 0.35V to 1.95V range. This voltage level is internally scaled to set the cycle-by-cycle current limit threshold (V_{OCP}), which is given by:

$$V_{OCP} = 0.06504 \times 10\mu A \times R_{ILIM}$$

When the ILIM pin voltage is found outside the 0.35V to 1.95V range, an internal 0.615V reference voltage is used to set the ILIM threshold.

The maximum output current (I_{LIM}) allowed by the cycle-by-cycle current-limit threshold is given by:

$$I_{LIM} = \frac{V_{OCP}}{R_{SENSE}} + \frac{\Delta I_L}{2}$$

where ΔI_L is the peak-to-peak inductor ripple current, and R_{SENSE} is the equivalent current-sense resistor between CSLP and CSLN. As shown in the *Standard Application Circuit*, with low-side resistor current-sense:

$$R_{SENSE} = R_S 1$$

and with lossless, low-side MOSFET R_{DSON} current-sense:

$$R_{SENSE} = \frac{R29}{R28 + R29} \times R_{DSON\_LSFET}$$

The device also has a negative overcurrent protection threshold, which is -100% of the cycle-by-cycle current-limit threshold set by R_{ILIM}.

Integrated High-Side Current Monitor (IMON)

The controller also includes a high-side current-sense amplifier. The current-monitor output generates a voltage equivalent to 50 times the differential CSHP-to-CSHN voltage. The current-sense amplifier only functions in a single quadrant, so the controller only monitors current sourced to the output (*Figure 1*).

The IMON output is compared with a 2.5V threshold ($V_{OCP(AVE)}$). Once the V_{IMON} exceeds $V_{OCP(AVE)}$ more than 32 consecutive clock cycles, the part enters hiccup mode (see *Figure 1*).

The maximum output current (I_{LIM}) allowed by $V_{OCP(AVE)}$ threshold is given by:

$$I_{LIM} = \frac{V_{OCP(AVE)}}{50 \times R_{SENSE\_H}}$$

where R_{SENSE_H} is the equivalent current-sense resistor between CSHP and CSHN.

With the high-side resistor current-sense shown in *Figure 1*:

$$R_{SENSE\_H} = R_S 2$$

and with the lossless low-side MOSFET $R_{DS(ON)}$ current-sense shown in the *Standard Application Circuit*:

$$R_{\mathrm{SENSE\_H}} = \frac{R14}{R14 + R30 + R33} \times R_{DSON_{LS}\ FET} \times (1 - D)$$

where D is the duty cycle.

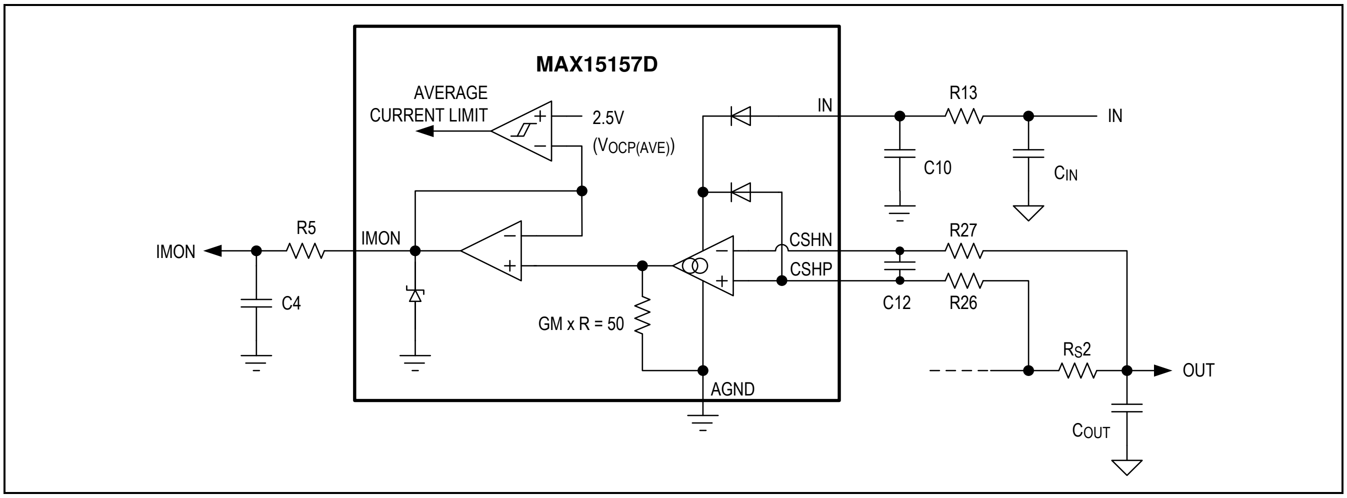


Figure 1. High-Side Output Current Monitor

Undervoltage Protection (UVP)

The device monitors the FB voltage for an output undervoltage-fault condition. If the feedback voltage drops 9% (typ) below the SS voltage for at least 32 clock cycles, the controller discharges the SS capacitor and turns off the drivers. The controller immediately restarts once the fault condition has been removed.

Overvoltage Protection (OVP)

The MAX15157D has three separate OVP comparators: the first monitors the FB voltage, the second monitors the high-side current-sense input (CSHN), and the third monitors the independent OVP input. The FB overvoltage comparator trips if the feedback voltage exceeds the SS voltage by 9% (typ) for more than 32 clock cycles. The CSH_ overvoltage comparator trips if the current-sense voltage exceeds 65V, which is the operating limit of the regulator and current-sense amplifier. Finally, the OVP comparator trips if it exceeds 2V.

To set the independent OVP input, connect the OVP pin to the center tap of an external resistor-divider from the output to AGND, as shown in the *Standard Application Circuit*, then the output overvoltage threshold (V_{OUT_OVP}) is given by:

$$V_{OUT\_OVP} = \frac{R24 + R25}{R24} \times 2V$$

When the independent OVP input is not used, short the OVP pin to AGND. Alternatively, the OVP input can monitor the input supply.

Thermal Shutdown (T_{SHDN})

The controller features a thermal fault-protection circuit. When the junction temperature rises above +165°C, the internal thermal sensor triggers the hiccup-fault protection, disables the drivers, and discharges the SS capacitor. The controller remains disabled until the junction temperature cools by 15°C. Once the device has cooled down, and at least 32,768 clock cycles have expired, the controller automatically restarts using the soft-start sequence.

Inductor Selection

The output inductor is selected based on the desired amount of inductor ripple current. A large inductance value minimizes output ripple current and increases efficiency, but slows down the current slew rate during a load transient. LIR is the ratio of inductor ripple current to the total current per phase. A LIR of 20% to 40% is recommended for the best efficiency and transient response tradeoff. A higher LIR could be selected to take advantage of ripple current cancellation in a multiphase operation. Choose the inductor as follows:

$$L = \frac{V_{OUT} \times (1 - D) \times N}{LIR \times I_{LOAD(MAX)} \times f_{SW}}$$

where:

f_{SW} = Switching frequency

$I_{LOAD(MAX)}$ = Maximum output current

V_{OUT} = Output voltage

D = Duty cycle (V_{OUT}/V_{IN})

N = Number of phases

The selected inductor should have low DC resistance, and the saturation current should be greater than the peak inductor current (I_{PEAK}), which is calculated by:

$$I_{PEAK} = \frac{I_{LOAD(MAX)}}{N} \times \left(1 + \frac{LIR}{2}\right)$$

Output Capacitor Selection

The output capacitors are selected to improve stability, output voltage ripple, and load-transient performance. Select the output capacitor to satisfy the load-transient requirements:

$$C_{OUT} \geq \frac{\Delta I_{LOAD}}{3 \times f_{CO} \times \Delta V_{OUT}}$$

where:

ΔI_{LOAD} = Load current step

f_{CO} = Control-loop crossover frequency

ΔV_{OUT} = Desired output voltage overshoot or undershoot

Input Capacitor Selection

The input capacitor reduces peak current drawn from the power source and reduces noise and voltage ripple on the input caused by the switching circuitry. The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching current as defined by:

$$I_{RMS} = I_{LOAD(MAX)} \times \sqrt{\left(D - \frac{floor(N \times D)}{N}\right) \times \left(\frac{1 + floor(N \times D)}{N} - D\right)}$$

where:

$I_{LOAD(MAX)}$ = Maximum output current

D = Duty cycle (V_{OUT}/V_{IN})

N = Number of phases

and floor (N×D) returns the largest integer smaller than or equal to (N×D).

To keep the input ripple voltage (V_{IN_RIPPLE}) within the specification and minimize the high-frequency ripple current being fed back to the input source, the input capacitance per phase (C_{IN_PHASE}) should be greater than the value calculated by:

$$C_{IN\_PHASE} = \frac{D \times (1 - D) \times I_{LOAD(MAX)}}{\eta \times V_{IN\_RIPPLE} \times f_{SW} \times N}$$

where η is the efficiency of the converter.

Compensation Design

The MAX15157D utilizes a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor. The current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor, resulting in a smaller phase shift and requiring a less elaborate error-amplifier compensation than voltage-mode control.

The MAX15157D uses an internal transconductance error amplifier, which has an output that compensates the control loop. As shown in *Figure 2*, a Type II compensation network connected between COMP and AGND is needed to provide sufficient phase and gain margins. Generally, the crossover frequency (f_{CO}) is selected at 1/10 of the switching frequency, the error amplifier compensation zero generated by R_C and C_C is placed at the modulator pole f_{pMOD}, and the error amplifier compensation pole determined by R_C and C_F is placed at the modulator zero f_{zMOD}, as shown in *Figure 3*. Then, the value of the compensation network can be approximately calculated by the following equations:

$$R_C = \frac{2 \times \pi \times f_{CO} \times C_{OUT} \times A_{CSL} \times R_{SENSE}}{G_{MEA} \times \frac{V_{REF}}{V_{OUT}} \times N}$$

$$C_C = \frac{R_{LOAD} \times C_{OUT}}{R_C}$$

$$C_F = \frac{ESR \times C_{OUT}}{R_C}$$

where:

A_{CSL} = Current-sense amplifier gain (4.2V/V, typ)

R_{SENSE} = Value of equivalent current-sense resistor between CSLP and CSLN

N = Number of phases

G_{MEA} = Error-amplifier transconductance (1.1mS, typ)

V_{REF} = Internal reference voltage set by REFIN pin

R_{LOAD} = V_{OUT}/I_{OUT}, output load resistance

V_{OUT} = Output voltage

C_{OUT} = Total output capacitance

ESR = Equivalent series resistance of C_{OUT}

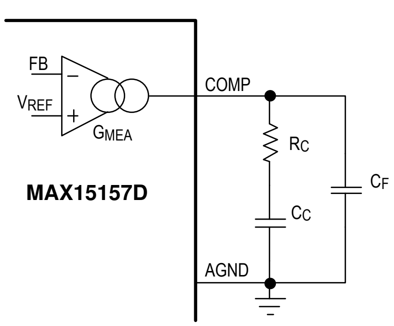


Figure 2. Type II Compensation Network

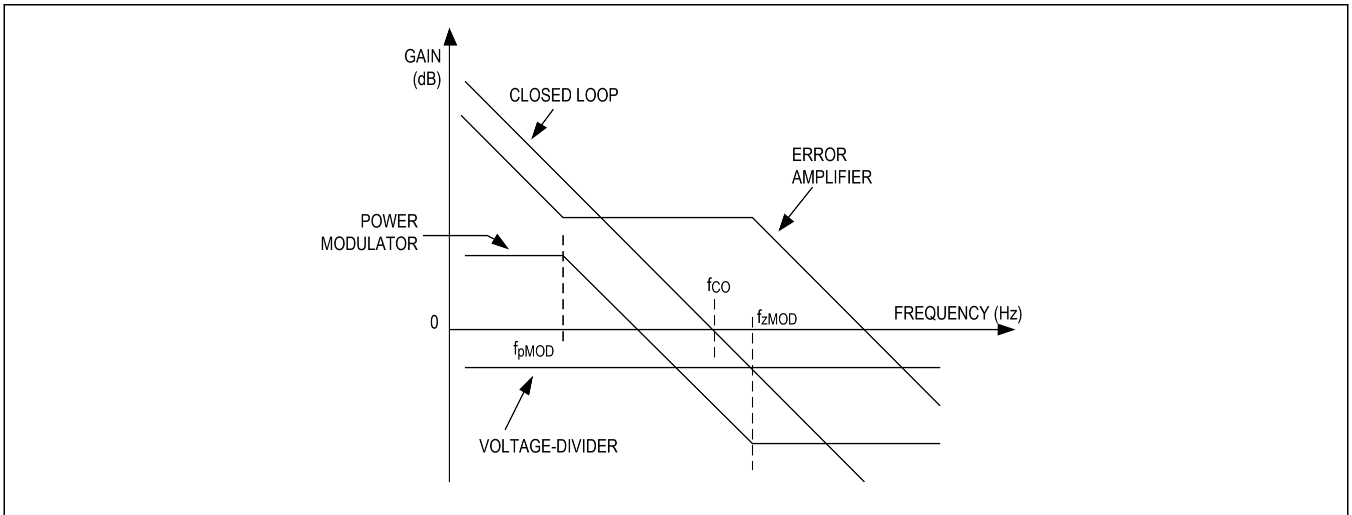


Figure 3. Simplified Gain Plot

PCB Layout

Component Placement (See the *Standard Application Circuit*)

Input and Output

Group the input power path components, capacitor (C_{IN}), switches M1 and M2, in a compact area.

The current path lengths of switches M1 and M2, and C_{IN} should be minimized as much as possible.

Place switch M2 as close as possible to the controller, keeping the PGND, DL, and SW traces short. Locate the current-sense circuits (Rs1 if used or M3, R28, and R29) as close as possible to M2 and the input and output capacitors.

The output capacitor (–) terminals should be located close to the (–) terminals of the input capacitor, forming an efficient ground star.

High dv/dt Device

Keep the high dv/dt LX, BST, and DH nodes away from sensitive small-signal nodes.

Control-Loop Component

The controller IC and its associated RC network should be located in the same PCB layer.

PCB Routing (See the *Standard Application Circuit*)

Input Trace

Use planes for input and output voltage to maintain good voltage filtering and keep power losses low. Route the traces as close as possible for the (+) and (–) terminals of the input and output capacitors.

Ground

Since PGND is part of the input and output (load) currents path, it is crucial to use enough vias to connect to the inner PGND layers. The same consideration applies to the input supply voltage.

Separate the signal and power grounds. All small-signal components should return to the AGND pin at one point, which is then tied to the PGND pin through R19 to (–) terminals of the input and output capacitors.

The second layer from the top and bottom should be reserved for contiguous GND planes (for electrical and thermal reasons). “Quiet GND” on the MAX15157D should be a contained shape right under the chip on one of the inner layers and be connected to other AGND at one point through a single via.

REFIN should be referred to the AGND and not to PGND. Any offset from PGND impacts voltage regulation accuracy.

Use immediate vias to connect the components (including the MAX15157D AGND and PGND pins) to the ground plane. Use multiple large vias for each power component.

High dv/dt and di/dt Loop

Locate the top driver bootstrap capacitor (C14) close to the IC BST and LX pins.

Locate the input and output capacitors close to the power MOSFETs. These capacitors carry the MOSFET AC/switching current.

Thermal

Add enough copper planes for each termination of the power inductor/MOSFET. The layout needs to meet the thermal current PCB guideline per the inductor/MOSFET specification.

Flood all unused areas on all layers with copper. Flooding with copper reduces the temperature rise of power components. Connect the copper areas to any DC net (V_{IN} or PGND).

Exposed Pad

The exposed pad (EP) works as a heatsink to dissipate the heat generated from the silicon power loss. It is crucial to provide a relatively quiet AGND to operate correctly. Connect EP to AGND. The exposed pad must be soldered evenly to the PCB ground plane for proper operation and best cooling using multiple vias beneath the exposed pad for maximum heat dissipation. A 1.0mm to 1.2mm pitch is the recommended spacing for these vias, and they should be plated (1oz copper) with a small barrel diameter (0.30mm to 0.33mm).

Multiphase Interconnections

The master and slaves are connected through multiple analog traces. Use the shortest direct path for these connections. Try to avoid layer changes.

Have a thick trace (or another long shape) going from the master “quiet GND” to all slaves. The master controller should share the same AGND with the slaves. For proper synchronization between phases in a multiphase configuration, connect the master device SYNCIN output to the FREQ/CLK pin of all of the slave devices. Couple the SYNCIN and SYNCOUT, CSIOP and CSION traces with AGND. Carefully arrange the AGND between phases to add no additional offset to the CSIO_ pins.

All traces should be routed from each slave together and away from any known sources of noise.

Keep the FREQ/CLK, SYNCIN, and SYNCOUT traces far away from the CSIO_ trace to avoid unnecessary noise coupling, using inner layers, to avoid cutting the power paths on the top and bottom layers.

CSIO_ traces should be routed away from the high current paths using internal layers shielded between AGND planes.

Standard Application Circuits

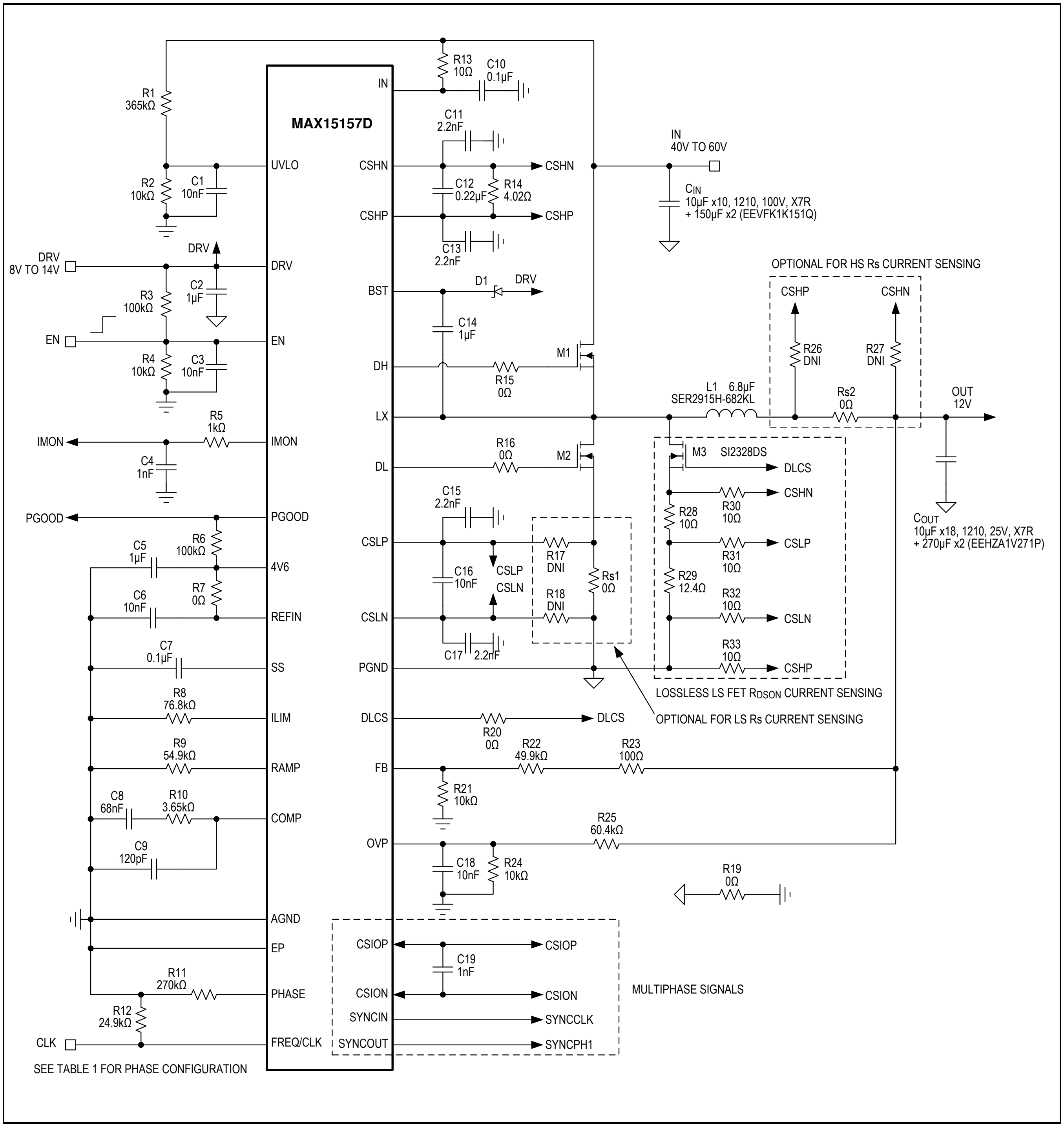


Figure 4. Single-Phase Buck Converter with Lossless LS FET R_{DSON} Current Sensing

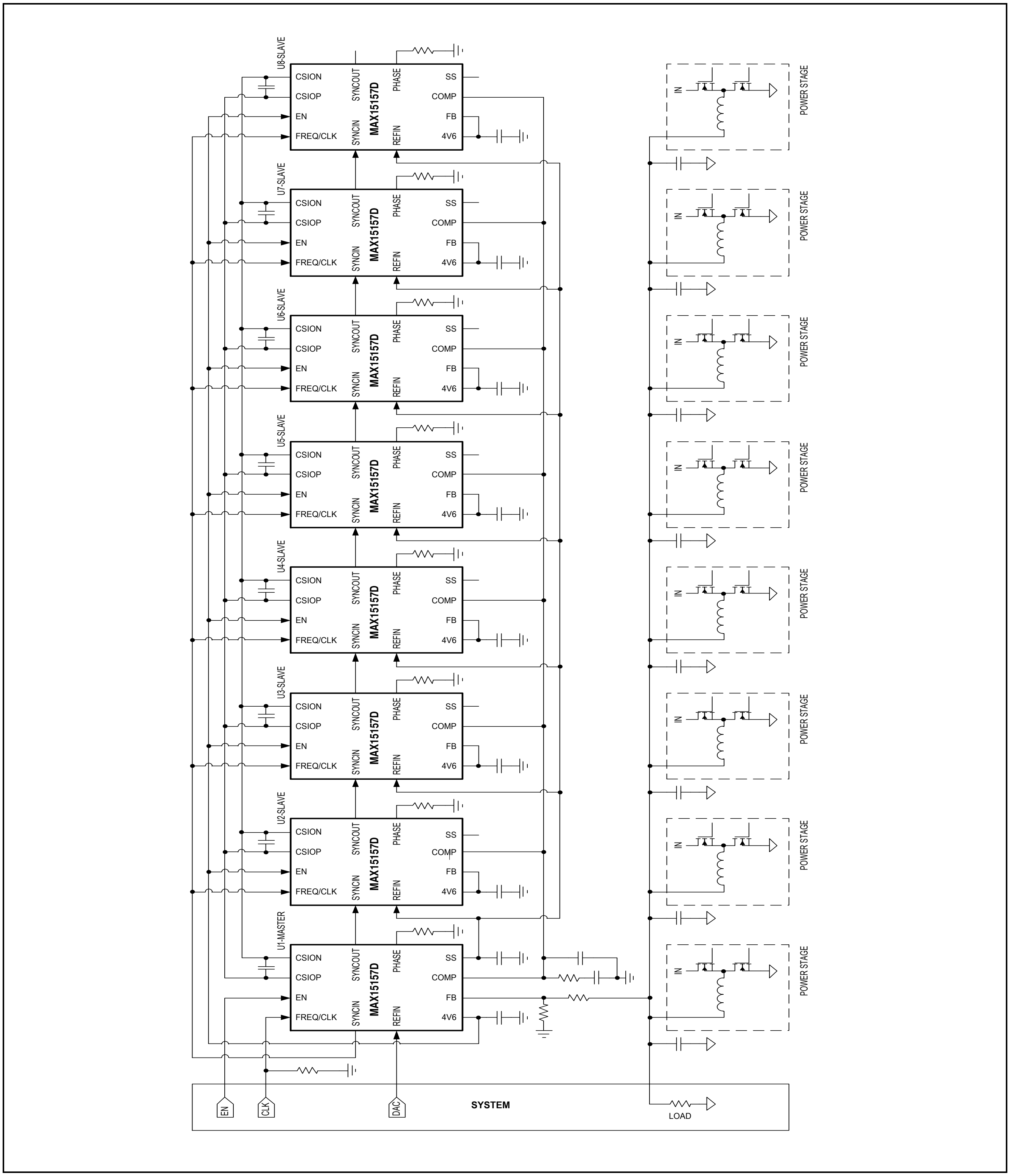


Figure 5. Multiphase Interconnects

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX15157DATJ+	-40°C to +125°C	32 TQFN-EP*
MAX15157DATJ+T	-40°C to +125°C	32 TQFN-EP*

+ Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/21	Initial release	—
1	1/22	Updated *Applications*, *Absolute Maximum Ratings*, *Electrical Characteristics*, *Pin Descriptions*, *Block Diagram*, and *Detailed Description*	1, 3, 5, 11–12, 13, 14–22