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Evaluation Board for the ADF4153A Fractional-N PLL Frequency Synthesizer

FEATURES

Self-contained evaluation board including synthesizer, VCO, TCXO for reference frequency, and loop filter
Designed for 25 MHz PFD frequency, 2.5 mA charge pump current, and 50 kHz loop bandwidth
Accompanying software allows complete control of synthesizer functions from a PC

EVALUATION KIT CONTENTS

EV-ADF4153ASD1Z board
CD that includes
- **Self-installing software that allows users to control the board and exercise all functions of the device**
- **Electronic version of the ADF4153A data sheet**
- **Electronic version of the UG-485 user guide**
- **Electronic version of the UG-476 user guide (PLL software installation procedure)**

ADDITIONAL EQUIPMENT

PC running Windows XP or more recent version
SDP-S board (system demonstration platform, serial only)
Spectrum analyzer
Oscilloscope (optional)

DOCUMENTS NEEDED

ADF4153A data sheet

REQUIRED SOFTWARE

ADI Frac-N PLL software (Revision 4.2.1 or higher)
ADIsimPLL

GENERAL DESCRIPTION

This evaluation board is designed to allow the user to evaluate the performance of the ADF4153A frequency synthesizer for phase-locked loops (PLLs). Figure 1 shows the board, which contains the ADF4153A synthesizer, an edge-mounted SMA connector for the RF output signal, power supply connectors, a temperature compensated reference oscillator (TCXO) of 25 MHz frequency, and an SDP connector. There is also a loop filter (50 kHz) and a VCO (Mini-Circuits ROS-1800+) on board.

The package also contains Windows® software (XP or later) to allow easy programming of the synthesizer.

This board requires a system demonstration platform-serial (SDP-S) board (not supplied with the kit). The SDP-S allows software programming of the ADF4153A device.

EVALUATION BOARD

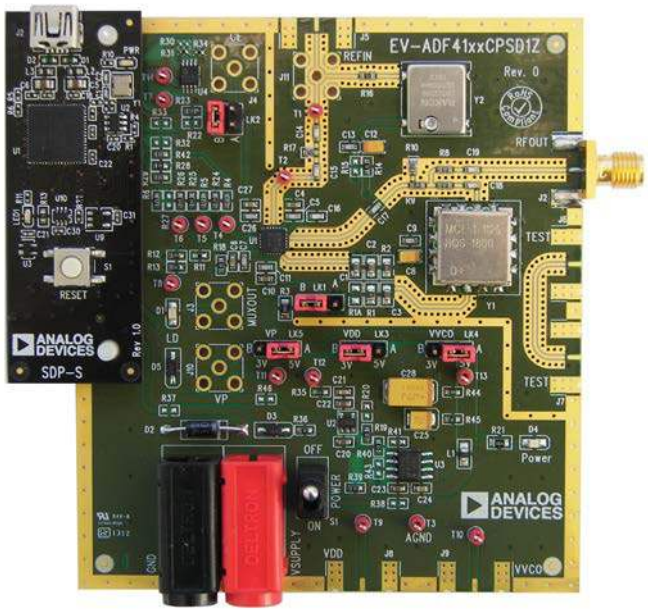

Figure 1. EV-ADF4153ASD1Z with SDP-S

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REVISION HISTORY

12/12—Revision 0: Initial Version

QUICK START GUIDE

Follow these steps to quickly evaluate the ADF4153A device:

1. Install the ADI Frac-N PLL software (see UG-476)
2. Connect the SDP-S motherboard to the EV-ADF4153ASD1Z and the PC.
3. Follow the hardware driver installation procedure when appears (Windows XP only).
4. Connect the power supplies to banana connectors (5.5 V).
5. Run the ADI Frac-N PLL software.
6. Select the **SDP board** and the ADF4153 device in the **Select Device and Connection** tab of the software front panel window. Note that ADF4153 and ADF4153A are software compatible.
7. Click the **Main Controls** tab and update all registers.
8. Connect the spectrum analyzer to J2.
9. Measure the results.

EVALUATION BOARD HARDWARE

The evaluation board requires the use of an SDP-S motherboard to program the device. This is not included and must be purchased separately. The EV-ADF4153ASD1Z schematics are shown in Figure 7, Figure 8, and Figure 9.

POWER SUPPLIES

The board is powered from external banana connectors. The voltage should be 5.5 V. The power supply circuit provides 3.0 V to V_{DD} on the board (which supplies the ADF4153A AV_{DD} and DV_{DD} pins) and allows the user to choose either 3.0 V or 5 V for the ADF4153A V_P. The default settings are 3.0 V for the ADF4153A V_{DD} and 5 V for the ADF4153A V_P. Note that V_{DD} should never exceed 3.3 V. This can damage the device.

External power supplies can be used to directly drive the device. In this case, the user must insert SMA connectors as shown in Figure 2.

INPUT SIGNALS

The necessary reference input comes from an on-board temperature compensated crystal oscillator (TCXO) of 25 MHz frequency.

Alternatively, this can be sourced from an external generator. In this case, remove R16 and R14 to disconnect the TCXO from the supply and from the reference path, insert Connector J11 or the edge mount connector, J5, and connect the external generator to the connector. A low noise, high slew rate reference source is best for achieving the stated performance of the ADF4153A.

Digital SPI signals are supplied through the SDP connector, J1. Using the SDP-S platform is recommended. The SDP-B can also be used, but Resistor R57 must be removed on the SDP-B board. Some additional spurious low frequencies may appear if the SDP-B connector is used.

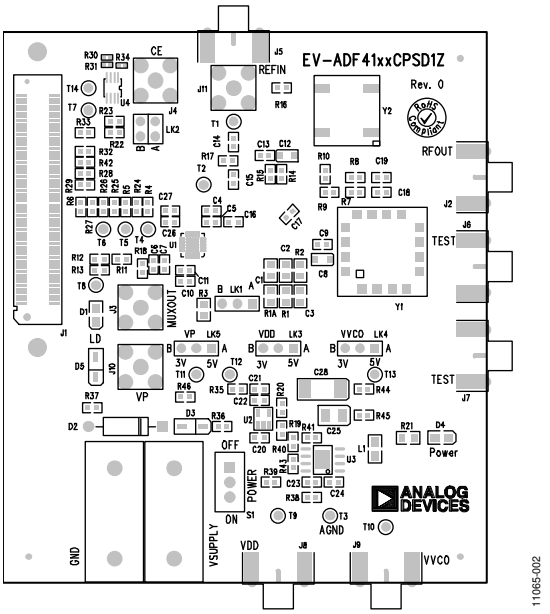

Figure 2. Evaluation Board Silkscreen

OUTPUT SIGNALS

All components necessary for LO generation are inserted on board. The PLL is made up of the ADF4153A synthesizer, a passive loop filter, and the VCO. This board is supplied with a VCO ROS1800+ from Mini-Circuits, which covers a frequency range from 1700 MHz to 1800 MHz. A low-pass filter of 50 kHz loop bandwidth is inserted between the charge pump output and the VCO input. The 2.5 mA charge pump current setting is used. The VCO output is available at RFOUT through a standard SMA connector, J2. The MUXOUT signal can be monitored at Test Point T8 or at SMA Connector J3.

DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

Link positions are detailed in Table 1.

Table 1. Link Positions and Functions

Link	Position	Options	Description
LK1	A	R1A	Not used
	B	RSET	Normal operation
LK2	A	GND	Not used
	B	VDD	Normal operation
LK3 (V_{DD})	A	5 V	Not used
	B	3 V	Normal operation
LK4 (V_{VCO})	A	5 V	VCO supply (5 V)
	B	3 V	VCO supply (3 V)
LK5 (V_P)	A	5 V	V_P supply (5 V)
	B	3 V	V_P supply (3 V)

SYSTEM DEMONSTRATION PLATFORM (SDP)

The system demonstration platform (SDP) is a series of controller boards, interposer boards, and daughter boards that can be used for easy, low cost evaluation of Analog Devices, Inc., components and reference circuits. It is a reusable platform whereby a single controller board can be reused in various daughter board evaluation systems.

Controller boards connect to the PC via USB 2.0 and provide a range of communication interfaces on a 120-pin connector. The pinout for this connector is strictly defined. This 120-pin connector's receptacle is on all SDP daughter boards, component evaluation boards, and Circuits from the Lab™ reference circuit boards. There are two controller boards in the platform: the SDP-B, which is based on the Blackfin® ADSP-BF527, and the SDP-S, which is a serial interface only controller board. The SDP-S has a subset of the SDP-B functionality.

Interposer boards route signals between the SDP 120-pin connector and a second connector. When the second connector is also a 120-pin connector, the interposer can be used for signal monitoring of the 120-pin connector signals. Alternatively, the second connector allows SDP platform elements to be integrated into a second platform, for example, the BeMicro SDK. More information on the SDP can be found at www.analog.com/sdp.

EVALUATION BOARD SOFTWARE

The control software for the EV-ADF4153ASD1Z accompanies the board on the CD included in the evaluation kit. To install the software, see UG-476 (the PLL Software Installation Guide).

To run the software, click the **ADI PLL Frac-N** file on the desktop or in the **Start** menu.

On the **Select Device and Connection** tab, choose ADF4153 and **SDP board (black)**, and click **Connect.**

Confirm that **SDP board connected** is displayed at the bottom left of the window (see Figure 3). Otherwise, the software has no connection to the evaluation board.

Note that, when connecting the board, it takes about 5 sec to 10 sec for the status label to change.

Under the **File** menu, the current settings can be saved to, and loaded from, a text file.

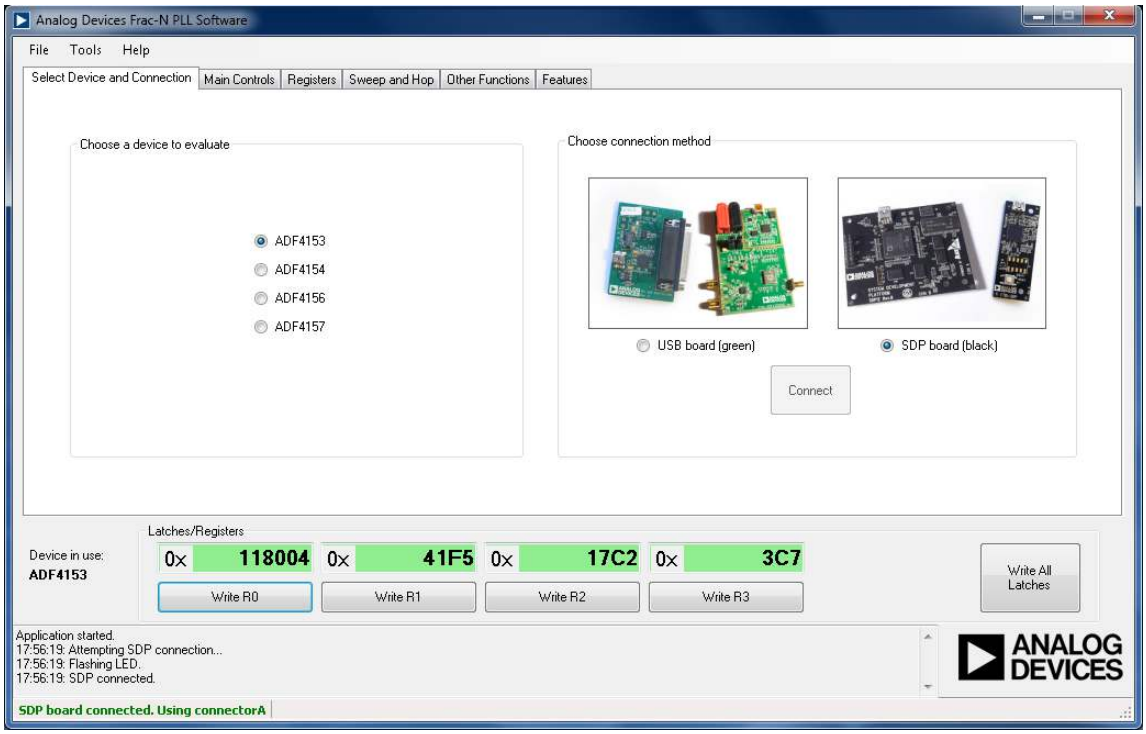

Figure 3. Software Front Panel Display—Select Device and Connection

The **Main Controls** tab controls the PLL settings (see Figure 4).

Use the **Reference Frequency** text box to set the correct reference frequency and the reference frequency divider. The default reference on the software window is at 25 MHz to match the on-board reference crystal oscillator.

Use the **RF Settings** section to control the output frequency. You can type the desired output frequency in the **RF VCO Output Frequency** text box (in megahertz).

In the **Registers** tab, you can manually input the desired value to be written to the registers.

In the **Sweep and Hop** tab, you can make the device sweep a range of frequencies or hop between two set frequencies.

In the **Latches/Registers** section at the bottom of the window, the values to be written to each register are displayed. If the background on the text box is green, the value displayed is different from the value actually on the device. Click **Write Rx** (where x = 0 to 3) to write that value to the device.

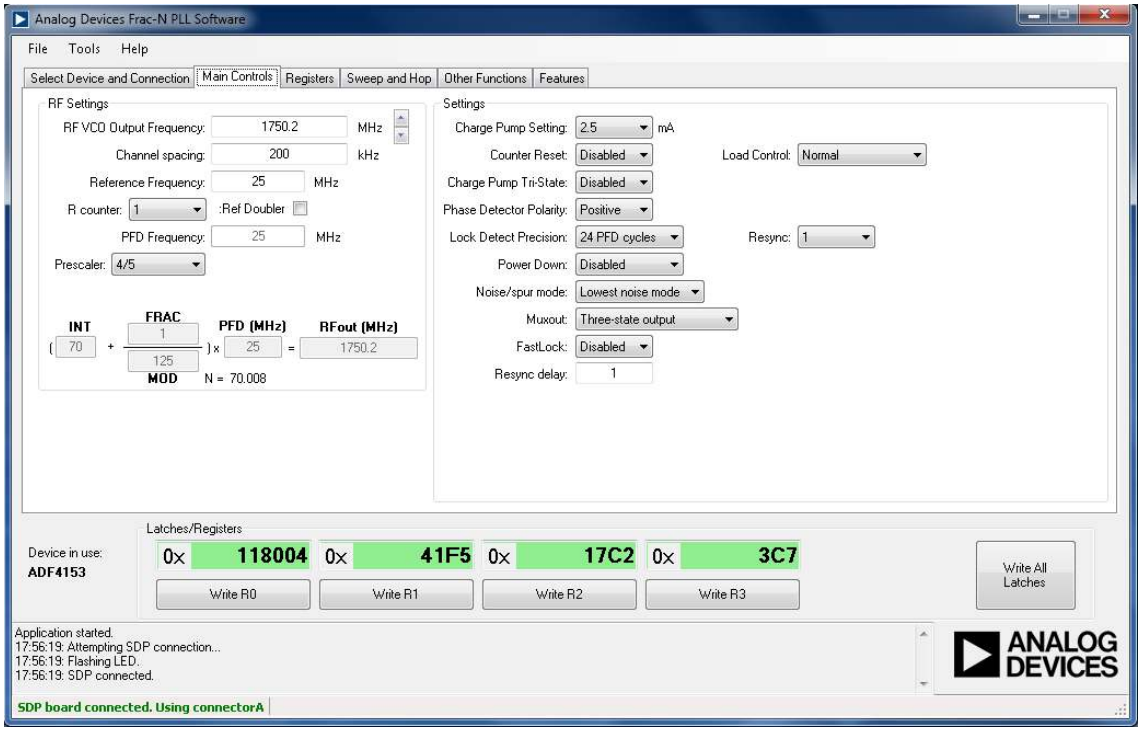

Figure 4. Software Front Panel Display—Main Controls

EVALUATION AND TEST

To evaluate and test the performance of the ADF4153A, use the following procedure:

1. Install the ADI Frac-N PLL software.
2. Connect the SDP-S connector to the EV-ADF4153ASD1Z.
3. Connect the evaluation board to a PC using the supplied USB cable.
4. Follow the hardware installation procedure that appears (Windows XP only).
5. Connect a spectrum analyzer to Connector J2.
6. Run the ADI Frac-N PLL software.
7. Select the **SDP board** and the **ADF4153** device in the **Select Device and Connection** tab of the software front panel window. Note that ADF4153 and ADF4153A are software compatible.
8. In the **Main Controls** panel, set the VCO center frequency, PFD frequency, and reference frequency. By default, VCO frequency is set to 1750.2 MHz (middle range of the Mini-Circuits ROS-1800+ VCO), and both reference frequency and PFD frequency are set to 25 MHz to match the frequency of the TCXO applied on board. The charge pump current should equal 2.5 mA. See Figure 6 for the suggested setup.
9. Measure the output spectrum. Figure 5 shows a screenshot of the signal source analyzer operating in phase noise mode, taken at a frequency of 1750.2 MHz.

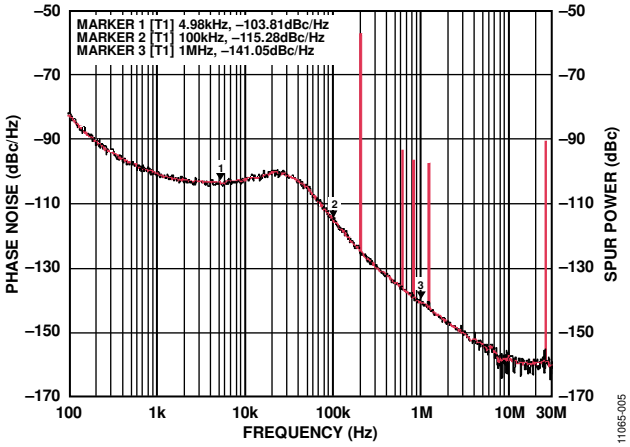

Figure 5. Spectrum Analyzer Display

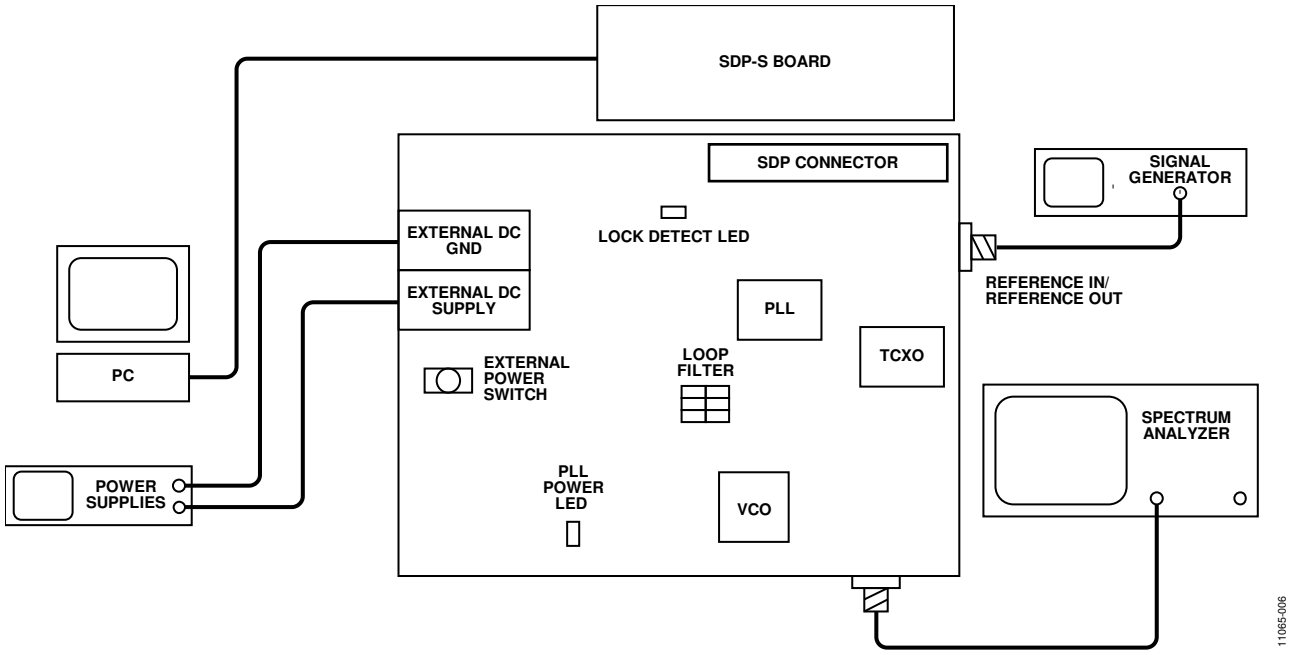

Figure 6. Typical Evaluation Setup

EVALUATION BOARD SCHEMATICS AND ARTWORK

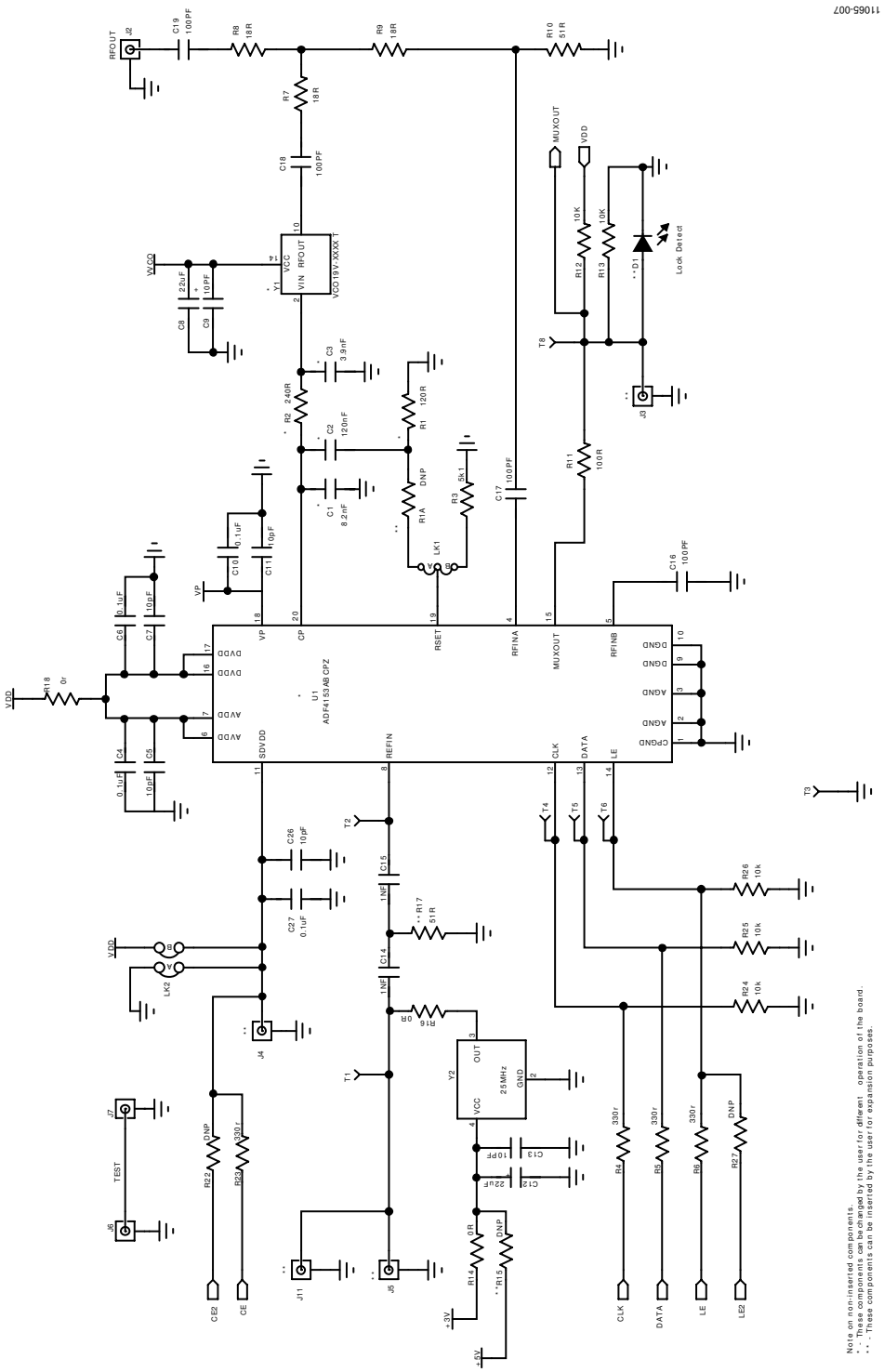

Figure 7. Evaluation Board Schematic (Page 1)

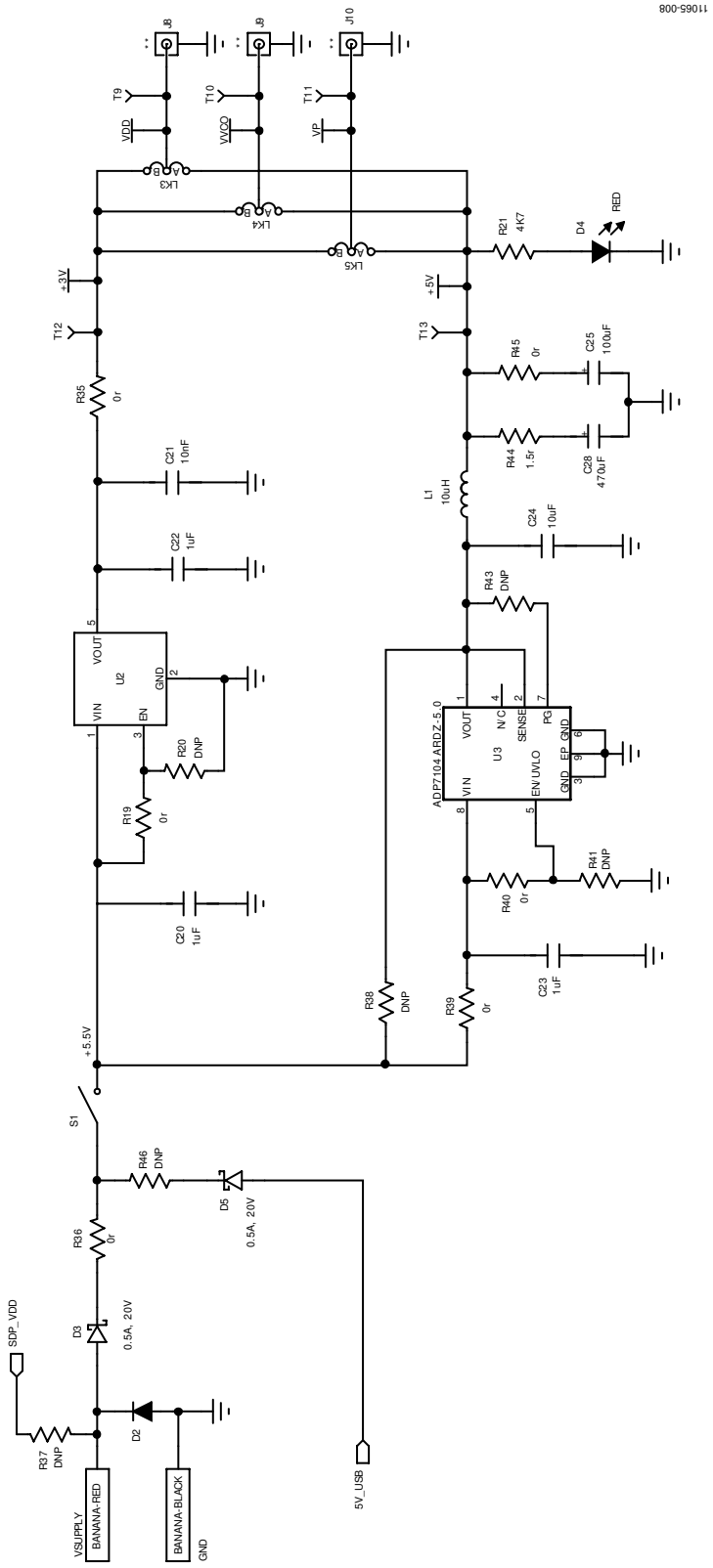

Figure 8. Evaluation Board Schematic (Page 2)

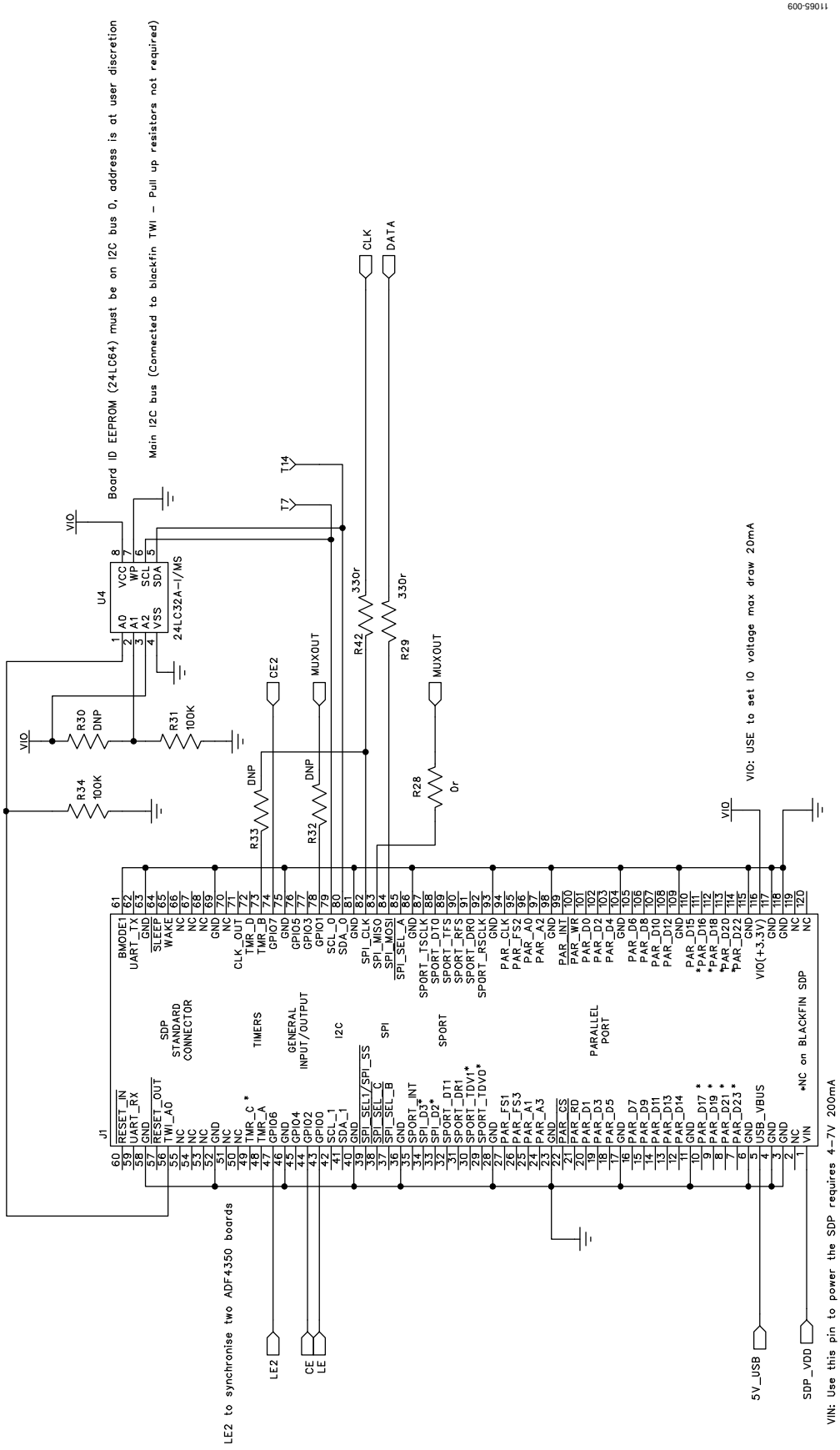

Figure 9. Evaluation Board Schematic (Page 3)

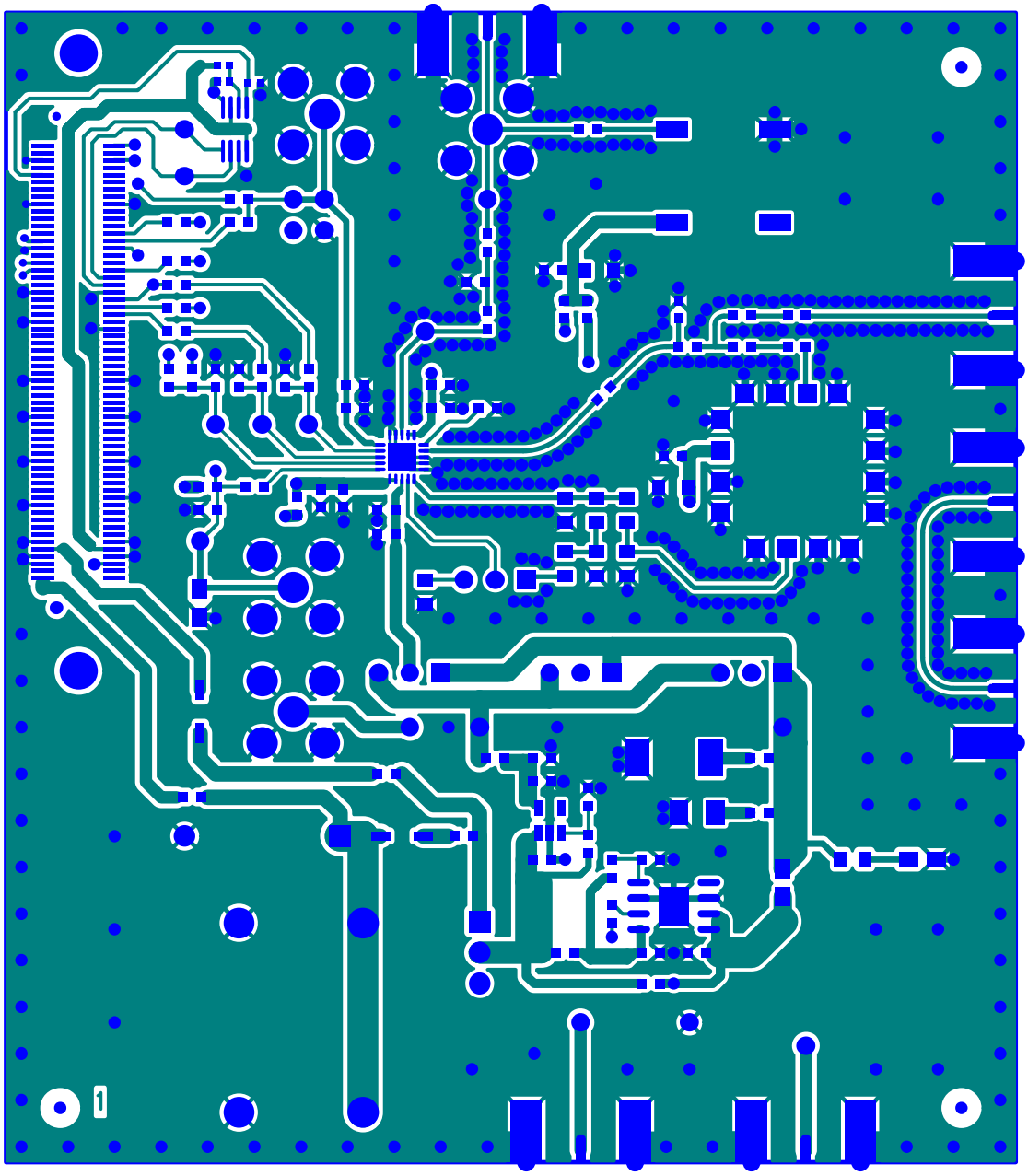

Figure 10. Layer 1 (Component Side)

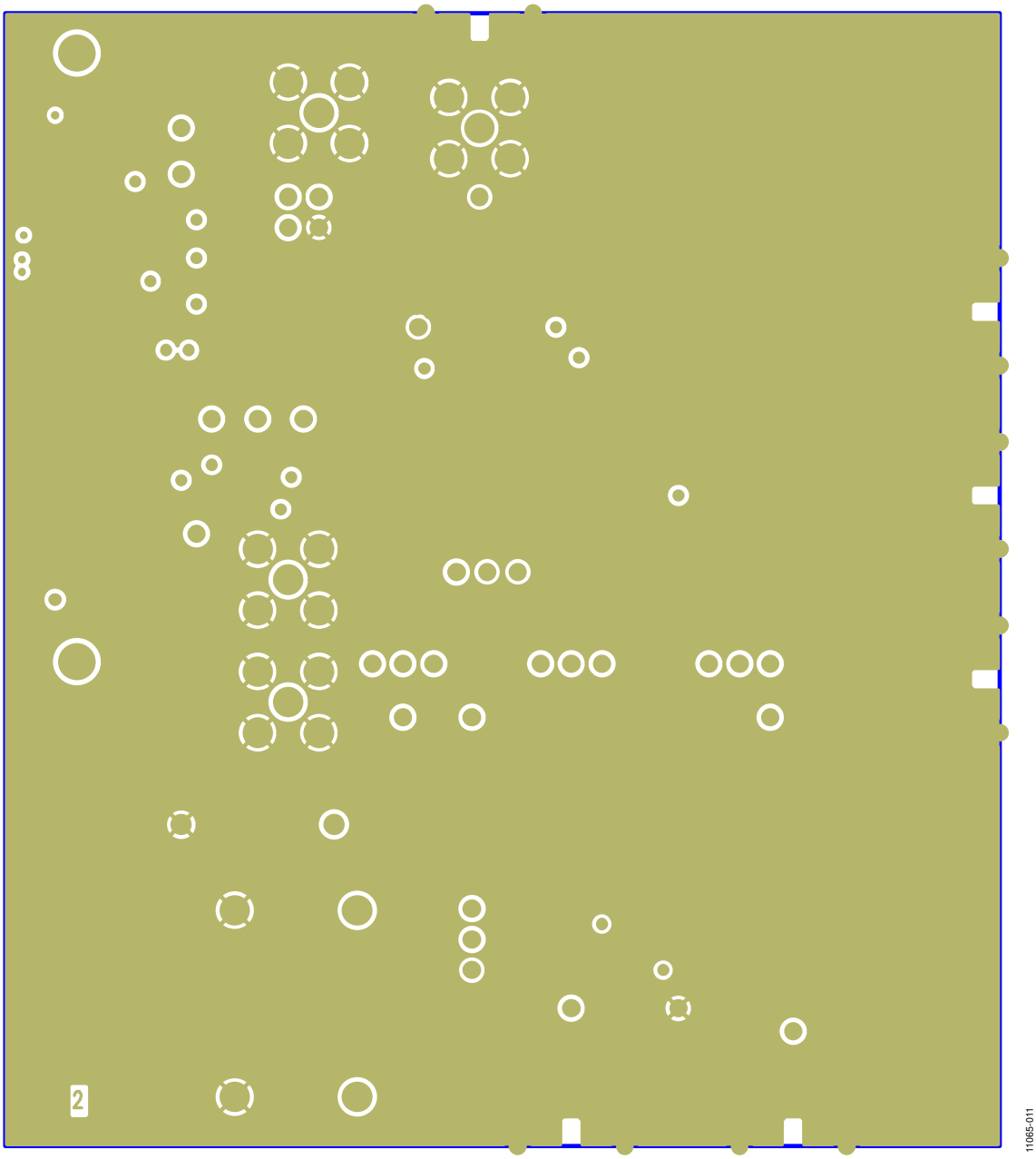

Figure 11. Layer 2 (Ground Plane)

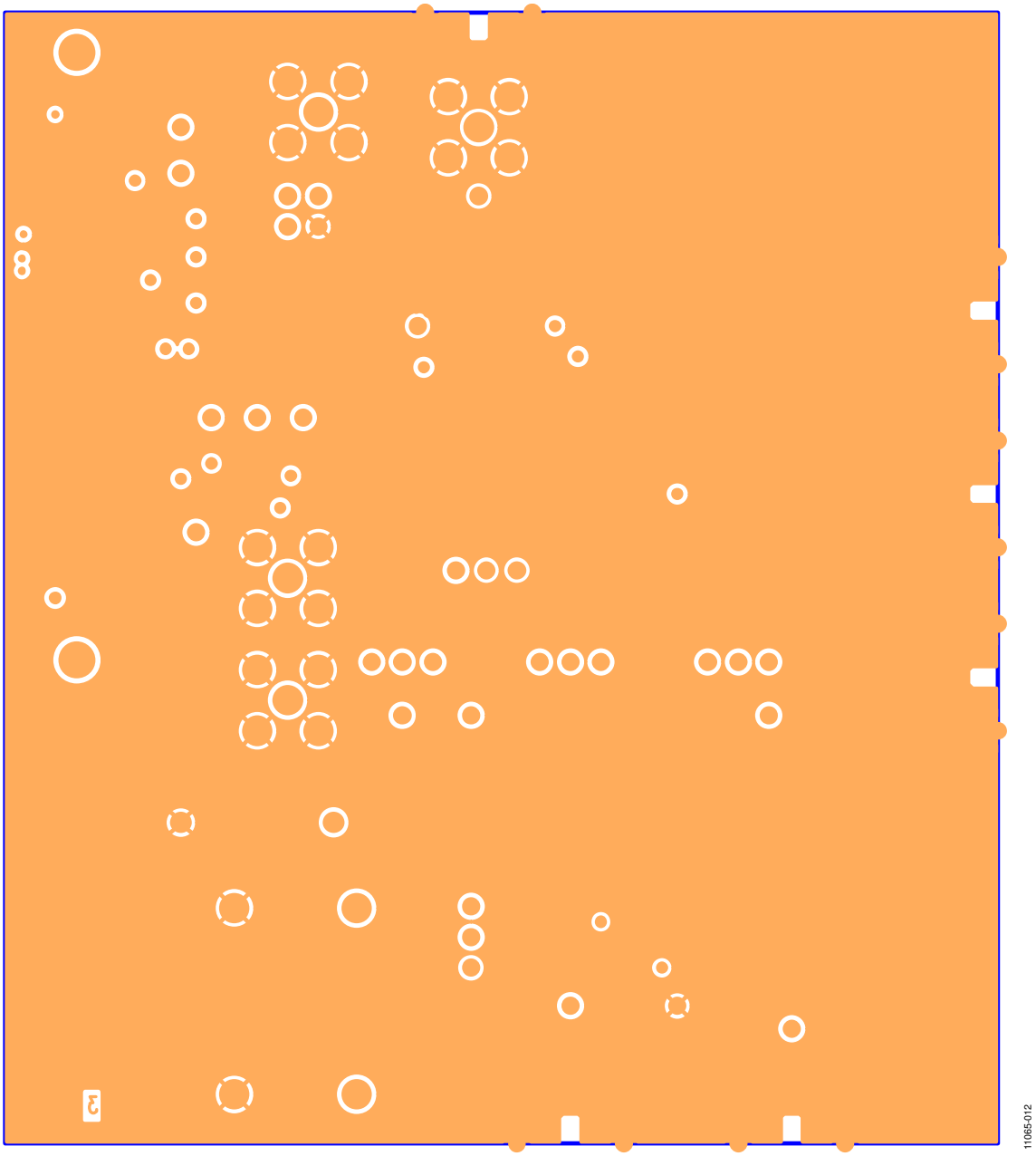

Figure 12. Layer 3 (Power Plane)

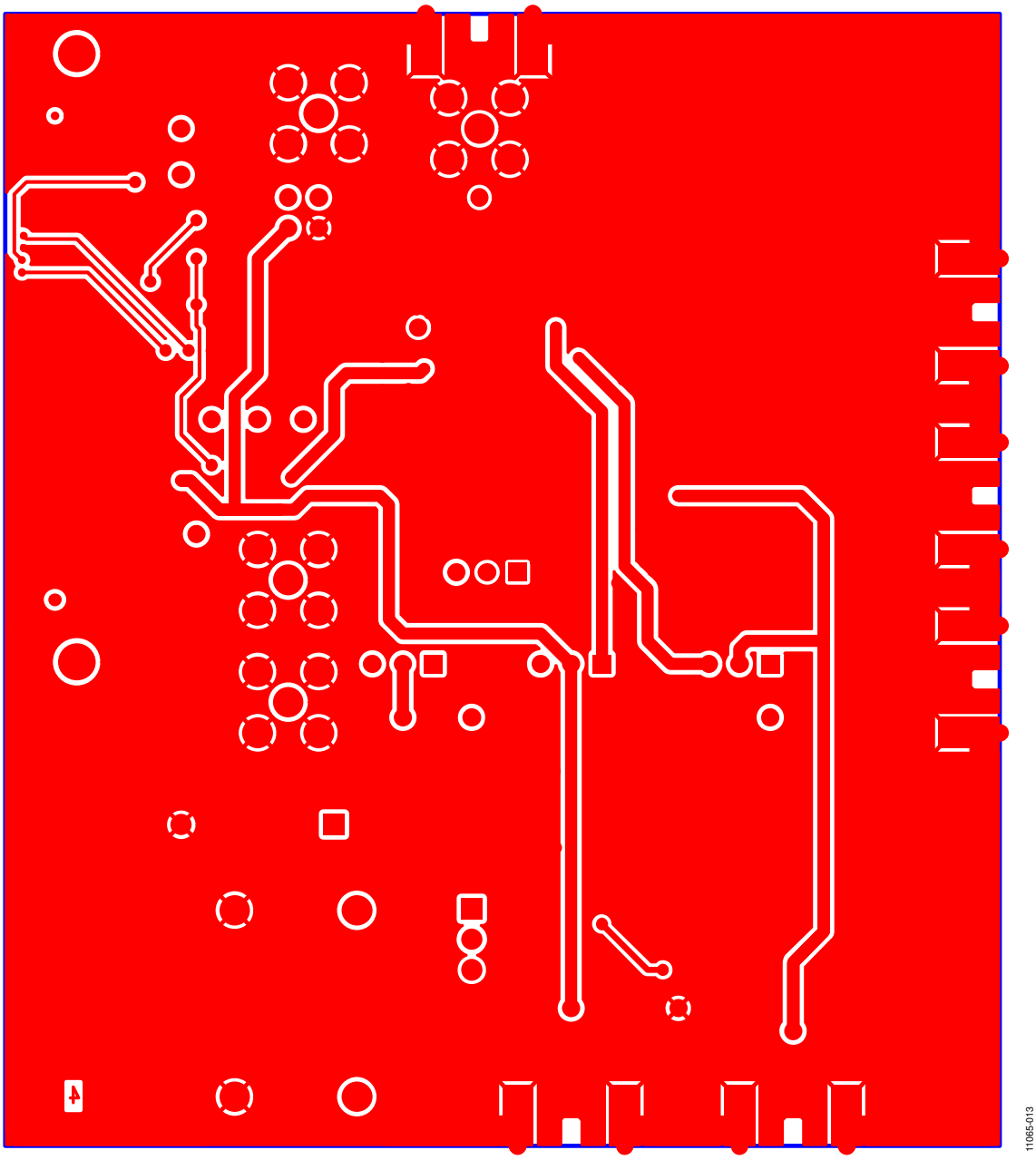

Figure 13. Layer 4 (Solder Side)

BILL OF MATERIALS

Table 2.

Reference Designator	Part Description	Manufacturer/Part No.
C1	Capacitor, 0603, 8.2 nF, 25 V, NP0	Kemet C0603C822J3GACTU
C2	Capacitor, 0603, 120 nF, 50 V, X7R	Kemet C0603C124K5RACTU
C3	Capacitor, 0603, 3.9 nF, 50 V	Kemet C0603C392J5GACTU
C4, C6, C10, C27	Capacitor, 0603, 0.1 µF, 16 V	AVX CM105X7R104K16AT
C5, C7, C9, C11, C13, C26	Capacitor, 0603, 10 pF, 50 V	AVX 06035A100JAT2A
C8, C12	Capacitor, Case A, 22 µF, 6.3 V	AVX TAJA226K006RNJ
C14, C15	Capacitor, 0603, 1 nF, 50 V	AVX 06035A102JAT2A
C16, C17, C18, C19	Capacitor, 0603, 100 pF, 50 V	AVX 06035A101JAT2A
C20, C22, C23	Capacitor, 0603, 1 µF, 10 V	Murata GRM188R61A105KA61D
C21	Capacitor, 0603, 10 nF, 50 V	AVX 06035C103JAT2A
C24	Capacitor, 0603, X5R, 10 µF V, 10 V	AVX 00603ZD106MAT2A
C25	Capacitor, Case B, 100 µF, 6.3 V	AVX TAJB107K006R
C28	Capacitor, Case D, 470 µF, 6.3 V	AVX TAJD477K006R
D1	LED, green	OSRAM LGR971-Z
D2	Diode, DO41, 1 A, 50 V	Multicomp 1N4001
D3, D5	SD103C, 6.2 V	ON Semiconductor MBR0520LT1G
D4	LED, red	Avago HSMS-C170
J1	120-way connector, 0.6 mm pitch	Hirose FX8-120S-SV(21)
J2	Jack, SMA, SMA_EDGE	Emerson 142-0701-851
J3, J4, J10, J11	Jack, SMA, receptacle straight PCB	Not inserted
J5, J6, J7, J8, J9	Jack, SMA, SMA_EDGE	Not inserted
L1	Inducor, 0805, 10 µH	KEMET L0805C100MDWIT
LK1, LK3, LK4, LK5	Jumper-2\SIP3, Link-3P	Harwin M20-9990345 and M7566-05
LK2	Jumper-2	Harwin M20-9990245 and M7566-05
GND	Black 4 mm banana socket	Deltron 571-0100-01
VSUPPLY	Red 4 mm banana socket	Deltron 571-0500-01
R1A	Resistor, 0805	Not inserted
R1	Resistor, 0603, 120 Ω	Multicomp MC 0.063 0603 1% 120R
R2	Resistor, 0603, 240 Ω	Multicomp MC 0.063 0603 1% 240R
R3	Resistor, 0805, 5.1 kΩ, ±1%, 0.1 W	Multicomp MC 0.1 0805 1% 5K1
R4, R5, R6, R23, R29, R42	Resistor, 0603, 330 Ω	Multicomp MC 0.063W 0603 1% 330R
R7, R8, R9	Resistor, 0603, 18 Ω	Multicomp MC 0.063W 0603 1% 18R
R10, R17	Resistor, 0603, 51 Ω	Multicomp MC 0.063W 0603 1% 51R
R11	Resistor, 0603 100 Ω	Multicomp MC 0.0625W 0402 1% 100R
R12, R13, R24, R25, R26	Resistor, 0603, 10 kΩ	Multicomp MC 0.063W 0603 1% 10K
R14, R16, R18, R19, R28, R35, R36, R39, R40, R45	Resistor, 0603, 0 Ω	Multicomp MC 0.063W 0603 1% 0R
R15, R20, R22, R27, R32, R33, R37, R38, R41, R43, R46	Resistor, 0603	Not inserted
R21	Resistor, 0603, 4.7 kΩ, ±1%, 0.063 W	Multicomp MC 0.063W 0603 1% 4K7
R30	Resistor, 0402	Not inserted
R31, R34	Resistor, RC31, 0402, 100 kΩ	YAGEO (Phycomp) RC0402JR-07100KL
R44	Resistor, 0603, 1.5 Ω	Multicomp MC 0.063W 0603 1% 1R5
S1	Switch, PCB, SPDT, 20 V	APEM TL36P0050
T1 to T14	Test point, PCB, red PK_100	Vero 20-313137
U1	ADF4153A, 20-lead LFCSP	ADF4153ABCPZ
U2	ADP150, 5-lead TSOT-5	ADP150AUJZ-3.0
U3	ADP7104, 8-lead SOIC	ADP7104ARDZ-5.0
U4	32k I^2C serial EEPROM, MSOP8	Microchip 24LC32A-I/MS
Y1	1700 MHz to 1800 MHz VCO	Mini-Circuits ROS-1800+
Y2	25 MHz, SMD, temperature compensated crystal oscillator	Rakon TXO225B

RELATED LINKS

Resource	Description
ADF4153A	Product Page, Fractional-N Frequency Synthesizer
ADP150	Product Page, Ultralow Noise 150 mA CMOS Linear Regulator
ADP7104	Product Page, 20 V, 500 mA Low Noise, CMOS Low-Dropout Linear Regulator

NOTES

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I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG11065-0-12/12(0)

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